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PIC16(L)F1784/6/7

28-Pin 8-Bit Advanced Analog Flash Microcontroller

High-Performance RISC CPU:

- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
- Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Memory Features:

- Up to 8 KW Flash Program Memory:
  - Self-programmable under software control
  - Programmable code protection
  - Programmable write protection
- 256 Bytes of Data EEPROM
- Up to 1024 Bytes of RAM

High-Performance PWM Controller:

- Three Programmable Switch Mode Controller (PSMC) modules:
  - Digital and/or analog feedback control of PWM frequency and pulse begin/end times
  - 16-bit Period, Duty Cycle and Phase
  - 16 ns clock resolution
  - Supports Single PWM, Complementary, Push-Pull and 3-phase modes of operation
  - Dead-band control with 8-bit counter
  - Auto-shutdown and restart
  - Leading and falling edge blanking
  - Burst mode

Extreme Low-Power Management PIC16LF1784/6/7 with XLP:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Timer1 Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 μA @ 32 kHz, 1.8V, typical
  - 32 μA/MHz @ 1.8V, typical

Analog Peripheral Features:

- Analog-to-Digital Converter (ADC):
  - Fully differential 12-bit converter
  - Up to 75 ksps conversion rate
  - 11 single-ended channels
  - 5 differential channels
  - Positive and negative reference selection
- 8-bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Positive and negative reference selection
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Four High-Speed Comparators:
  - 50 ns response time @ V_{DD} = 5V
  - Rail-to-rail inputs
  - Software selectable hysteresis
  - Internal connection to op amps, FVR and DAC
- Up to three Operational Amplifiers:
  - Rail-to-rail inputs/outputs
  - High/Low selectable Gain Bandwidth Product
  - Internal connection to DAC and FVR
- Fixed Voltage Reference (FVR):
  - 1.024V, 2.048V and 4.096V output levels
  - Internal connection to ADC, comparators and DAC

I/O Features:

- Up to 36 I/O Pins and 1 Input-only Pin:
- High Current Sink/Source for LED Drivers
- Individually Programmable Interrupt-on-Change Pins
- Individually Programmable Weak Pull-Ups
- Individual Input Level Selection
- Individually Programmable Slew Rate Control
- Individually Programmable Open Drain Outputs

Digital Peripheral Features:

- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture/Compare/PWM modules (CCP):
  - 16-bit capture, maximum resolution 12.5 ns
  - 16-bit compare, max resolution 31.25 ns
  - 10-bit PWM, max frequency 32 kHz
- Master Synchronous Serial Port (SSP) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-baud detect
  - Auto-wake-up on start

Oscillator Features:

- Operate up to 32 MHz from Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 32.768 kHz Timer1 Oscillator:
  - Available as system clock
  - Low-power RTC
- External Oscillator Block with:
  - 4 crystal/resonator modes up to 32 MHz using 4x PLL
  - 3 external clock modes up to 32 MHz
- 4x Phase-Locked Loop (PLL)
- Fail-Safe Clock Monitor:
  - Detect and recover from external oscillator failure
- Two-Speed Start-up:
  - Minimize latency between code execution and external oscillator start-up

General Microcontroller Features:

- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debug (ICD)
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1784/6/7)
  - 2.3V to 5.5V (PIC16F1784/6/7)

PIC16(L)F178X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	Data SRAM (bytes)	I/O's(2)	12-bit ADC (ch)	Comparators	Operational Amplifiers	DAC (8/5-bit)	Timers (8/16-bit)	Programmable Switch Mode Controllers (PSMC)	CCP	EUSART	MSSP (I^2C™/SPI)	Debug(1)	XLP
PIC16(L)F1782	(1)	2048	256	256	25	11	3	2	1/0	2/1	2	2	1	1	I	Y
PIC16(L)F1783	(1)	4096	256	512	25	11	3	2	1/0	2/1	2	2	1	1	I	Y
PIC16(L)F1784	(2)	4096	256	512	36	15	4	3	1/0	2/1	3	3	1	1	I	Y
PIC16(L)F1786	(2)	8192	256	1024	25	11	4	2	1/0	2/1	3	3	1	1	I	Y
PIC16(L)F1787	(2)	8192	256	1024	36	15	4	3	1/0	2/1	3	3	1	1	I	Y
PIC16(L)F1788	(3)	16384	256	2048	25	11	4	2	1/3	2/1	4	3	1	1	I	Y
PIC16(L)F1789	(3)	16384	256	2048	36	15	4	3	1/3	2/1	4	3	1	1	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

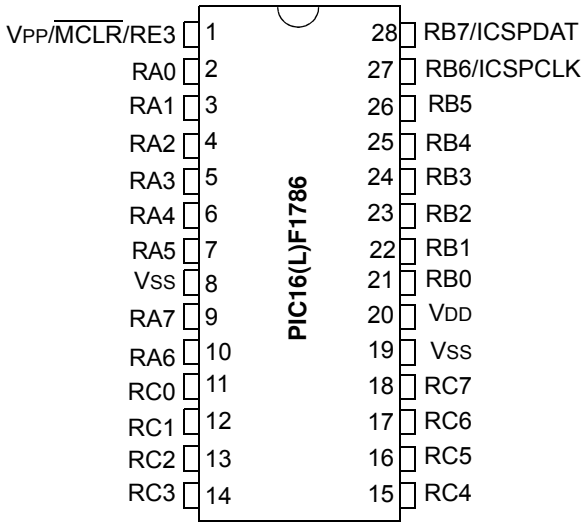
1: DS40001579 PIC16(L)F1782/3 Data Sheet, 28-Pin Flash, 8-bit Advanced Analog MCUs.

2: DS40001637 PIC16(L)F1784/6/7 Data Sheet, 28/40/44-Pin Flash, 8-bit Advanced Analog MCUs.

3: DS40001675 PIC16(L)F1788/9 Data Sheet, 28/40/44-Pin Flash, 8-bit Advanced Analog MCUs.

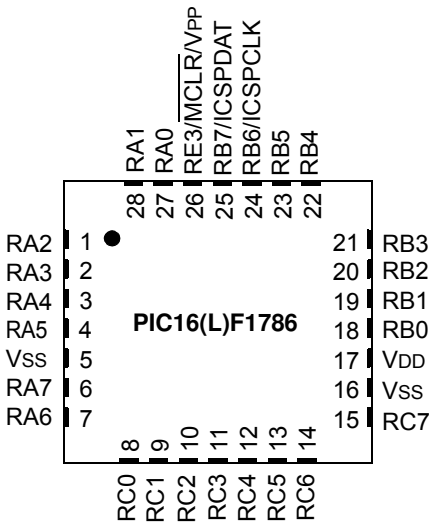
Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

Pin Diagram – 28-Pin SPDIP, SOIC, SSOP



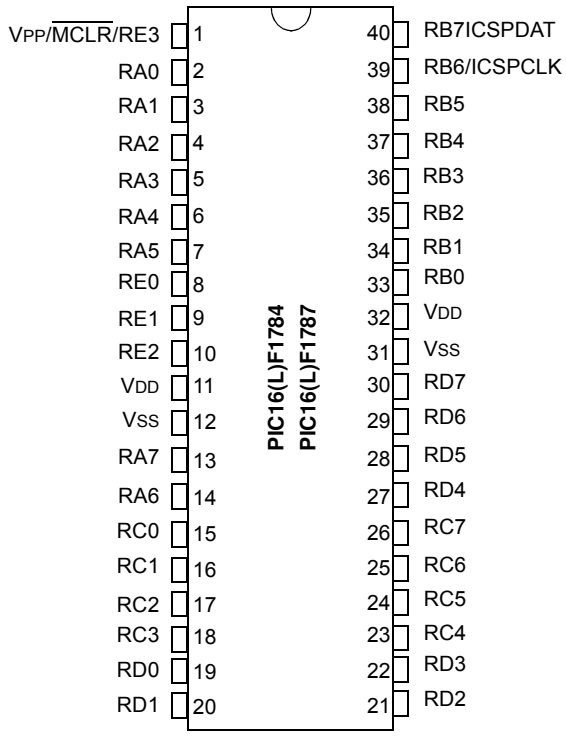
Note: See Table 1 for the location of all peripheral functions.

Pin Diagram – 28-Pin QFN



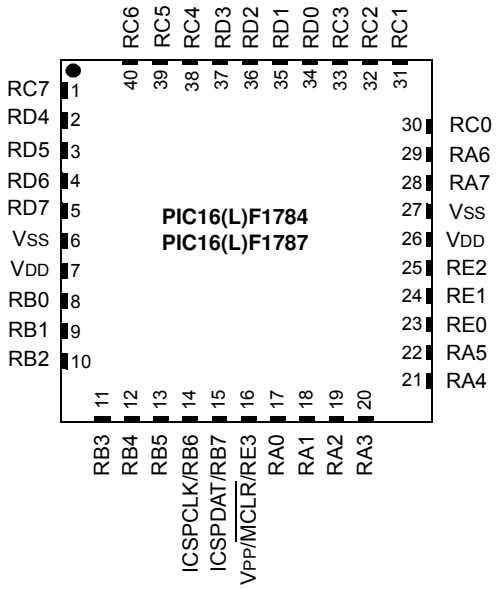
Note: See Table 1 for the location of all peripheral functions.

Pin Diagram – 40-Pin PDIP



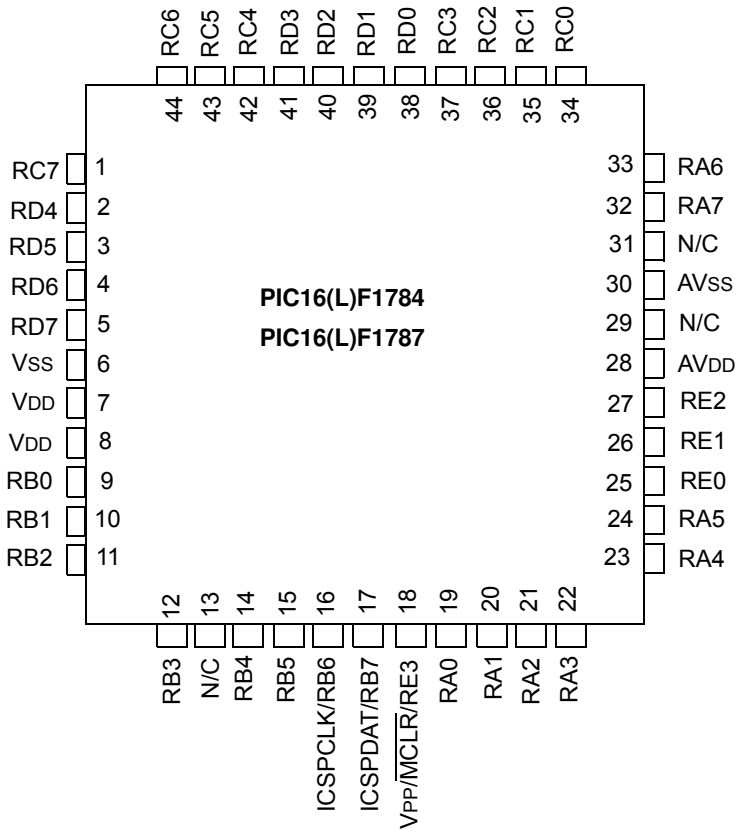
Note: See Table 2 for the location of all peripheral functions.

Pin Diagram – 40-Pin UQFN (5x5)



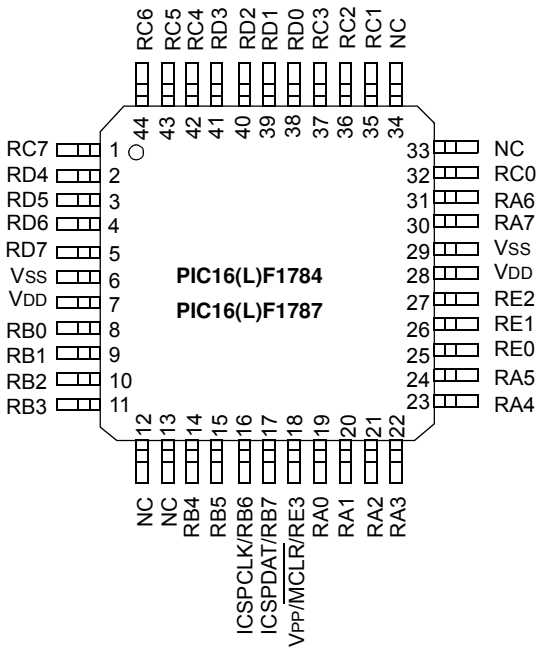
Note: See Table 2 for the location of all peripheral functions.

Pin Diagram – 44-Pin QFN



Note: See Table 2 for the location of all peripheral functions.

Pin Diagram – 44-Pin TQFP



Note: See Table 2 for the location of all peripheral functions.

PIN ALLOCATION TABLE

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1786)

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN,	ADC	Reference	Comparator	Operation Amplifiers	8-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN0	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	—	IOC	Y	—
RA1	3	28	AN1	—	C1IN1- C2IN1- C3IN1- C4IN1-	OPA1OUT	—	—	—	—	—	—	IOC	Y	—
RA2	4	1	AN2	VREF- DAC1VREF-	C1IN0+ C2IN0+ C3IN0+ C4IN0+		DAC1OUT1	—	—	—	—	—	IOC	Y	—
RA3	5	2	AN3	VREF+ DAC1VREF+	C1IN1+	—	—	—	—	—	—	—	IOC	Y	—
RA4	6	3	—	—	C1OUT	OPA1IN+	—	T0CKI	—	—	—	—	IOC	Y	—
RA5	7	4	AN4	—	C2OUT	OPA1IN-	—	—	—	—	—	$\overline{SS}$	IOC	Y	—
RA6	10	7	—	—	C2OUT(1)	—	—	—	—	—	—	—	IOC	Y	VCAP OSC2 CLKOUT
RA7	9	6	—	—	—	—	—	—	PSMC1CLK PSMC2CLK PSMC3CLK	—	—	—	IOC	Y	OSC1 CLKIN
RB0	21	18	AN12	—	C2IN1+	—	—	—	PSMC1IN PSMC2IN PSMC3IN	CCP1(1)	—	—	INT IOC	Y	—
RB1	22	19	AN10	—	C1IN3- C2IN3- C3IN3- C4IN3-	OPA2OUT	—	—	—	—	—	—	IOC	Y	—
RB2	23	20	AN8	—	—	OPA2IN-	—	—	—	—	—	—	IOC	Y	CLKR
RB3	24	21	AN9	—	C1IN2- C2IN2- C3IN2-	OPA2IN+	—	—	—	CCP2(1)	—	—	IOC	Y	—
RB4	25	22	AN11	—	C3IN1+	—	—	—	—	—	—	—	IOC	Y	—
RB5	26	23	AN13	—	C4IN2- C3OUT	—	—	T1G	—	CCP3(1)	—	SDO(1)	IOC	Y	—
RB6	27	24	—	—	C4IN1+	—	—	—	—	—	TX(1) CK(1)	SDI(1) SDA(1)	IOC	Y	ICSPCLK

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1786) (Continued)

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN,	ADC	Reference	Comparator	Operation Amplifiers	8-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RB7	28	25	—	—	—	—	DAC1OUT2	—	—	—	RX(1) DT(1)	SCK(1) SCL(1)	IOC	Y	ICSPDAT
RC0	11	8	—	—	—	—	—	T1OSO T1CKI	PSMC1A	—	—	—	IOC	Y	—
RC1	12	9	—	—	—	—	—	T1OSI	PSMC1B	CCP2	—	—	IOC	Y	—
RC2	13	10	—	—	—	—	—	—	PSMC1C PSMC3B	CCP1	—	—	IOC	Y	—
RC3	14	11	—	—	—	—	—	—	PSMC1D	—	—	SCK SCL	IOC	Y	—
RC4	15	12	—	—	—	—	—	—	PSMC1E	—	—	SDI SDA	IOC	Y	—
RC5	16	13	—	—	—	—	—	—	PSMC1F PSMC3A	—	—	SDO	IOC	Y	—
RC6	17	14	—	—	—	—	—	—	PSMC2A	CCP3	TX CK	—	IOC	Y	—
RC7	18	15	—	—	C4OUT	—	—	—	PSMC2B	—	RX DT	—	IOC	Y	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ V_{PP}
V_{DD}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8, 19	5, 16	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

TABLE 2: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1784/7)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Op Amps	8-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	17	19	19	AN0	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	—	IOC	Y	—
RA1	3	18	20	20	AN1	—	C1IN1- C2IN1- C3IN1- C4IN1-	OPA1OUT	—	—	—	—	—	—	IOC	Y	—
RA2	4	19	21	21	AN2	DAC1VREF- VREF-	C1IN0+ C2IN0+ C3IN0+ C4IN0+		DAC1OUT1	—	—	—	—	—	IOC	Y	—
RA3	5	20	22	22	AN3	DAC1VREF+ VREF+	C1IN1+	—	—	—	—	—	—	—	IOC	Y	—
RA4	6	21	23	23	—	—	C1OUT	OPA1IN+	—	T0CKI	—	—	—	—	IOC	Y	—
RA5	7	22	24	24	AN4	—	C2OUT	OPA1IN-	—	—	—	—	—	$\overline{SS}$	IOC	Y	—
RA6	14	29	31	33	—	—	C2OUT(1)	—	—	—	—	—	—	—	IOC	Y	VCAP CLKOUT OSC2
RA7	13	28	30	32	—	—	—	—	—	—	PSMC1CLK PSMC2CLK PSMC3CLK	—	—	—	IOC	Y	CLKIN OSC1
RB0	33	8	8	9	AN12	—	C2IN1+	—	—	—	PSMC1IN PSMC2IN PSMC3IN	CCP1(1)	—	—	INT IOC	Y	—
RB1	34	9	9	10	AN10	—	C1IN3- C2IN3- C3IN3- C4IN3-	OPA2OUT	—	—	—	—	—	—	IOC	Y	—
RB2	35	10	10	11	AN8	—	—	OPA2IN-	—	—	—	—	—	—	IOC	Y	CLKR
RB3	36	11	11	12	AN9	—	C1IN2- C2IN2- C3IN2-	OPA2IN+	—	—	—	CCP2(1)	—	—	IOC	Y	—
RB4	37	12	14	14	AN11	—	C3IN1+	—	—	—	—	—	—	—	IOC	Y	—
RB5	38	13	15	15	AN13	—	C4IN2-	—	—	T1G	—	CCP3(1)	—	SDO(1)	IOC	Y	—
RB6	39	14	16	16	—	—	C4IN1+	—	—	—	—	—	TX(1) CK(1)	SDA(1) SDI(1)	IOC	Y	ICSPCLK
RB7	40	15	17	17	—	—	—	—	DAC1OUT2	—	—	—	RX(1) DT(1)	SCL(1) SCK(1)	IOC	Y	ICSPDAT
RC0	15	30	32	34	—	—	—	—	—	T1CKI T1OSO	PSMC1A	—	—	—	IOC	Y	—

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

TABLE 2: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1784/7) (Continued)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Op Amps	8-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RC1	16	31	35	35	—	—	—	—	—	T1OSI	PSMC1B	CCP2	—	—	IOC	Y	—
RC2	17	32	36	36	—	—	—	—	—	—	PSMC1C	CCP1	—	—	IOC	Y	
RC3	18	33	37	37	—	—	—	—	—	—	PSMC1D	—	—	SCL SCK	IOC	Y	—
RC4	23	38	42	42	—	—	—	—	—	—	PSMC1E	—	—	SDI SDA	IOC	Y	—
RC5	24	39	43	43	—	—	—	—	—	—	PSMC1F	—	—	SDO	IOC	Y	—
RC6	25	40	44	44	—	—	—	—	—	—	PSMC2A	—	TX CK	—	IOC	Y	—
RC7	26	1	1	1	—	—	—	—	—	—	PSMC2B	—	RX DT	—	IOC	Y	—
RD0	19	34	38	38	—	—	—	OPA3IN+	—	—	—	—	—	—	—	Y	—
RD1	20	35	39	39	AN21	—	C1IN4- C2IN4- C3IN4- C4IN4-	OPA3OUT	—	—	—	—	—	—	—	Y	—
RD2	21	36	40	40	—	—	—	OPA3IN-	—	—	—	—	—	—	—	Y	—
RD3	22	37	41	41	—	—	—	—	—	—	—	—	—	—	—	Y	
RD4	27	2	2	2	—	—	—	—	—	—	PSMC3F	—	—	—	—	Y	—
RD5	28	3	3	3	—	—	—	—	—	—	PSMC3E	—	—	—	—	Y	—
RD6	29	4	4	4	—	—	C3OUT	—	—	—	PSMC3D	—	—	—	—	Y	—
RD7	30	5	5	5	—	—	C4OUT	—	—	—	PSMC3C	—	—	—	—	Y	—
RE0	8	23	25	25	AN5	—	—	—	—	—	—	CCP3	—	—	—	Y	—
RE1	9	24	26	26	AN6	—	—	—	—	—	PSMC3B	—	—	—	—	Y	—
RE2	10	25	27	27	AN7	—	—	—	—	—	PSMC3A	—	—	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ V_{PP}
V_{DD}	11,32	7,26	7,28	7,8, 28	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
Vss	12,31	6,27	6,29	6,30,	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

Table of Contents

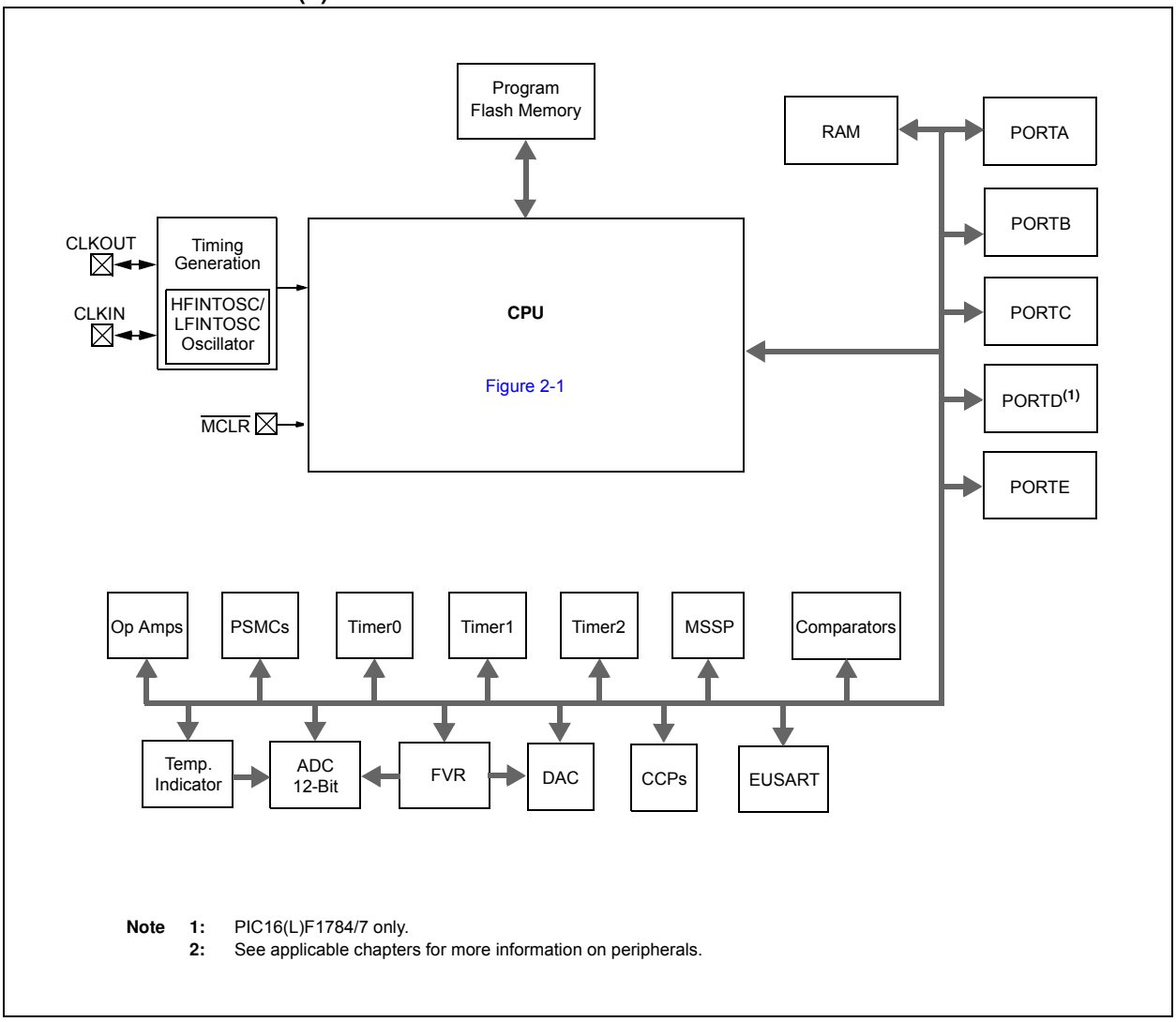
1.0 DEVICE OVERVIEW

The PIC16(L)F1784/6/7 are described within this data sheet. The block diagram of these devices are shown in Figure 1-1. The available peripherals are shown in Table 1-1, and the pin out descriptions are shown in Table 1-2.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1782	PIC16(L)F1783	PIC16(L)F1784	PIC16(L)F1786	PIC16(L)F1787	PIC16(L)F1788	PIC16(L)F1789
Analog-to-Digital Converter (ADC)		•	•	•	•	•	•	•
Fixed Voltage Reference (FVR)		•	•	•	•	•	•	•
Reference Clock Module		•	•	•	•	•	•	•
Temperature Indicator		•	•	•	•	•	•	•
Capture/Compare/PWM (CCP/ECCP) Modules								
	CCP1	•	•	•	•	•	•	•
	CCP2	•	•	•	•	•	•	•
	CCP3			•	•	•	•	•
Comparators								
	C1	•	•	•	•	•	•	•
	C2	•	•	•	•	•	•	•
	C3	•	•	•	•	•	•	•
	C4			•	•	•	•	•
Digital-to-Analog Converter (DAC)								
	(8-bit DAC) D1	•	•	•	•	•	•	•
	(5-bit DAC) D2							•
	(5-bit DAC) D3							•
	(5-bit DAC) D4							•
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)								
	EUSART	•	•	•	•	•	•	•
Master Synchronous Serial Ports								
	MSSP	•	•	•	•	•	•	•
Op Amp								
	Op Amp 1	•	•	•	•	•	•	•
	Op Amp 2	•	•	•	•	•	•	•
	Op Amp 3			•		•		•
Programmable Switch Mode Controller (PSMC)								
	PSMC1	•	•	•	•	•	•	•
	PSMC2	•	•	•	•	•	•	•
	PSMC3			•	•	•	•	•
	PSMC4						•	•
Timers								
	Timer0	•	•	•	•	•	•	•
	Timer1	•	•	•	•	•	•	•
	Timer2	•	•	•	•	•	•	•

FIGURE 1-1: PIC16(L)F1784/6/7 BLOCK DIAGRAM



Note 1: PIC16(L)F1784/7 only.
2: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/ C3IN0-/C4IN0-	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	C3IN0-	AN	—	Comparator C3 negative input.
	C4IN0-	AN	—	Comparator C4 negative input.
RA1/AN1/C1IN1-/C2IN1-/ C3IN1-/C4IN1-/OPA1OUT	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	C3IN1-	AN	—	Comparator C3 negative input.
	C4IN1-	AN	—	Comparator C4 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
RA2/AN2/C1IN0+/C2IN0+/ C3IN0+/C4IN0+/DAC1OUT1/ VREF-/DAC1VREF-/OPA1IN-	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	C2IN0+	AN	—	Comparator C2 positive input.
	C3IN0+	AN	—	Comparator C3 positive input.
	C4IN0+	AN	—	Comparator C4 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	VREF-	AN	—	ADC Negative Voltage Reference input.
	DAC1VREF-	AN	—	Digital-to-Analog Converter negative reference.
RA3/AN3/VREF+/C1IN1+/ DAC1VREF+	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC Voltage Reference input.
	C1IN1+	AN	—	Comparator C1 positive input.
	DAC1VREF+	AN	—	Digital-to-Analog Converter positive reference.
RA4/C1OUT/OPA1IN+/T0CKI	RA4	TTL/ST	CMOS	General purpose I/O.
	C1OUT	—	CMOS	Comparator C1 output.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	T0CKI	ST	—	Timer0 clock input.
RA5/AN4/C2OUT(1)/OPA1IN-/ $\overline{SS}$	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	C2OUT	—	CMOS	Comparator C2 output.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	$\overline{SS}$	ST	—	Slave Select input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA6/C2OUT(1)/OSC2/ CLKOUT/VCAP	RA6	TTL/ST	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator.
RA7/PSMC1CLK/PSMC2CLK/ PSMC3CLK/OSC1/CLKIN	RA7	TTL/ST	CMOS	General purpose I/O.
	PSMC1CLK	ST	—	PSMC1 clock input.
	PSMC2CLK	ST	—	PSMC2 clock input.
	PSMC3CLK	ST	—	PSMC3 clock input.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	st	—	External clock input (EC mode).
RB0/AN12/C2IN1+/PSMC1IN/ PSMC2IN/PSMC3IN/CCP1(1)/ INT	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	PSMC1IN	ST	—	PSMC1 Event Trigger input.
	PSMC2IN	ST	—	PSMC2 Event Trigger input.
	PSMC3IN	ST	—	PSMC3 Event Trigger input.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	INT	ST	—	External interrupt.
RB1/AN10/C1IN3-/C2IN3-/ C3IN3-/C4IN3-/OPA2OUT	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	C3IN3-	AN	—	Comparator C3 negative input.
	C4IN3-	AN	—	Comparator C4 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
RB2/AN8/OPA2IN-/CLKR	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	CLKR	—	CMOS	Clock output.
RB3/AN9/C1IN2-/C2IN2-/ C3IN2-/OPA2IN+/CCP2(1)	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	C3IN2-	AN	—	Comparator C3 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RB4/AN11/C3IN1+	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
	C3IN1+	AN	—	Comparator C3 positive input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I2C™ = Schmitt Trigger input with I2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB5/AN13/C4IN2-/T1G/CCP3(1) SDO(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	C4IN2-	AN	—	Comparator C4 negative input.
	T1G	ST	—	Timer1 gate input.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SDO	—	CMOS	SPI data output.
RB6/C4IN1+/TX(1)/CK(1)/SDI(1)/ SDA(1)/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	C4IN1+	AN	—	Comparator C4 positive input.
	TX	—	CMOS	EUSART asynchronous transmit.
	CK	ST	CMOS	EUSART synchronous clock.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/DAC1OUT2/RX(1)/DT(1)/ SCK(1)/SCL(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DAC1OUT2	—	AN	Voltage Reference output.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C™ clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1OSO/T1CKI/PSMC1A	RC0	TTL/ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 Oscillator Connection.
	T1CKI	ST	—	Timer1 clock input.
	PSMC1A	—	CMOS	PSMC1 output A.
RC1/T1OSI/PSMC1B/CCP2	RC1	TTL/ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 Oscillator Connection.
	PSMC1B	—	CMOS	PSMC1 output B.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/PSMC1C/CCP1	RC2	TTL/ST	CMOS	General purpose I/O.
	PSMC1C	—	CMOS	PSMC1 output C.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/PSMC1D/SCK(1)/SCL(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	PSMC1D	—	CMOS	PSMC1 output D.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C™ clock.
RC4/PSMC1E/SDI(1)/SDA(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	PSMC1E	—	CMOS	PSMC1 output E.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC5/PSMC1F/SDO(1)	RC5	TTL/ST	CMOS	General purpose I/O.
	PSMC1F	—	CMOS	PSMC1 output F.
	SDO	—	CMOS	SPI data output.
RC6/PSMC2A/TX(1)/CK(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	PSMC2A	—	CMOS	PSMC2 output A.
	TX	—	CMOS	EUSART asynchronous transmit.
	CK	ST	CMOS	EUSART synchronous clock.
RC7/PSMC2B/RX(1)/DT(1)/ C4OUT(4)	RC7	TTL/ST	CMOS	General purpose I/O.
	PSMC2B	—	CMOS	PSMC2 output B.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.
	C4OUT	—	CMOS	Comparator C4 output.
RD0(3)/OPA3IN+	RD0	TTL/ST	CMOS	General purpose I/O.
	OPA3IN+	AN	—	Operational Amplifier 3 non-inverting input.
RD1(3)/AN21/C1IN4-/C2IN4-/ C3IN4-/C4IN4-/OPA3OUT	RD1	TTL/ST	CMOS	General purpose I/O.
	AN21	AN	—	ADC Channel 21 input.
	C1IN4-	AN	—	Comparator C4 negative input.
	C2IN4-	AN	—	Comparator C4 negative input.
	C3IN4-	AN	—	Comparator C4 negative input.
	C4IN4-	AN	—	Comparator C4 negative input.
	OPA3OUT	—	AN	Operational Amplifier 3 output.
RD2(3)/OPA3IN-	RD2	TTL/ST	CMOS	General purpose I/O.
	OPA3IN-	AN	—	Operational Amplifier 3 inverting input.
RD3(3)	RD3	TTL/ST	CMOS	General purpose I/O.
RD4(3)/PSMC3F	RD4	TTL/ST	CMOS	General purpose I/O.
	PSMC3F	—	CMOS	PSMC3 output F.
RD5(3)/PSMC3E	RD5	TTL/ST	CMOS	General purpose I/O.
	PSMC3E	—	CMOS	PSMC3 output E.
RD6(3)/C3OUT/PSMC3D	RD6	TTL/ST	CMOS	General purpose I/O.
	C3OUT	—	CMOS	Comparator C3 output.
	PSMC3D	—	CMOS	PSMC3 output D.
RD7(3)/C4OUT/PSMC3C	RD6	TTL/ST	CMOS	General purpose I/O.
	C4OUT	—	CMOS	Comparator C4 output.
	PSMC3C	—	CMOS	PSMC3 output C.
RE0(3)/AN5/CCP3(1)	RE0	TTL/ST	—	General purpose input.
	AN5	AN	—	ADC Channel 5 input.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
RE1(3)/AN6/PSMC3B	RE1	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	PSMC3B	—	CMOS	PSMC3 output B.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RE2(3)/AN7/PSMC3A	RE2	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	PSMC3A	—	CMOS	PSMC3 output A.
RE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

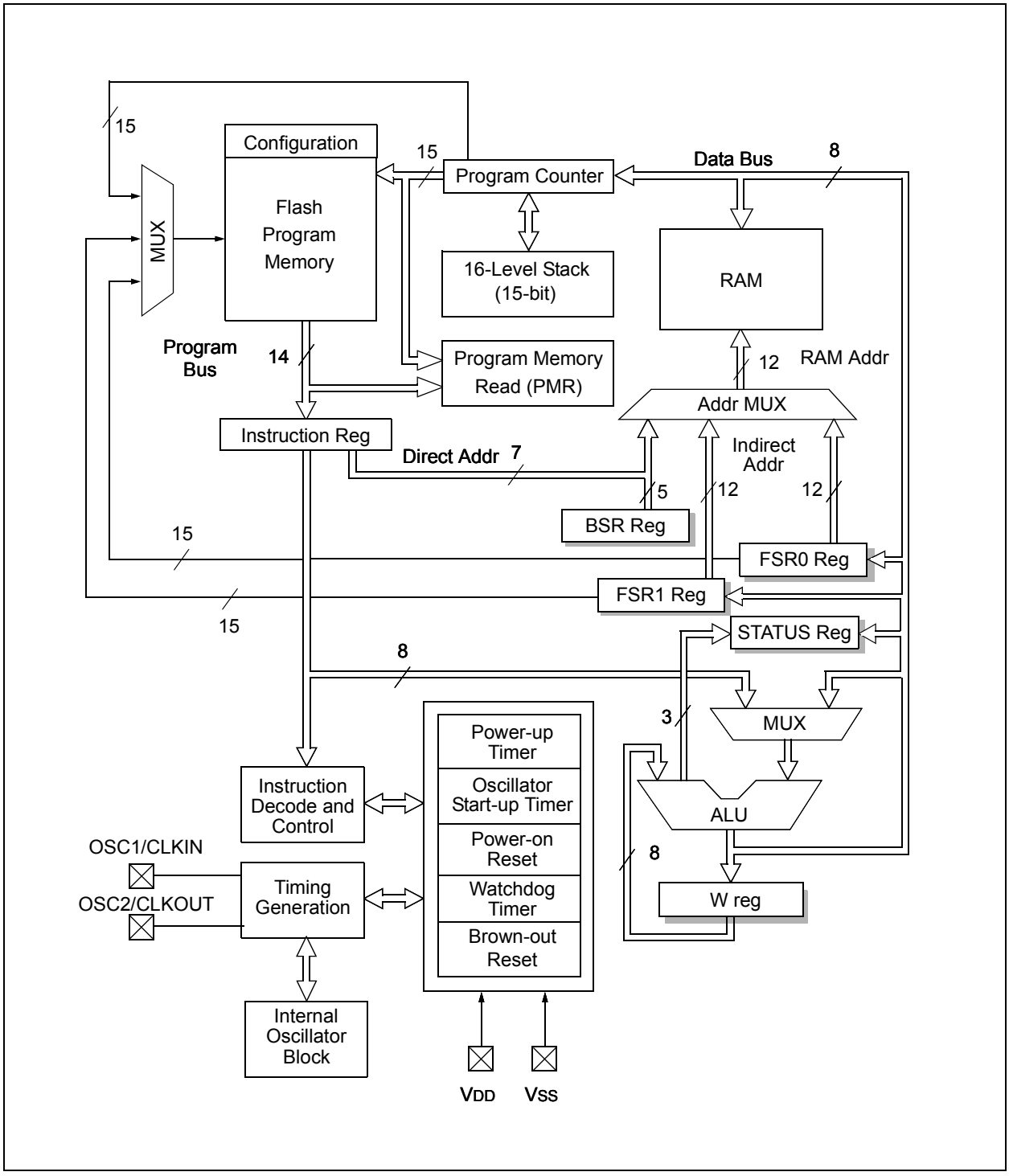
Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **8.5 "Automatic Context Saving"**, for more information.

2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See **Section 3.5 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.6 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 29.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
- Data EEPROM memory(1)

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in **Section 12.0 "Data EEPROM and Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1784/6/7 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1 and 3-2).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
PIC16(L)F1784	4,096	0FFFh
PIC16(L)F1786/7	8,192	1FFFh

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1786/7

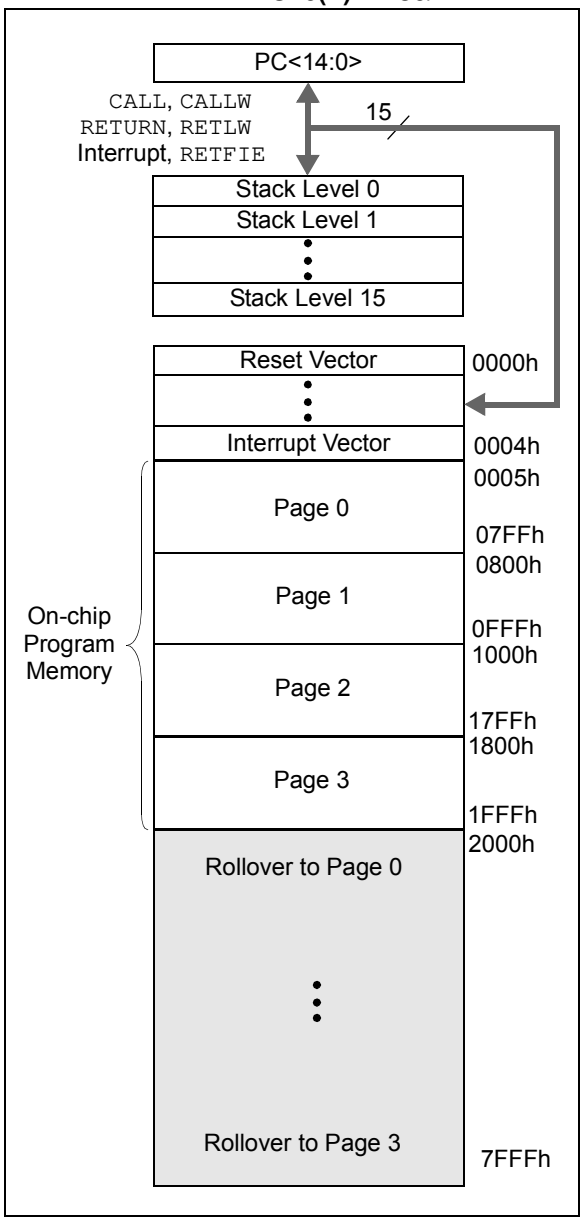
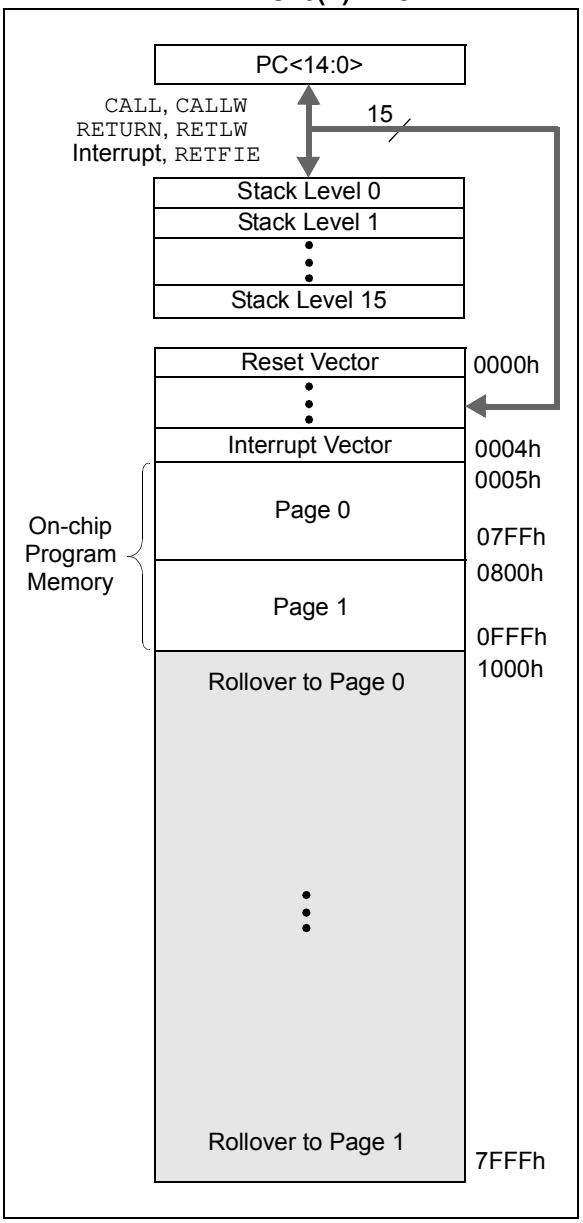


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1784



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The high directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```