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PIC16(L)F1826/27
Data Sheet

18/20/28-Pin Flash Microcontrollers with nanoWatt XLP Technology

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PIC16(L)F1826/27

18/20/28-Pin Flash Microcontrollers with nanoWatt XLP Technology

High-Performance RISC CPU:

- C Compiler Optimized Architecture
- 256 bytes Data EEPROM
- Up to 8 Kbytes Linear Program Memory Addressing
- Up to 384 bytes Linear Data Memory Addressing
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Flexible Oscillator Structure:

- Precision 32 MHz Internal Oscillator Block:
  - Factory calibrated to ± 1%, typical
  - Software selectable frequencies range of 31 kHz to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- Four Crystal modes up to 32 MHz
- Three External Clock modes up to 32 MHz
- 4X Phase-Lock Loop (PLL)
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Reference Clock Module:
  - Programmable clock output frequency and duty-cycle

Special Microcontroller Features:

- 1.8V-5.5V Operation – PIC16F1826/27
- 1.8V-3.6V Operation – PIC16LF1826/27
- Self-Programmable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT):
  - Programmable period from 1ms to 268s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Enhance Low-Voltage Programming
- Power-Saving Sleep mode

Extreme Low-Power Management PIC16LF1826/27 with nanoWatt XLP:

- Operating Current: 75 μA @ 1 MHz, 1.8V, typical
- Sleep mode: 30 nA
- Watchdog Timer: 500 nA
- Timer1 Oscillator: 600 nA @ 32 kHz

Analog Features:

- Analog-to-Digital Converter (ADC) Module:
  - 10-bit resolution, 12 channels
  - Auto acquisition capability
  - Conversion available during Sleep
- Analog Comparator Module:
  - Two rail-to-rail analog comparators
  - Power mode control
  - Software controllable hysteresis
- Voltage Reference Module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

Peripheral Highlights:

- 15 I/O Pins and 1 Input Only Pin:
  - High current sink/source 25 mA/25 mA
  - Programmable weak pull-ups
  - Programmable interrupt-on- change pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated, low-power 32 kHz oscillator driver
- Up to three Timer2-types: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Up to two Capture, Compare, PWM (CCP) Modules
- Up to two Enhanced CCP (ECCP) Modules:
  - Software selectable time bases
  - Auto-shutdown and auto-restart
  - PWM steering
- Up to two Master Synchronous Serial Port (MSSP) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) Module
- mTouch™ Sensing Oscillator Module:
  - Up to 12 input channels
- Data Signal Modulator Module:
  - Selectable modulator and carrier sources
- SR Latch:
  - Multiple Set/Reset input options
  - Emulates 555 Timer applications

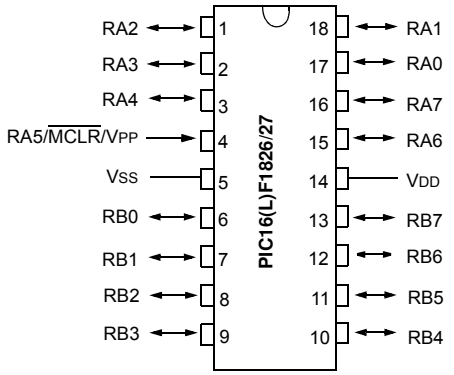
PIC16(L)F1826/27 Family Types

Device	Program Memory	Data Memory		I/O's(1)	10-bit ADC (ch)	CapSense (ch)	Comparators	Timers (8/16-bit)	EUSART	MSSP	ECCP (Full-Bridge)	ECCP (Half-Bridge)	CCP	SR Latch
	Words	SRAM (bytes)	Data EEPROM (bytes)											
PIC16LF1826	2K	256	256	16	12	12	2	2/1	1	1	1	—	—	Yes
PIC16F1826	2K	256	256	16	12	12	2	2/1	1	1	1	—	—	Yes
PIC16LF1827	4K	384	256	16	12	12	2	4/1	1	2	1	1	2	Yes
PIC16F1827	4K	384	256	16	12	12	2	4/1	1	2	1	1	2	Yes

Note 1: One pin is input only.

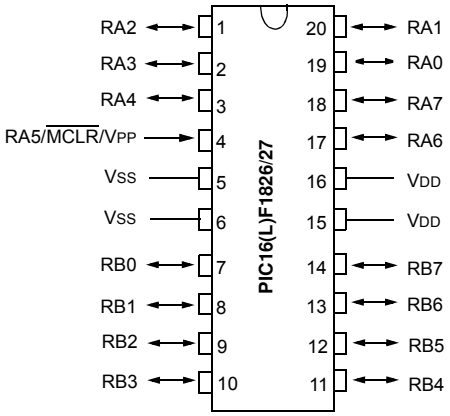
Pin Diagram – 18-Pin PDIP, SOIC (PIC16(L)F1826/27)

PDIP, SOIC



Pin Diagram – 20-Pin SSOP (PIC16(L)F1826/27)

SSOP



Pin Diagram – 28-Pin QFN/UQFN (PIC16(L)F1826/27)

QFN/UQFN

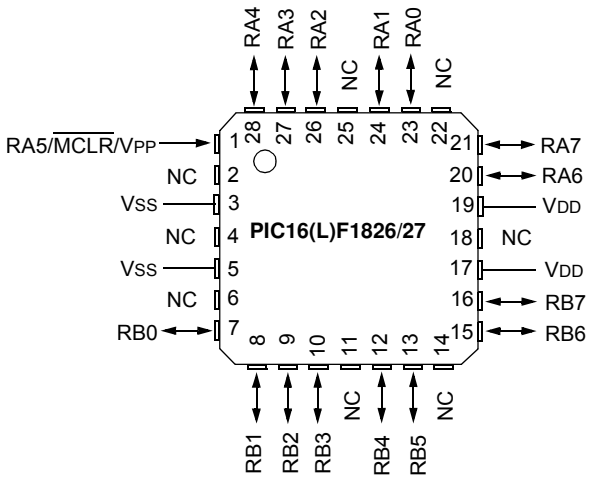


TABLE 1: 18/20/28-PIN SUMMARY (PIC16(L)F1826/27)

I/O	18-Pin PDIP/SOIC	20-Pin SSOP	28-Pin QFN/UQFN	ANSEL	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	MSSP	Interrupt	Modulator	Pull-up	Basic
RA0	17	19	23	Y	AN0	—	CPS0	C12IN0-	—	—	—	—	SDO2(2)	—	—	N	—
RA1	18	20	24	Y	AN1	—	CPS1	C12IN1-	—	—	—	—	$\overline{SS2}$(2)	—	—	N	—
RA2	1	1	26	Y	AN2	VREF- DACOUT	CPS2	C12IN2- C12IN+	—	—	—	—	—	—	—	N	—
RA3	2	2	27	Y	AN3	VREF+	CPS3	C12IN3- C1IN+ C1OUT	SRQ	—	CCP3(2)	—	—	—	—	N	—
RA4	3	3	28	Y	AN4	—	CPS4	C2OUT	SRNQ	T0CKI	CCP4(2)	—	—	—	—	N	—
RA5	4	4	1	N	—	—	—	—	—	—	—	—	$\overline{SS1}$(1)	—	—	Y(3)	$\overline{MCLR}$, VPP
RA6	15	17	20	N	—	—	—	—	—	—	P1D(1) P2B(1,2)	—	SDO1(1)	—	—	N	OSC2 CLKOUT CLKR
RA7	16	18	21	N	—	—	—	—	—	—	P1C(1) CCP2(1,2) P2A(1,2)	—	—	—	—	N	OSC1 CLKIN
RB0	6	7	7	N	—	—	—	—	SRI	T1G	CCP1(1) P1A(1) FLT0	—	—	INT IOC	—	Y	—
RB1	7	8	8	Y	AN11	—	CPS11	—	—	—	—	RX(1,4) DT(1,4)	SDA1 SDI1	IOC	—	Y	—
RB2	8	9	9	Y	AN10	—	CPS10	—	—	—	—	RX(1)DT(1) TX(1,4) CK(1,4)	SDA2(2) SDI2(2) SDO1(1,4)	IOC	MDMIN	Y	—
RB3	9	10	10	Y	AN9	—	CPS9	—	—	—	CCP1(1,4) P1A(1,4)	—	—	IOC	MDOUT	Y	—
RB4	10	11	12	Y	AN8	—	CPS8	—	—	—	—	—	SCL1 SCK1	IOC	MDCIN2	Y	—
RB5	11	12	13	Y	AN7	—	CPS7	—	—	—	P1B	TX(1) CK(1)	SCL2(2) $\overline{SCK2}$(2) $\overline{SS1}$(1,4)	IOC	—	Y	—
RB6	12	13	15	Y	AN5	—	CPS5	—	—	T1CKI T1OSI	P1C(1,4) CCP2(1,2,4) P2A(1,2,4)	—	—	IOC	—	Y	ICSPCLK/ ICDCLK
RB7	13	14	16	Y	AN6	—	CPS6	—	—	T1OSO	P1D(1,4) P2B(1,2,4)	—	—	IOC	MDCIN1	Y	ICSPDAT/ ICDDAT
VDD	14	15,16	17,19	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
Vss	5	5,6	3,5	—	—	—	—	—	—	—	—	—	—	—	—	—	Vss

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Functions are only available on the PIC16(L)F1827.
3: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.
4: Default function location.

Table of Contents

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1.0 DEVICE OVERVIEW

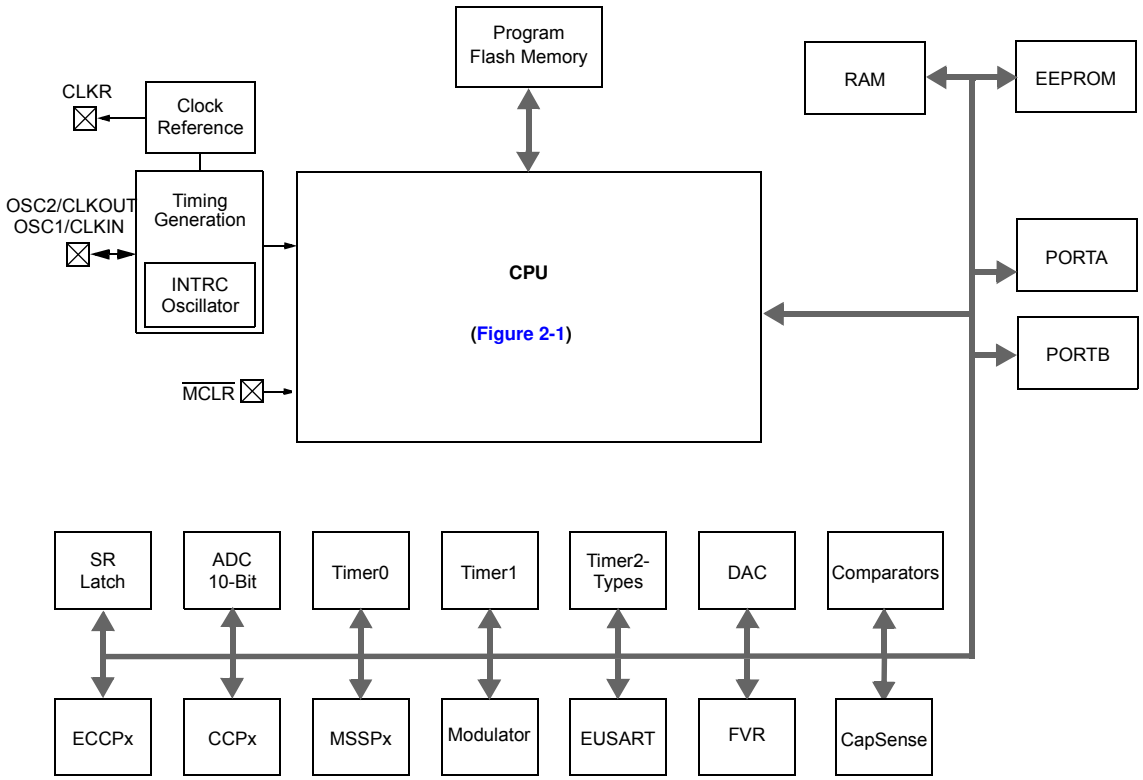
The PIC16(L)F1826/27 are described within this data sheet. They are available in 18/20/28-pin packages. Figure 1-1 shows a block diagram of the PIC16(L)F1826/27 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16F/LF1826	PIC16(L)F1827
ADC		•	•
Capacitive Sensing Module		•	•
Digital-to-Analog Converter (DAC)		•	•
Digital Signal Modulator (DSM)		•	•
EUSART		•	•
Fixed Voltage Reference (FVR)		•	•
Reference Clock Module		•	•
SR Latch		•	•
Capture/Compare/PWM Modules			
	ECCP1	•	•
	ECCP2		•
	CCP3		•
	CCP4		•
Comparators			
	C1	•	•
	C2	•	•
Master Synchronous Serial Ports			
	MSSP1	•	•
	MSSP2		•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	•	•
	Timer4		•
	Timer6		•

FIGURE 1-1: PIC16(L)F1826/27 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.
2: See Table 1-1 for peripherals available on specific devices.

TABLE 1-2: PIC16(L)F1826/27 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C12IN0-/ SDO2(2)	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	CPS0	AN	—	Capacitive sensing input 0.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	SDO2	—	CMOS	SPI data output.
RA1/AN1/CPS1/C12IN1-/$\overline{SS2}$(2)	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	CPS1	AN	—	Capacitive sensing input 1.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
	$\overline{SS2}$	ST	—	Slave Select input 2.
RA2/AN2/CPS2/C12IN2-/ C12IN+/VREF-/DACOUT	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	CPS2	AN	—	Capacitive sensing input 2.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	C12IN+	AN	—	Comparator C1 or C2 positive input.
	VREF-	AN	—	A/D Negative Voltage Reference input.
	DACOUT	—	AN	Voltage Reference output.
RA3/AN3/CPS3/C12IN3-/C1IN+/ VREF+/C1OUT/CCP3(2)/SRQ	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	CPS3	AN	—	Capacitive sensing input 3.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF+	AN	—	A/D Voltage Reference input.
	C1OUT	—	CMOS	Comparator C1 output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SRQ	—	CMOS	SR latch non-inverting output.
RA4/AN4/CPS4/C2OUT/T0CKI/ CCP4(2)/SRNQ	RA4	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS4	AN	—	Capacitive sensing input 4.
	C2OUT	—	CMOS	Comparator C2 output.
	T0CKI	ST	—	Timer0 clock input.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
	SRNQ	—	CMOS	SR latch inverting output.
RA5/$\overline{MCLR}$/VPP/$\overline{SS1}$(1,2)	RA5	TTL	CMOS	General purpose I/O.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
	$\overline{SS1}$	ST	—	Slave Select input 1.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Functions are only available on the PIC16(L)F1827.
3: Default function location.

TABLE 1-2: PIC16(L)F1826/27 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA6/OSC2/CLKOUT/CLKR/ P1D(1)/P2B(1,2)/SDO1(1)	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	CLKR	—	CMOS	Clock Reference Output.
	P1D	—	CMOS	PWM output.
	P2B	—	CMOS	PWM output.
	SDO1	—	CMOS	SPI data output 1.
RA7/OSC1/CLKIN/P1C(1)/ CCP2(1,2)/P2A(1,2)	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	P1C	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P2A	—	CMOS	PWM output.
RB0/T1G/CCP1(1)/P1A(1)/INT/ SRI/FLT0	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	T1G	ST	—	Timer1 Gate input.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	P1A	—	CMOS	PWM output.
	INT	ST	—	External interrupt.
	SRI	ST	—	SR latch input.
	FLT0	ST	—	ECCP Auto-Shutdown Fault input.
RB1/AN11/CPS11/RX(1,3)/ DT(1,3)/SDA1/SDI1	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN11	AN	—	A/D Channel 11 input.
	CPS11	AN	—	Capacitive sensing input 11.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	SDA1	I2C™	OD	I2C™ data input/output 1.
	SDI1	CMOS	—	SPI data input 1.
RB2/AN10/CPS10/MDMIN/ TX(1,3)/CK(1,3)/RX(1)/DT(1)/ SDA2(2)/SDI2(2)/SDO1(1,3)	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	CPS10	AN	—	Capacitive sensing input 10.
	MDMIN	—	CMOS	Modulator source input.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	SDA2	I2C™	OD	I2C™ data input/output 2.
	SDI2	ST	—	SPI data input 2.
	SDO1	—	CMOS	SPI data output 1.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I2C™ = Schmitt Trigger input with I2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Functions are only available on the PIC16(L)F1827.
3: Default function location.

TABLE 1-2: PIC16(L)F1826/27 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3/AN9/CPS9/MDOUT/ CCP1(1,3)/P1A(1,3)	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9 input.
	CPS9	AN	—	Capacitive sensing input 9.
	MDOUT	—	CMOS	Modulator output.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	P1A	—	CMOS	PWM output.
RB4/AN8/CPS8/SCL1/SCK1/ MDCIN2	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8 input.
	CPS8	AN	—	Capacitive sensing input 8.
	SCL1	I^2C™	OD	I^2C™ clock 1.
	SCK1	ST	CMOS	SPI clock 1.
	MDCIN2	ST	—	Modulator Carrier Input 2.
RB5/AN7/CPS7/P1B/TX(1)/CK(1)/ SCL2(2)/SCK2(2)/$\overline{SS1}$(1,3)	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN7	AN	—	A/D Channel 7 input.
	CPS7	AN	—	Capacitive sensing input 7.
	P1B	—	CMOS	PWM output.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	SCL2	I^2C™	OD	I^2C™ clock 2.
	SCK2	ST	CMOS	SPI clock 2.
	$\overline{SS1}$	ST	—	Slave Select input 1.
RB6/AN5/CPS5/T1CKI/T1OSI/ P1C(1,3)/CCP2(1,2,3)/P2A(1,2,3)/ ICSPCLK	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN5	AN	—	A/D Channel 5 input.
	CPS5	AN	—	Capacitive sensing input 5.
	T1CKI	ST	—	Timer1 clock input.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	P1C	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P2A	—	CMOS	PWM output.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/AN6/CPS6/T1OSO/ P1D(1,3)/P2B(1,2,3)/MDCIN1/ ICSPDAT	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN6	AN	—	A/D Channel 6 input.
	CPS6	AN	—	Capacitive sensing input 6.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	P1D	—	CMOS	PWM output.
	P2B	—	CMOS	PWM output.
	MDCIN1	ST	—	Modulator Carrier Input 1.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Functions are only available on the PIC16(L)F1827.
3: Default function location.

TABLE 1-2: PIC16(L)F1826/27 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Functions are only available on the PIC16(L)F1827.
3: Default function location.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 8.5 "Automatic Context Saving"**, for more information.

2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See section **Section 3.4 "Stack"** for more details.

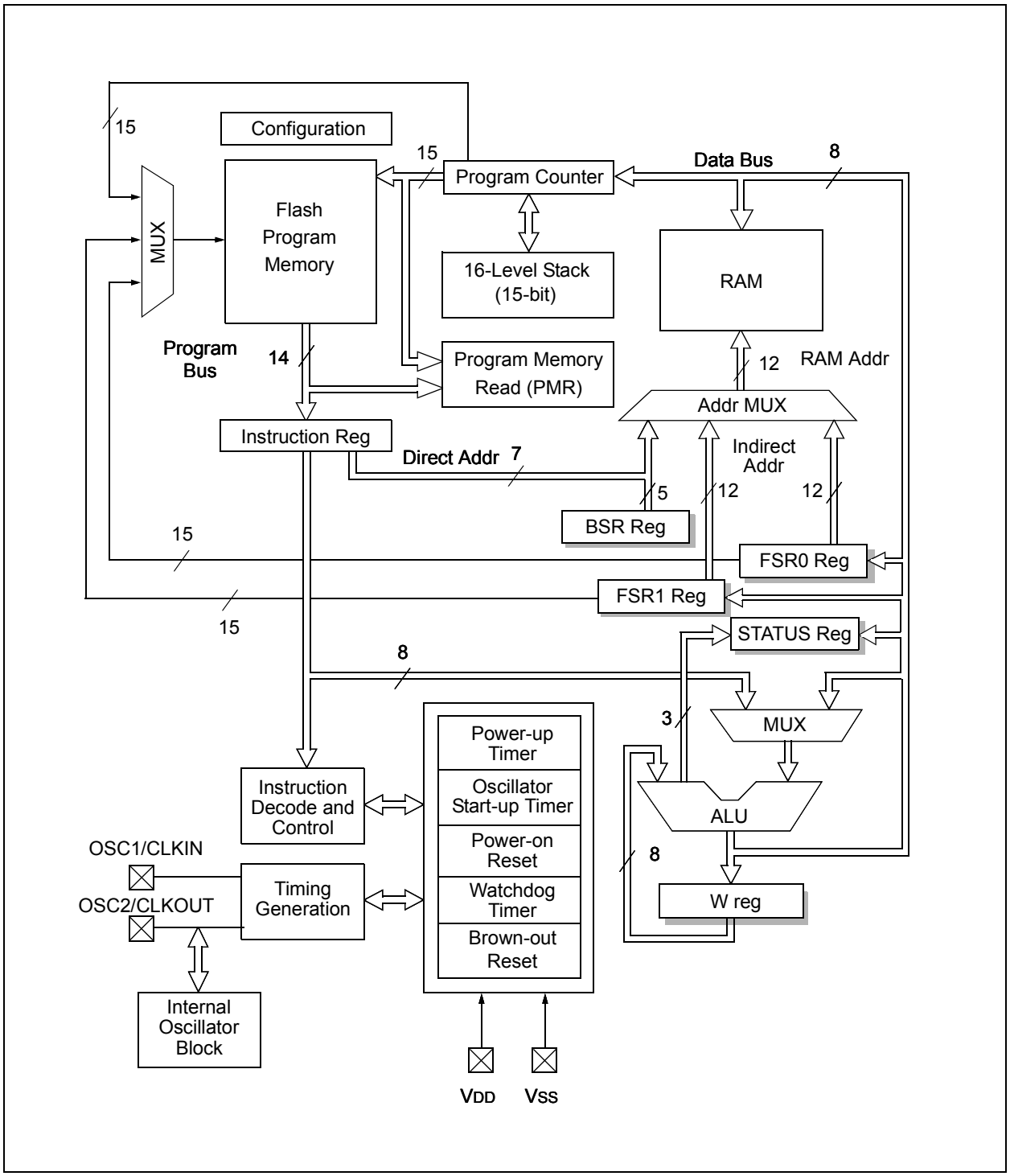
2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.4 "Stack"**for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 29.0 "Instruction Set Summary"** for more details.

FIGURE 2-1: CORE BLOCK DIAGRAM



3.0 MEMORY ORGANIZATION

There are three types of memory in PIC16(L)F1826/27: Data Memory, Program Memory and Data EEPROM Memory(1).

- Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
  - Device Memory Maps
  - Special Function Registers Summary
- Data EEPROM memory(1)

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in **Section 11.0 "Data EEPROM and Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1826/27 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1 and 3-2).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
PIC16(L)F1826	2,048	07FFh
PIC16(L)F1827	4,096	0FFFh

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1826

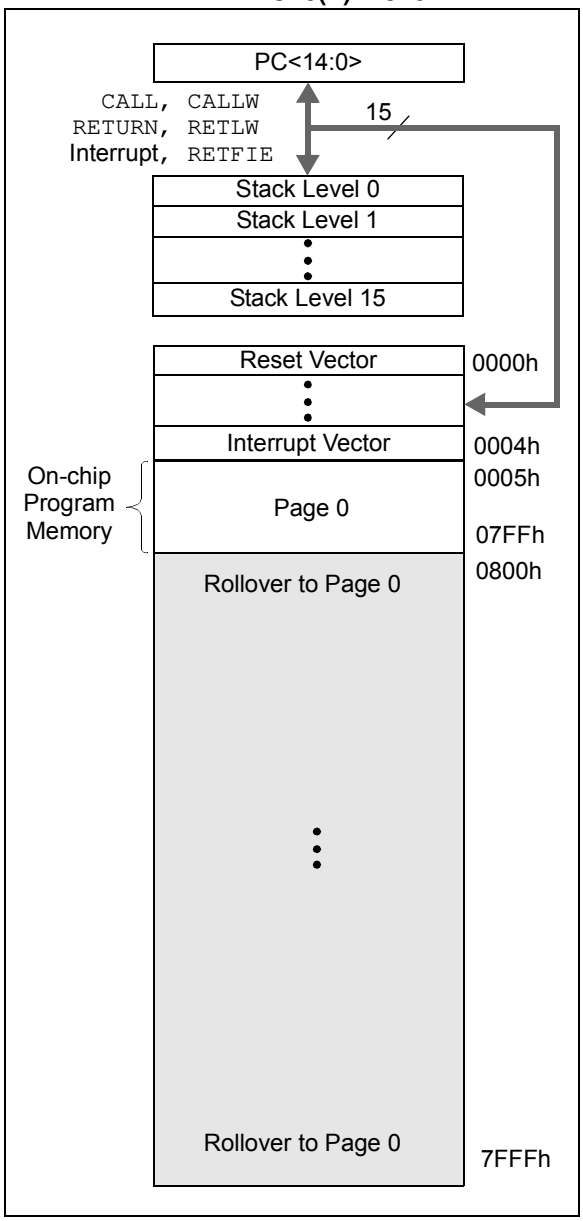
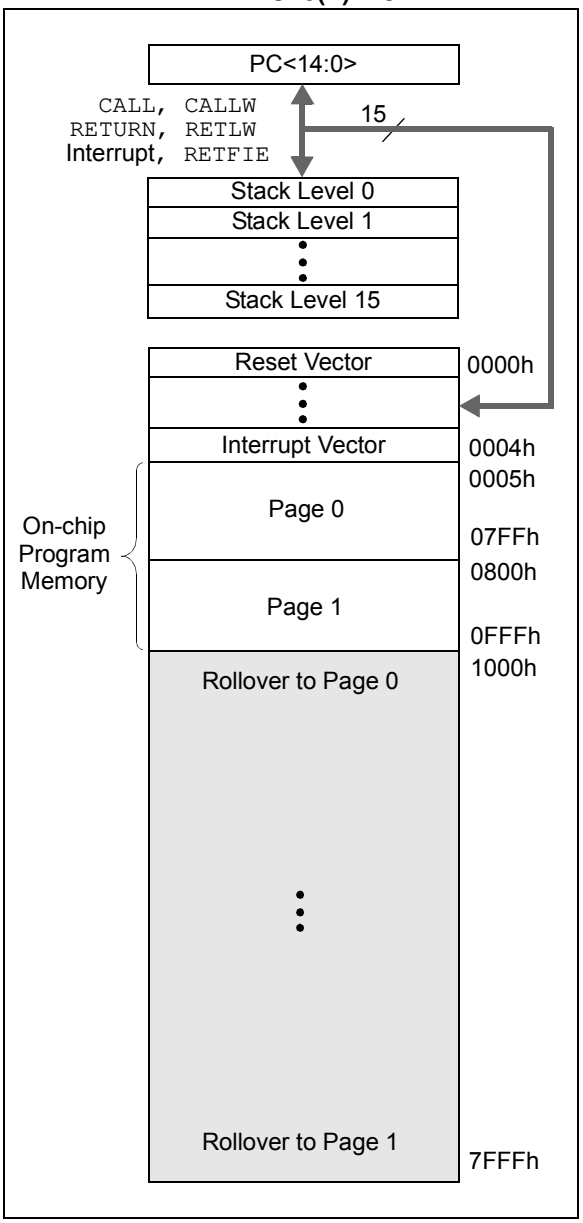


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1827



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW 0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.5 "Indirect Addressing"** for more information.

Data Memory uses a 12-bit address. The upper 7-bit of the address define the Bank address and the lower 5-bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For for detailed information, see Table 3-5.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 29.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

3.2.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.2.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

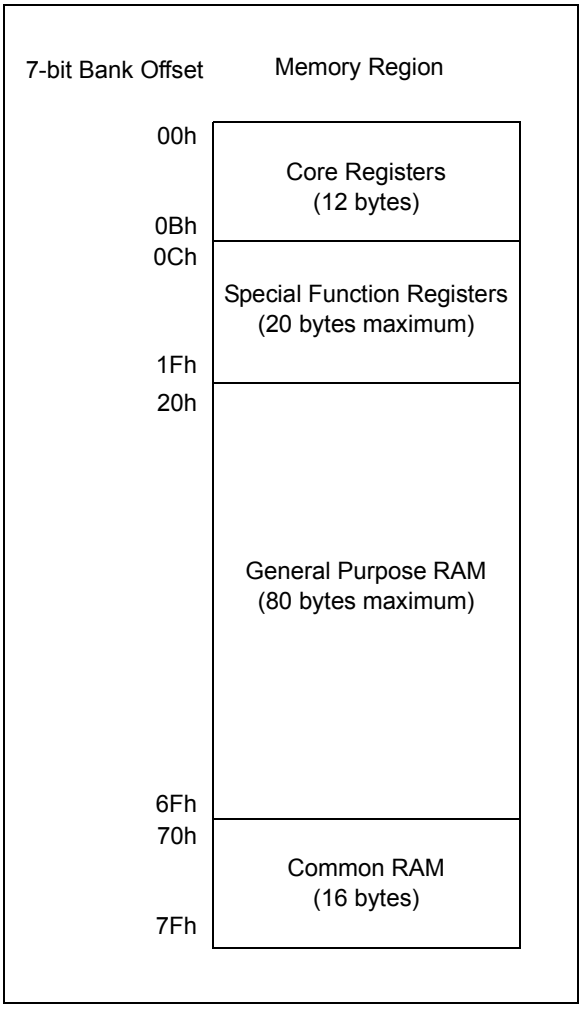
3.2.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.5.2 "Linear Data Memory"** for more information.

3.2.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.2.5 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Table 3-3 and Table 3-4.

TABLE 3-3: PIC16(L)F1826/27 MEMORY MAP

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	—	30Ch	—	38Ch	—
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	—	30Dh	—	38Dh	—
00Eh	—	08Eh	—	10Eh	—	18Eh	—	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	—	090h	—	110h	—	190h	—	210h	—	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	EEADRL	211h	SSP1BUF	291h	CCPR1L	311h	CCPR3L(1)	391h	—
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	EEADRH	212h	SSP1ADD	292h	CCPR1H	312h	CCPR3H(1)	392h	—
013h	PIR3(1)	093h	PIE3(1)	113h	CM2CON0	193h	EEDATL	213h	SSP1MASK	293h	CCP1CON	313h	CCP3CON(1)	393h	—
014h	PIR4(1)	094h	PIE4(1)	114h	CM2CON1	194h	EEDATH	214h	SSP1STAT	294h	PWM1CON	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION	115h	CMOUT	195h	EECON1	215h	SSP1CON	295h	CCP1AS	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	SSP1CON2	296h	PSTR1CON	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	SSP1CON3	297h	—	317h	—	397h	—
018h	T1CON	098h	OSCTUNE	118h	DACCON0	198h	—	218h	—	298h	CCPR2L(1)	318h	CCPR4L(1)	398h	—
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	RCREG	219h	SSP2BUF(1)	299h	CCPR2H(1)	319h	CCPR4H(1)	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	SRCON0	19Ah	TXREG	21Ah	SSP2ADD(1)	29Ah	CCP2CON(1)	31Ah	CCP4CON(1)	39Ah	CLKRCON
01Bh	PR2	09Bh	ADRESL	11Bh	SRCON1	19Bh	SPBRGL	21Bh	SSP2MASK(1)	29Bh	PWM2CON(1)	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SPBRGH	21Ch	SSP2STAT(1)	29Ch	CCP2AS(1)	31Ch	—	39Ch	MDCON
01Dh	—	09Dh	ADCON0	11Dh	APFCON0	19Dh	RCSTA	21Dh	SSP2CON(1)	29Dh	PSTR2CON(1)	31Dh	—	39Dh	MDSRC
01Eh	CPSCON0	09Eh	ADCON1	11Eh	APFCON1	19Eh	TXSTA	21Eh	SSP2CON2(1)	29Eh	CCPTMRS(1)	31Eh	—	39Eh	MDCARL
01Fh	CPSCON1	09Fh	—	11Fh	—	19Fh	BAUDCON	21Fh	SSP2CON3(1)	29Fh	—	31Fh	—	39Fh	MDCARH
020h	General Purpose Register 96 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes(1)	220h	General Purpose Register 48 Bytes(1)	2A0h	Unimplemented Read as '0'	320h	Unimplemented Read as '0'	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh	Unimplemented Read as '0'	2EFh		36Fh		3EFh	
070h		0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'

Note 1: Available only on PIC16(L)F1827.

TABLE 3-3: PIC16(L)F1826/27 MEMORY MAP (CONTINUED)

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	—	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	—	48Dh	—	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	—	490h	—	510h	—	590h	—	610h	—	690h	—	710h	—	790h	—
411h	—	491h	—	511h	—	591h	—	611h	—	691h	—	711h	—	791h	—
412h	—	492h	—	512h	—	592h	—	612h	—	692h	—	712h	—	792h	—
413h	—	493h	—	513h	—	593h	—	613h	—	693h	—	713h	—	793h	—
414h	—	494h	—	514h	—	594h	—	614h	—	694h	—	714h	—	794h	—
415h	TMR4(1)	495h	—	515h	—	595h	—	615h	—	695h	—	715h	—	795h	—
416h	PR4(1)	496h	—	516h	—	596h	—	616h	—	696h	—	716h	—	796h	—
417h	T4CON(1)	497h	—	517h	—	597h	—	617h	—	697h	—	717h	—	797h	—
418h	—	498h	—	518h	—	598h	—	618h	—	698h	—	718h	—	798h	—
419h	—	499h	—	519h	—	599h	—	619h	—	699h	—	719h	—	799h	—
41Ah	—	49Ah	—	51Ah	—	59Ah	—	61Ah	—	69Ah	—	71Ah	—	79Ah	—
41Bh	—	49Bh	—	51Bh	—	59Bh	—	61Bh	—	69Bh	—	71Bh	—	79Bh	—
41Ch	TMR6(1)	49Ch	—	51Ch	—	59Ch	—	61Ch	—	69Ch	—	71Ch	—	79Ch	—
41Dh	PR6(1)	49Dh	—	51Dh	—	59Dh	—	61Dh	—	69Dh	—	71Dh	—	79Dh	—
41Eh	T6CON(1)	49Eh	—	51Eh	—	59Eh	—	61Eh	—	69Eh	—	71Eh	—	79Eh	—
41Fh	—	49Fh	—	51Fh	—	59Fh	—	61Fh	—	69Fh	—	71Fh	—	79Fh	—
420h	Unimplemented Read as '0'	4A0h	Unimplemented Read as '0'	520h	Unimplemented Read as '0'	5A0h	Unimplemented Read as '0'	620h	Unimplemented Read as '0'	6A0h	Unimplemented Read as '0'	720h	Unimplemented Read as '0'	7A0h	Unimplemented Read as '0'
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
470h	Accesses 70h – 7Fh	4F0h	Accesses 70h – 7Fh	570h	Accesses 70h – 7Fh	5F0h	Accesses 70h – 7Fh	670h	Accesses 70h – 7Fh	6F0h	Accesses 70h – 7Fh	770h	Accesses 70h – 7Fh	7F0h	Accesses 70h – 7Fh
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

Legend: = Unimplemented data memory locations, read as '0'

TABLE 3-3: PIC16(L)F1826/27 MEMORY MAP (CONTINUED)

BANK16	BANK17	BANK18	BANK19	BANK20	BANK21	BANK22	BANK23
800h	880h	900h	980h	A00h	A80h	B00h	B80h
Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)
80Bh	88Bh	90Bh	98Bh	A0Bh	A8Bh	B0Bh	B8Bh
80Ch	88Ch	90Ch	98Ch	A0Ch	A8Ch	B0Ch	B8Ch
Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'
86Fh	8EFh	96Fh	9EFh	A6Fh	AEFh	B6Fh	BEFh
870h	8F0h	970h	9F0h	A70h	AF0h	B70h	BF0h
Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)
87Fh	8FFh	97Fh	9FFh	A7Fh	AFFh	B7Fh	BFFh

BANK 24	BANK 25	BANK 26	BANK 27	BANK 28	BANK 29	BANK 30	BANK 31
C00h	C80h	D00h	D80h	E00h	E80h	F00h	F80h
Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)	Core Registers (Table 3-2)
C0Bh	C8Bh	D0Bh	D8Bh	E0Bh	E8Bh	F0Bh	F8Bh
C0Ch	C8Ch	D0Ch	D8Ch	E0Ch	E8Ch	F0Ch	F8Ch
Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'
C6Fh	CEFh	D6Fh	DEFh	E6Fh	EEFh	F6Fh	F9Fh
							FA0h
							See Table 3-4 for more information
							FEFh
C70h	CF0h	D70h	DF0h	E70h	EF0h	F70h	FF0h
Accesses 70h – 7Fh	Accesses 70h – 7Fh	Accesses 70h – 7Fh	Accesses 70h – 7Fh	Accesses 70h – 7Fh	Accesses 70h – 7Fh	Common RAM (Accesses 70h – 7Fh)	Common RAM (Accesses 70h – 7Fh)
C7Fh	CFFh	D7Fh	DFFh	E7Fh	EFFh	F7Fh	FFFh

Legend: = Unimplemented data memory locations, read as '0'