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PIC16(L)F18324/18344

Full-Featured, Low Pin Count Microcontrollers with XLP

Description

PIC16(L)F18324/18344 microcontrollers feature Analog, Core Independent Peripherals and Communication Peripherals, combined with eXtreme Low Power (XLP) for a wide range of general purpose and low-power applications. The Peripheral Pin Select (PPS) functionality enables pin mapping when using the digital peripherals (CLC, CWG, CCP, PWM and communications) to add flexibility to the application design.

Core Features

- C Compiler Optimized RISC Architecture
- Only 48 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- Up to Three 16-Bit Timers
- Low-Current Power-on Reset (POR)
- Power-up Timer (PWRTE)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Extended Watchdog Timer (WDT) with Dedicated On-Chip Oscillator for Reliable Operation
- Programmable Code Protection

Memory

- 7 Kbytes Program Flash Memory
- 512 Bytes Data SRAM Memory
- 256B of EEPROM
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF18324/18344)
  - 2.3V to 5.5V (PIC16F18324/18344)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features

- Sleep mode: 40 nA @ 1.8V, typical
- Watchdog Timer: 250 nA @ 1.8V, typical
- Secondary Oscillator: 300 nA @ 32 kHz
- Operating Current:
  - 8 μA @ 32 kHz, 1.8V, typical
  - 37 μA/MHz @ 1.8V, typical

Power-Saving Functionality

- IDLE mode: ability to put the CPU core to Sleep while internal peripherals continue operating from the system clock
- DOZE mode: ability to run the CPU core slower than the system clock used by the internal peripherals
- SLEEP mode: Lowest Power Consumption
- Peripheral Module Disable (PMD): peripheral power disable hardware module to minimize power consumption of unused peripherals

Digital Peripherals

- Configurable Logic Cell (CLC):
  - Four CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Two CWGs
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules
  - Four CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Pulse-Width Modulators (PWM):
  - Two 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock: 0 Hz < F_{NCO} < 32 MHz
  - Resolution: $F_{NCO}/2^{20}$
- Serial Communications:
  - EUSART
    - RS-232, RS-485, LIN compatible
    - Auto-Baud Detect, auto-wake-up on start
  - Master Synchronous Serial Port (MSSP)
    - SPI
    - I^2C, SMBus, PMBus™ compatible
- Data Signal Modulator (DSM):
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms

- Up to 18 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable
- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Timer modules:
  - Timer0:
    - 8/16-bit timer/counter
    - Synchronous or asynchronous operation
    - Programmable prescaler/postscaler
    - Time base for capture/compare function
  - Timer1/3/5 with gate control:
    - 16-bit timer/counter
    - Programmable internal or external clock sources
    - Multiple gate sources
    - Multiple gate modes
    - Time base for capture/compare function
  - Timer2/4/6:
    - 8-bit timers
    - Programmable prescaler/postscaler
    - Time base for PWM function

Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - 17 external channels
  - Conversion available during Sleep
- Comparator:
  - Two comparators
  - Fixed Voltage Reference at non-inverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Software-selectable frequency range up to 32 MHz
  - ±2% at nominal 4 MHz calibration point
- 4x PLL with External Sources
- Low-Power Internal 31 kHz Oscillator (LFINTOSC)
- External Low-power 32 kHz Crystal Oscillator (SOSC)
- External Oscillator Block with:
  - Three Crystal/Resonator modes up to 20 MHz
  - Three External Clock modes up to 20 MHz
  - Fail-Safe Clock Monitor:
    - Detects clock source failure
  - Oscillator Start-up Timer (OST)
    - Ensures stability of crystal oscillator sources

PIC16(L)F183XX Family Types

Device	Data Sheet Index	Program Flash Memory (Words)	Program Flash Memory (Kbytes)	Data Memory (EEPROM)(bytes)	Data SRAM (bytes)	I/Os(2)	10-bit ADC (ch)	5-bit DAC	Comparators	CWG	Clock Ref	Timers (8/16-bit)	CCP	PWM	NCO	EUSART	I²C/SPI	CLC	DSM	PPS	XLP	PMD	Idle and Doze	Debug(1)
PIC16(L)F18313	(1)	2048	3.5	256	256	6	9	1	1	1	Y	2/1	2	2	1	1	1/1	2	1	Y	Y	Y	Y	I
PIC16(L)F18323	(1)	2048	3.5	256	256	12	15	1	2	1	Y	2/1	2	2	1	1	1/1	2	1	Y	Y	Y	Y	I
PIC16(L)F18324	(2)	4096	7	256	512	12	15	1	2	2	Y	4/3	4	2	1	1	1/1	4	1	Y	Y	Y	Y	I
PIC16(L)F18325	(3)	8192	14	256	1024	12	15	1	2	2	Y	4/3	4	2	1	1	2/2	4	1	Y	Y	Y	Y	I
PIC16(L)F18326	(4)	16384	28	256	2048	12	15	1	2	2	Y	4/3	4	2	1	1	2/2	4	1	Y	Y	Y	Y	I
PIC16(L)F18344	(2)	4096	7	256	512	18	21	1	2	2	Y	4/3	4	2	1	1	1/1	4	1	Y	Y	Y	Y	I
PIC16(L)F18345	(3)	8192	14	256	1024	18	21	1	2	2	Y	4/3	4	2	1	1	2/2	4	1	Y	Y	Y	Y	I
PIC16(L)F18346	(4)	16384	28	256	2048	18	21	1	2	2	Y	4/3	4	2	1	1	2/2	4	1	Y	Y	Y	Y	I

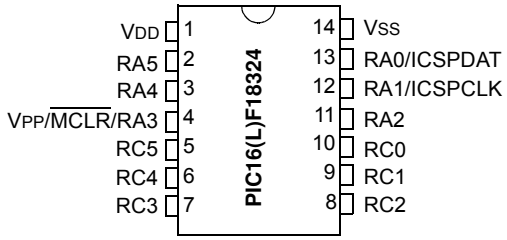
Note 1: Debugging Methods: (I) – Integrated on Chip
2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)
1: DS40001799 PIC16(L)F18313/18323 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP
2: DS40001800 PIC16(L)F18324/18344 Data Sheet, Full Featured, Low Pin Count Microcontrollers with XLP
3: DS40001795 PIC16(L)F18325/18345 Data Sheet, Full Featured, Low Pin Count Microcontrollers with XLP
4: DS40001839 PIC16(L)F18326/18346 Data Sheet, Full Featured, Low Pin Count Microcontrollers with XLP

Note: For other small form-factor package availability and marking information, visit **http://www.microchip.com/packaging** or contact your local sales office.

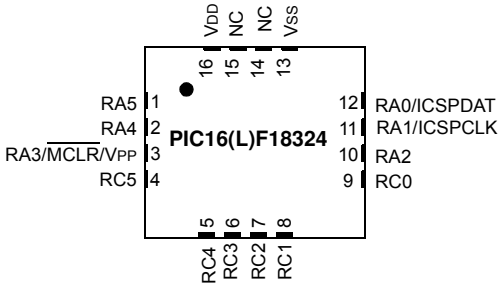
PIN DIAGRAMS

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP



Note: See Table 1 for location of all peripheral functions.

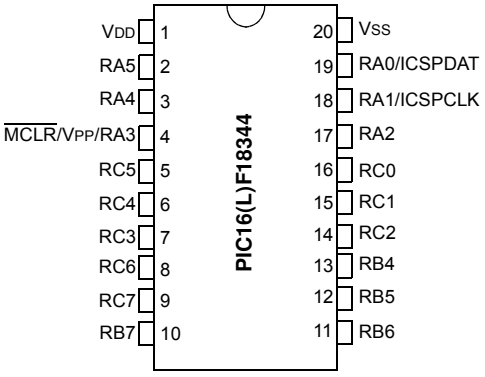
FIGURE 2: 16-PIN UQFN (4x4)



Note 1: See Table 1 for location of all peripheral functions.

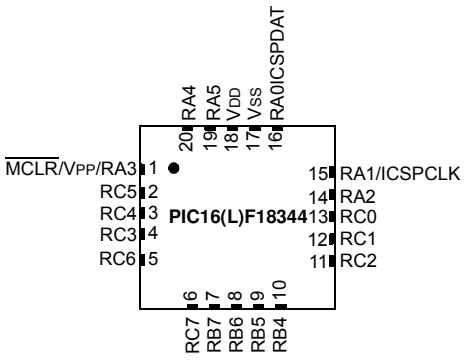
2: It is recommended that the exposed bottom pad be connected to VSS, but must not be the main VSS connection to the device.

FIGURE 3: 20-PIN PDIP, SOIC, SSOP



Note: See Table 2 for location of all peripheral functions.

FIGURE 4: 20-PIN UQFN (4x4)



Note 1: See Table 2 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS, but must not be the main VSS connection to the device.

PIN ALLOCATION TABLES

TABLE 1: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324)

I/O(2)	14-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOC	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1IN(1) CWG2IN(1)	—	—	—	—	INT(1) IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) SOSCIN SOSCI	—	—	—	—	—	CLCIN3(1)	—	IOC	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI(1)	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOC	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4(1)	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOC	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	T5G(1)	CCP2(1)	—	—	$\overline{\text{SS1}}$(1)	—	CLCIN0(1)	—	IOC	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	—	—	CLCIN1(1)	—	IOC	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2(1)	T3CKI(1)	CCP1(1)	—	—	—	RX(1)	—	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ ST as selected by the INLVL register.

TABLE 1: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324) (CONTINUED)

I/O[2]	14-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT[2]	—	—	—	—	C1OUT	NCO1	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA1[3]	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL1[3]	DT	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO1	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK1	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16(L)F18344)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	ICDDAT ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOC	Y	ICDCLK ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1IN(1) CWG2IN(1)	—	—	CLCIN0(1)	—	IOC INT(1)	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$ VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G(1) T3G(1) T5G(1) SOSCO	CCP4(1)	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI(1) T3CKI(1) T5CKI(1) SOSCIN SOSCI	—	—	—	—	—	—	—	IOC	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOC	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	—	RX(1)	CLCIN3(1)	—	IOC	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOC	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	—	CCP2(1)	—	—	—	—	CLCIN1(1)	—	IOC	Y	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16(L)F18344) (CONTINUED)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2(1)	—	CCP1(1)	—	—	—	—	—	—	IOC	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	$\overline{SS1}$(1)	—	—	—	IOC	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	NCO1	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1	DT	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK1	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1(3)	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1(3)	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

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1.0 DEVICE OVERVIEW

The PIC16(L)F18324/18344 devices are described within this data sheet. PIC16(L)F18324 is available in 14-pin PDIP, SOIC, TSSOP and 16-pin UQFN packages. PIC16(L)F18344 is available in 20-pin PDIP, SOIC, SSOP and UQFN packages. See **Section 38.0 "Packaging Information"** for further packaging information. Figure 1-1 shows a block diagram of the PIC16(L)F18324/18344 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

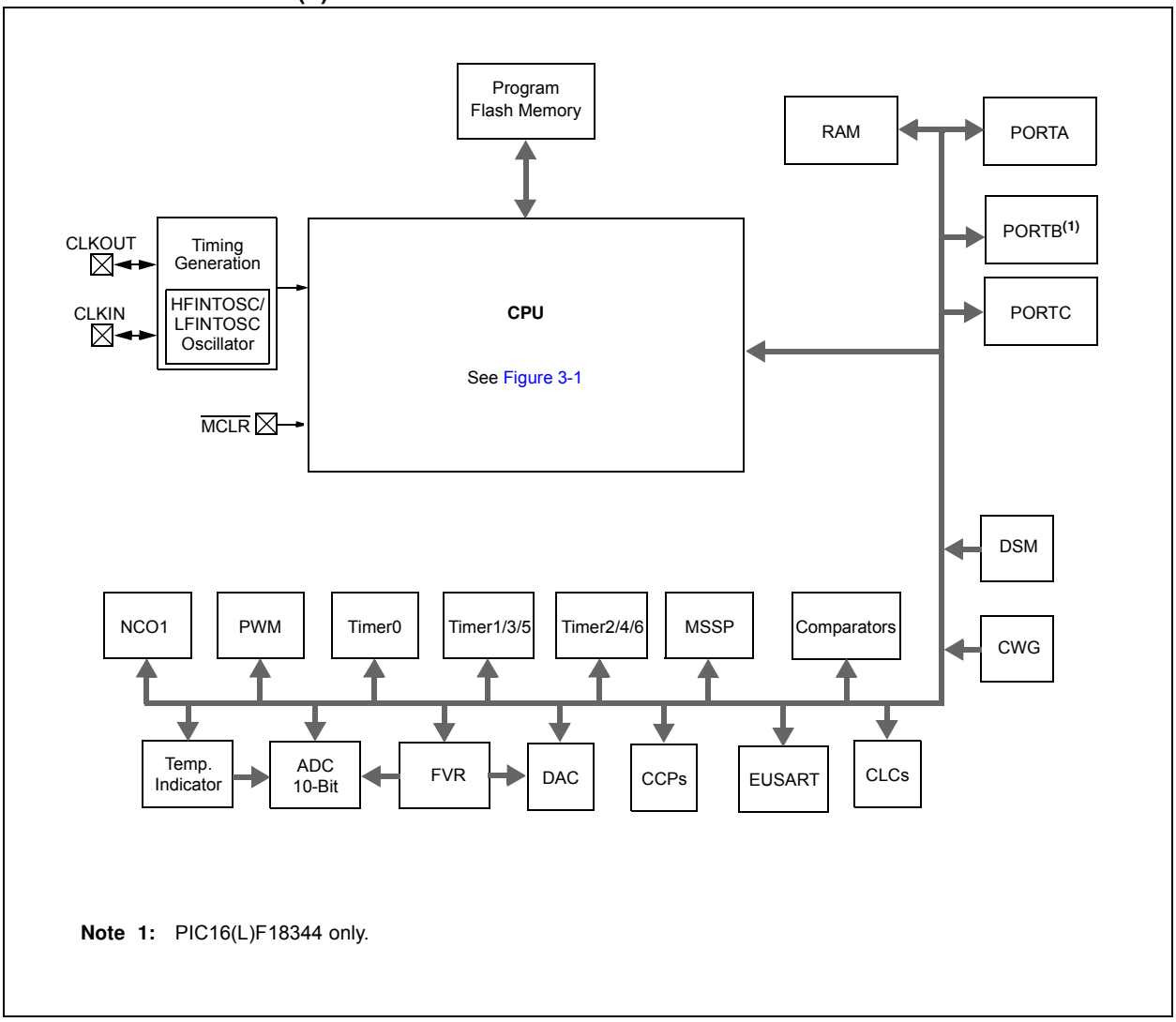
TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F18324	PIC16(L)F18344
Analog-to-Digital Converter (ADC)		•	•
Temperature Indicator		•	•
Digital-to-Analog Converter (DAC)			
	DAC1	•	•
Fixed Voltage Reference (FVR)			
	ADCFVR	•	•
	CDAFVR	•	•
Digital Signal Modulator (DSM)			
	DSM1	•	•
Numerically Controlled Oscillator (NCO)			
	NCO1	•	•
Capture/Compare/PWM Modules (CCP)			
	CCP1	•	•
	CCP2	•	•
	CCP3	•	•
	CCP4	•	•
Comparators			
	C1	•	•
	C2	•	•
Complementary Waveform Generator (CWG)			
	CWG1	•	•
	CWG2	•	•
Configurable Logic Cell (CLC)			
	CLC1	•	•
	CLC2	•	•
	CLC3	•	•
	CLC4	•	•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART)			
	EUSART1	•	•

TABLE 1-1: DEVICE PERIPHERAL SUMMARY (CONTINUED)

Peripheral		PIC16(L)F18324	PIC16(L)F18344
Master Synchronous Serial Port (MSSP)			
	MSSP1	•	•
Pulse-Width Modulator (PWM)			
	PWM5	•	•
	PWM6	•	•
Timers (TMR)			
	TMR0	•	•
	TMR1	•	•
	TMR2	•	•
	TMR3	•	•
	TMR4	•	•
	TMR5	•	•
	TMR6	•	•

FIGURE 1-1: PIC16(L)F18324/18344 BLOCK DIAGRAM



Note 1: PIC16(L)F18344 only.

TABLE 1-2: PIC16(L)F18324 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0+/DAC1OUT/ ICDDAT/ICSPDAT	RA0	TTL/ST	CMOS	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	ICDDAT	TTL/ST	CMOS	In-Circuit Debug Data I/O.
	ICSPDAT	TTL/ST	CMOS	ICSP™ Data I/O.
RA1/ANA1/VREF+/C1IN0-/ C2IN0-/DAC1REF+/ ICDCLK/ ICSPCLK	RA1	TTL/ST	CMOS	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	VREF+	AN	—	ADC positive voltage reference input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	DAC1REF+	—	AN	Digital-to-Analog Converter positive reference input.
	ICDCLK	TTL/ST	CMOS	In-Circuit Debug Clock I/O.
	ICSPCLK	TTL/ST	CMOS	ICSP Clock I/O.
RA2/ANA2/VREF-/ DAC1REF-/ T0CKI(1)/ CCP3(1)/CWG1IN(1)/ CWG2IN(1)/INT(1)	RA2	TTL/ST	CMOS	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	VREF-	AN	—	ADC negative voltage reference input.
	DAC1REF-	—	AN	Digital-to-Analog Converter negative reference input.
	T0CKI	TTL/ST	—	TMR0 Clock input.
	CCP3	TTL/ST	CMOS	Capture/Compare/PWM 3 input.
	CWG1IN	TTL/ST	—	Complementary Waveform Generator 1 input.
	CWG2IN	TTL/ST	—	Complementary Waveform Generator 2 input.
	INT	TTL/ST	—	External interrupt input.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL/ST	CMOS	General purpose I/O.
	$\overline{\text{MCLR}}$	TTL/ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
RA4/ANA4/T1G(1)/ SOSCO/ CLKOUT/OSC2	RA4	TTL/ST	CMOS	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T1G	ST	—	TMR1 gate input.
	SOSCO	—	XTAL	Secondary Oscillator connection.
	CLKOUT	—	CMOS	FOSC/4 output.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
RA5/ANA5/T1CKI(1)/ SOSCIN/ SOSCI/ CLCIN3(1)/CLKIN/ OSC1	RA5	TTL/ST	CMOS	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	T1CKI	TTL/ST	—	TMR1 Clock input.
	SOSCIN	TTL/ST	—	Secondary Oscillator input connection.
	SOSCI	XTAL	—	Secondary Oscillator connection.
	CLCIN3	TTL/ST	—	Configurable Logic Cell 3 input.
	CLKIN	TTL/ST	—	External clock input.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-1.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.
3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F18324 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC0/ANC0/C2IN0+/ T5CKI(1)/ SCK1(1)/ SCL1(1,3)	RC0	TTL/ST	CMOS	General purpose I/O.
	ANC0	AN	—	ADC Channel C0 input.
	C2IN0+	AN	—	Comparator C2 positive input.
	T5CKI	TTL/ST	—	TMR5 Clock input.
	SCK1	TTL/ST	CMOS	SPI Clock 1.
	SCL1	I^2C	OD	I^2C Clock 1.
RC1/ANC1/C1IN1-/C2IN1-/ CCP4(1)/SDI1(1)/ SDA1(1,3)/ CLCIN2(1)	RC1	TTL/ST	CMOS	General purpose I/O.
	ANC1	AN	—	ADC Channel C1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	CCP4	TTL/ST	CMOS	Capture/Compare/PWM 4 input.
	SDI1	TTL/ST	CMOS	SPI Data input 1.
	SDA1	I^2C	OD	I^2C Data 1.
	CLCIN2	TTL/ST	—	Configurable Logic Cell 2 input.
RC2/ANC2/C1IN2-/C2IN2-/ MDCIN1(1)	RC2	TTL/ST	CMOS	General purpose I/O.
	ANC2	AN	—	ADC Channel C2 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	MDCIN1	TTL/ST	—	Modular Carrier input 1.
RC3/ANC3/C1IN3-/C2IN3-/ MDMIN(1)/T5G(1)/ CCP2(1)/ $\overline{SS1}$(1)/CLCIN0(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	ANC3	AN	—	ADC Channel C3 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	MDMIN	TTL/ST	—	Modular Source input.
	T5G	TTL/ST	—	TMR5 gate input.
	CCP2	TTL/ST	CMOS	Capture/Compare/PWM 2 input.
	$\overline{SS1}$	TTL/ST	—	Slave Select 1 input.
	CLCIN0	TTL/ST	—	Configurable Logic Cell 0 input.
RC4/ANC4/T3G(1)/CLCIN1(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
	T3G	TTL/ST	—	TMR3 gate input.
	CLCIN1	TTL/ST	—	Configurable Logic Cell 1 input.
RC5/ANC5/MDCIN2(1)/ T3CKI(1)/CCP1(1)/RX(1)/DT	RC5	TTL/ST	CMOS	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	MDCIN2	TTL/ST	—	Modular Carrier input 2.
	T3CKI	TTL/ST	—	TMR3 Clock input.
	CCP1	TTL/ST	CMOS	Capture/Compare/PWM 1 input.
	RX	TTL/ST	CMOS	EUSART Asynchronous input.
	DT	TTL/ST	CMOS	EUSART Synchronous input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F18324 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1OUT	—	CMOS	Comparator C1 output.
	C2OUT	—	CMOS	Comparator C2 output.
	NCO1	—	CMOS	Numerically Controlled Oscillator output.
	DSM	—	CMOS	Digital Signal Modulator output.
	TMR0	—	CMOS	TMR0 clock output.
	CCP1	—	CMOS	Capture/Compare/PWM 1 output.
	CCP2	—	CMOS	Capture/Compare/PWM 2 output.
	CCP3	—	CMOS	Capture/Compare/PWM 3 output.
	CCP4	—	CMOS	Capture/Compare/PWM 4 output.
	PWM5	—	CMOS	Pulse-Width Modulator 5 output.
	PWM6	—	CMOS	Pulse-Width Modulator 6 output.
	CWG1A	—	CMOS	Complementary Waveform Generator 1 output A.
	CWG2A	—	CMOS	Complementary Waveform Generator 2 output A.
	CWG1B	—	CMOS	Complementary Waveform Generator 1 output B.
	CWG2B	—	CMOS	Complementary Waveform Generator 2 output B.
	CWG1C	—	CMOS	Complementary Waveform Generator 1 output C.
	CWG2C	—	CMOS	Complementary Waveform Generator 2 output C.
	CWG1D	—	CMOS	Complementary Waveform Generator 1 output D.
	CWG2D	—	CMOS	Complementary Waveform Generator 2 output D.
	SDA1(3)	I^2C	OD	I^2C data output.
	SCL1(3)	I^2C	OD	I^2C clock output.
	SDO1	—	CMOS	SPI1 data output.
	SCK1	—	CMOS	SPI1 clock output.
	TX/CK	—	CMOS	Asynchronous TX data/synchronous clock output.
	DT(3)	—	CMOS	EUSART synchronous data output.
	CLC1OUT	—	CMOS	Configurable Logic Cell 1 source output.
	CLC2OUT	—	CMOS	Configurable Logic Cell 2 source output.
	CLC3OUT	—	CMOS	Configurable Logic Cell 3 source output.
	CLC4OUT	—	CMOS	Configurable Logic Cell 4 source output.
	CLKR	—	CMOS	Clock Reference output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F18344 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0+/DAC1OUT/ ICDDAT/ICSPDAT	RA0	TTL/ST	CMOS	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	ICDDAT	TTL/ST	CMOS	In-Circuit Debug Data I/O.
	ICSPDAT	TTL/ST	CMOS	ICSP™ Data I/O.
RA1/ANA1/VREF+/C1IN0-/ C2IN0-/ DAC1REF+/ICDCLK/ ICSPCLK	RA1	TTL/ST	CMOS	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	VREF+	AN	—	ADC positive voltage reference input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	DAC1REF+	AN	—	Digital-to-Analog Converter positive reference input.
	ICDCLK	TTL/ST	CMOS	In-Circuit Debug Clock I/O.
	ICSPCLK	TTL/ST	CMOS	ICSP Clock I/O.
RA2/ANA2/VREF-/ DAC1REF-/ T0CKI(1)/ CCP3(1)/CWG1IN(1)/ CWG2IN(1)/CLCIN0(1)/ INT(1)	RA2	TTL/ST	CMOS	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	VREF-	AN	—	ADC negative voltage reference input.
	DAC1REF-	AN	—	Digital-to-Analog Converter negative reference input.
	T0CKI	TTL/ST	—	TMR0 Clock input.
	CCP3	TTL/ST	CMOS	Capture/Compare/PWM 3 input.
	CWG1IN	TTL/ST	—	Complementary Waveform Generator 1 input.
	CWG2IN	TTL/ST	—	Complementary Waveform Generator 2 input.
	CLCIN0	TTL/ST	—	Configurable Logic Cell 0 input.
	INT	TTL/ST	—	External interrupt input.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL/ST	CMOS	General purpose I/O.
	$\overline{\text{MCLR}}$	TTL/ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
RA4/ANA4/T1G(1)/T3G(1)/ T5G(1)/SOSCO/CCP4(1)/ CLKOUT/OSC2	RA4	TTL/ST	CMOS	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T1G	TTL/ST	—	TMR1 gate input.
	T3G	TTL/ST	—	TMR3 gate input.
	T5G	TTL/ST	—	TMR5 gate input.
	SOSCO	—	XTAL	Secondary Oscillator connection.
	CCP4	TTL/ST	CMOS	Capture/Compare/PWM 4 input.
	CLKOUT	—	CMOS	FOSC/4 output.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-2.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F18344 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/ANA5/T1CKI(1)/ T3CKI(1)/ T5CKI(1)/ SOSCIN/SOSCI/ CLKIN/OSC1	RA5	TTL/ST	CMOS	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	T1CKI	TTL/ST	—	TMR1 Clock input.
	T3CKI	TTL/ST	—	TMR3 Clock input.
	T5CKI	TTL/ST	—	TMR5 Clock input.
	SOSCIN	TTL/ST	—	Secondary Oscillator input connection.
	SOSCI	XTAL	—	Secondary Oscillator connection.
	CLKIN	TTL/ST	—	External clock input.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
RB4/ANB4/SDI1(1)/SDA1(1,3)/ CLCIN2(1)	RB4	TTL/ST	CMOS	General purpose I/O.
	ANB4	AN	—	ADC Channel B4 input.
	SDI1	TTL/ST	CMOS	SPI Data input 1.
	SDA1	I^2C	OD	I^2C Data 1.
	CLCIN2	TTL/ST	—	Configurable Logic Cell 2 input.
RB5/ANB5/RX(1)/CLCIN3(1)/DT	RB5	TTL/ST	CMOS	General purpose I/O.
	ANB5	AN	—	ADC Channel B5 input.
	RX	TTL/ST	CMOS	EUSART Asynchronous input.
	CLCIN3	TTL/ST	—	Configurable Logic Cell 3 input.
	DT	TTL/ST	CMOS	EUSART Synchronous input.
RB6/ANB6/SCK1(1)/ SCL1(1,3)	RB6	TTL/ST	CMOS	General purpose I/O.
	ANB6	AN	—	ADC Channel B6 input.
	SCK1	TTL/ST	CMOS	SPI Clock 1.
	SCL1	I^2C	OD	I^2C Clock 1.
RB7/ANB7	RB7	TTL/ST	CMOS	General purpose I/O.
	ANB7	AN	—	ADC Channel B7 input.
RC0/ANC0/C2IN0+	RC0	TTL/ST	CMOS	General purpose I/O.
	ANC0	AN	—	ADC Channel C0 input.
	C2IN0+	AN	—	Comparator C2 positive input.
RC1/ANC1/C1IN1-/C2IN1-	RC1	TTL/ST	CMOS	General purpose I/O.
	ANC1	AN	—	ADC Channel C1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
RC2/ANC2/C1IN2-/C2IN2-/ MDCIN1(1)	RC2	TTL/ST	CMOS	General purpose I/O.
	ANC2	AN	—	ADC Channel C2 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	MDCIN1	TTL/ST	—	Modular Carrier input 1.

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open-Drain
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HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-2.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F18344 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC3/ANC3/C1IN3-/C2IN3-/ MDMIN(1)/ CCP2(1)/CLCIN1(1)/	RC3	TTL/ST	CMOS	General purpose I/O.
	ANC3	AN	—	ADC Channel C3 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	MDMIN	TTL/ST	—	Modular Source input.
	CCP2	TTL/ST	CMOS	Capture/Compare/PWM 2 input.
	CLCIN1	TTL/ST	—	Configurable Logic Cell 1 input.
RC4/ANC4	RC4	TTL/ST	CMOS	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
RC5/ANC5/MDCIN2(1)/ CCP1(1)	RC5	TTL/ST	CMOS	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	MDCIN2	TTL/ST	—	Modular Carrier input 2.
	CCP1	TTL/ST	CMOS	Capture/Compare/PWM 1 input.
RC6/ANC6/$\overline{SS1}$(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	ANC6	AN	—	ADC Channel C6 input.
	$\overline{SS1}$	TTL/ST	—	Slave Select 1 input.
RC7/ANC7	RC7	TTL/ST	CMOS	General purpose I/O.
	ANC7	AN	—	ADC Channel C7 input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
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Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-2.

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TABLE 1-3: PIC16(L)F18344 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1OUT	—	CMOS	Comparator C1 output.
	C2OUT	—	CMOS	Comparator C2 output.
	NCO1	—	CMOS	Numerically Controlled Oscillator output.
	DSM	—	CMOS	Digital Signal Modulator output.
	TMR0	—	CMOS	TMR0 clock output.
	CCP1	—	CMOS	Capture/Compare/PWM 1 output.
	CCP2	—	CMOS	Capture/Compare/PWM 2 output.
	CCP3	—	CMOS	Capture/Compare/PWM 3 output.
	CCP4	—	CMOS	Capture/Compare/PWM 4 output.
	PWM5	—	CMOS	Pulse-Width Modulator 5 output.
	PWM6	—	CMOS	Pulse-Width Modulator 6 output.
	CWG1A	—	CMOS	Complementary Waveform Generator 1 output A.
	CWG2A	—	CMOS	Complementary Waveform Generator 2 output A.
	CWG1B	—	CMOS	Complementary Waveform Generator 1 output B.
	CWG2B	—	CMOS	Complementary Waveform Generator 2 output B.
	CWG1C	—	CMOS	Complementary Waveform Generator 1 output C.
	CWG2C	—	CMOS	Complementary Waveform Generator 2 output C.
	CWG1D	—	CMOS	Complementary Waveform Generator 1 output D.
	CWG2D	—	CMOS	Complementary Waveform Generator 2 output D.
	SDA1(3)	I^2C	OD	I^2C data output.
	SCL1(3)	I^2C	OD	I^2C clock output.
	SDO1	—	CMOS	SPI1 data output.
	SCK1	—	CMOS	SPI1 clock output.
	TX/CK	—	CMOS	Asynchronous TX data/synchronous clock output.
	DT(3)	—	CMOS	EUSART synchronous data output.
	CLC1OUT	—	CMOS	Configurable Logic Cell 1 source output.
	CLC2OUT	—	CMOS	Configurable Logic Cell 2 source output.
	CLC3OUT	—	CMOS	Configurable Logic Cell 3 source output.
	CLC4OUT	—	CMOS	Configurable Logic Cell 4 source output.
	CLKR	—	CMOS	Clock Reference output.

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

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2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

2.0 GUIDELINES FOR GETTING STARTED WITH PIC16(L)F183XX MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC16(L)F183XX family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Power Supply Pins"**)
- MCLR pin (when configured for external operation) (see **Section 2.3 "Master Clear (MCLR) Pin"**)

These pins must also be connected if they are being used in the end application:

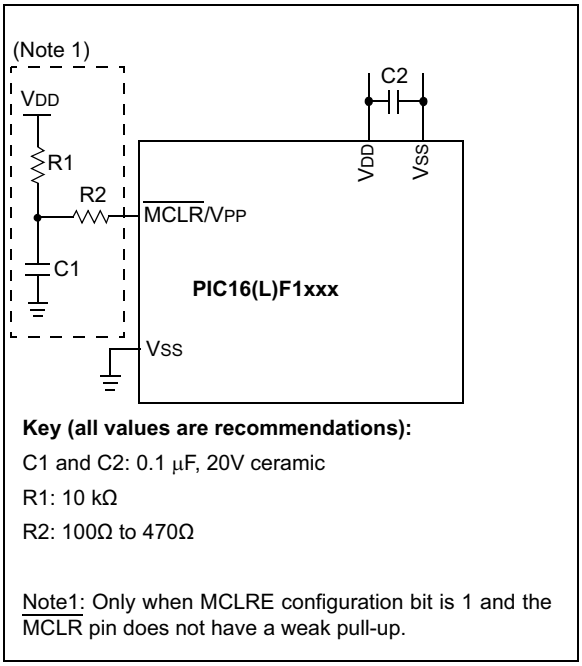
- ICSPCLK/ICSPDAT pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.4 "ICSP™ Pins"**)
- OSC1 and OSC2 pins when an external oscillator source is used (see **Section 2.5 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 and C2: 0.1 µF, 20V ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

Note1: Only when MCLRE configuration bit is 1 and the MCLR pin does not have a weak pull-up.

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins (VDD and VSS) is required. All VDD and VSS pins must be connected. None can be left floating.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 µF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 µF in parallel with 0.001 µF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 Master Clear ($\overline{MCLR}$) Pin

The MCLR pin provides three specific device functions:

- Device Reset (when MCLRE = 1)
- Digital input pin (when MCLRE = 0)
- Device Programming and Debugging

If programming and debugging are not required in the end application then either set the MCLRE configuration bit to '1' and use the pin as a digital input or clear the MCLRE Configuration bit and leave the pin open to use the internal weak pull-up. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, the programmer $\overline{MCLR}/V_{PP}$ output should be connected directly to the pin so that R1 isolates the capacitor, C1 from the $\overline{MCLR}$ pin during programming and debugging operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

2.4 ICSP™ Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be isolated from the programmer by resistors between the application and the device pins or removed from the circuit during programming. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/ emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 37.0 "Development Support"**.

2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 7.0 "Oscillator Module"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-2. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

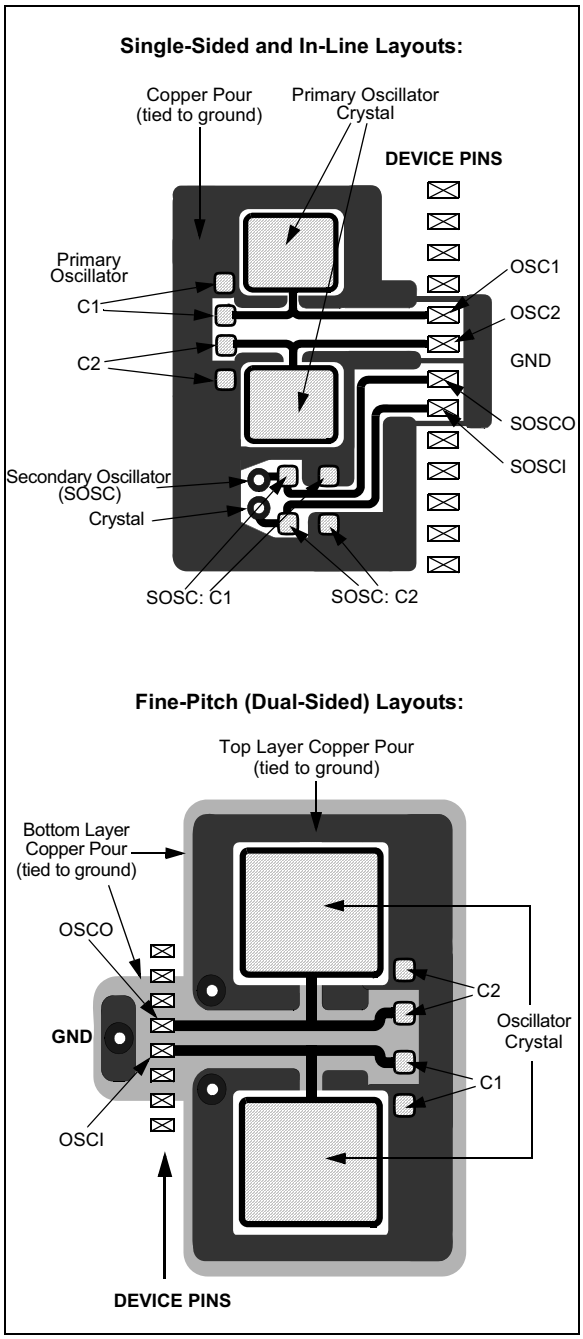
For additional information and design guidance on oscillator circuits, refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- AN826, *"Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- AN849, *"Basic PICmicro® Oscillator Design"*
- AN943, *"Practical PICmicro® Oscillator Analysis and Design"*
- AN949, *"Making Your Oscillator Work"*

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output logic low.

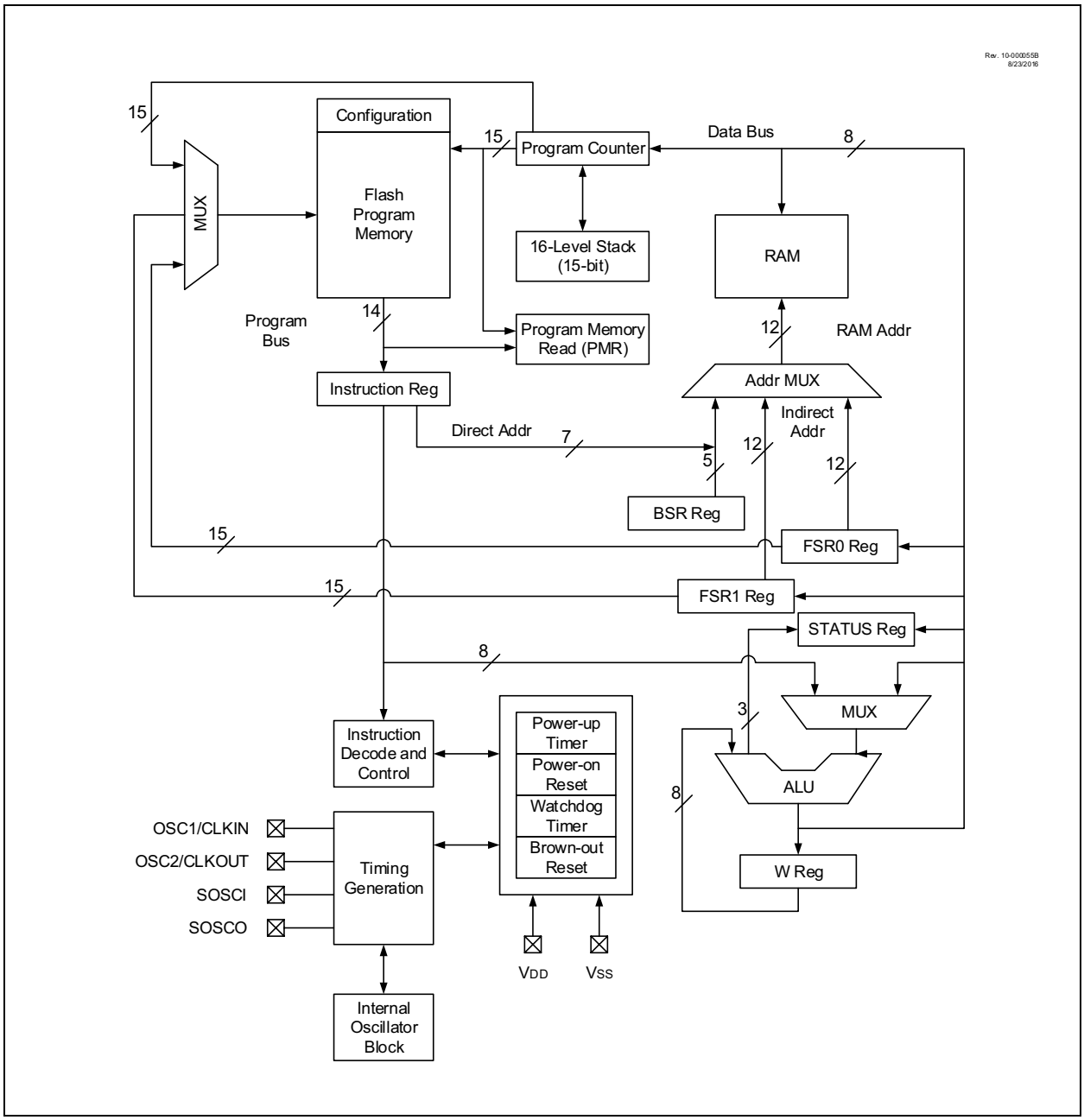
FIGURE 2-2: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



3.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 48 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16-levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

FIGURE 3-1: CORE DATA PATH BLOCK DIAGRAM



3.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 8.5 "Automatic Context Saving"** for more information.

3.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15-bits wide and 16-words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 4.4 "Stack"** for more details.

3.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers, program memory and data EEPROM, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. See **Section 4.5 "Indirect Addressing"** for more details.

3.4 Instruction Set

There are 48 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 34.0 "Instruction Set Summary"** for more details.

4.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - Revision ID
  - User ID
  - Program Flash Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
- Data EEPROM

4.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing 32K x 14 program memory space. Table 4-1 shows the memory sizes implemented. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 4-1).

TABLE 4-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Size (Words)	Last Program Memory Address
PIC16(L)F18324/18344	4096	0FFFh