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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Full-Featured 28/40/44-Pin Microcontrollers

Description

PIC16(L)F18856/76 microcontrollers feature Analog, Core Independent Peripherals and Communication Peripherals, combined with eXtreme Low-Power (XLP) technology for a wide range of general purpose and low-power applications. The family will feature the CRC/SCAN, Hardware Limit Timer (HLT) and Windowed Watchdog Timer (WWDT) to support customers looking to add safety to their application. Additionally, this family includes up to 28 KB of Flash memory, along with a 10-bit ADC with Computation (ADC²) extensions for automated signal analysis to reduce the complexity of the application.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
 - DC – 32 MHz clock input
 - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT) Extensions
- Four 16-Bit Timers (TMR0/1/3/5)
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
 - Variable prescaler selection
 - Variable window size selection
 - All sources configurable in hardware or software
- Programmable Code Protection

Memory

- Up to 28 KB Flash Program Memory
- Up to 2 KB Data SRAM
- 256B of EEPROM
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
 - 1.8V to 3.6V (PIC16LF18856/76)
 - 2.3V to 5.5V (PIC16F18856/76)
- Temperature Range:
 - Industrial: -40°C to 85°C
 - Extended: -40°C to 125°C

Power-Saving Functionality

- DOZE mode: Ability to run the CPU core slower than the system clock
- IDLE mode: Ability to halt CPU core while internal peripherals continue operating
- Sleep mode: Lowest Power Consumption
- Peripheral Module Disable (PMD):
 - Ability to disable hardware module to minimize power consumption of unused peripherals

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
 - 8 μ A @ 32 kHz, 1.8V, typical
 - 32 μ A/MHz @ 1.8V, typical

Digital Peripherals

- Four Configurable Logic Cells (CLC):
 - Integrated combinational and sequential logic
- Three Complementary Waveform Generators (CWG):
 - Rising and falling edge dead-band control
 - Full-bridge, half-bridge, 1-channel drive
 - Multiple signal sources
- Five Capture/Compare/PWM (CCP) module:
 - 16-bit resolution for Capture/Compare modes
 - 10-bit resolution for PWM mode
- 10-bit PWM:
 - Two 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
 - Generates true linear frequency control and increased frequency resolution
 - Input Clock: $0 \text{ Hz} < F_{\text{NCO}} < 32 \text{ MHz}$
 - Resolution: $F_{\text{NCO}}/2^{20}$
- Two Signal Measurement Timers (SMT):
 - 24-bit Signal Measurement Timer
 - Up to 12 different Acquisition modes

PIC16(L)F18856/76

Digital Peripherals (Cont.)

- Cyclical Redundancy Check (CRC/SCAN):
 - 16-bit CRC
 - Scans memory for NVM integrity
- Communication:
 - EUSART, RS-232, RS-485, LIN compatible
 - Two SPI
 - Two I²C, SMBus, PMBus™ compatible
- Up to 36 I/O Pins:
 - Individually programmable pull-ups
 - Slew rate control
 - Interrupt-on-change with edge-select
 - Input level selection control (ST or TTL)
 - Digital open-drain enable
 - Current mode enable
- Peripheral Pin Select (PPS):
 - Enables pin mapping of digital I/O
- Data Signal Modulator (DSM)
 - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC²):
 - 10-bit with up to 35 external channels
 - Automated post-processing
 - Automates math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
 - Operates in Sleep
- Two Comparators (COMP):
 - Fixed Voltage Reference at (non) inverting input(s)
 - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
 - 5-bit resolution, rail-to-rail
 - Positive Reference Selection
 - Unbuffered I/O pin output
 - Internal connections to ADCs and comparators
- Voltage Reference:
 - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
 - Software selectable frequency range up to 32 MHz, ±1% typical
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External Oscillator Block with:
 - Three crystal/resonator modes up to 20 MHz
 - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock stops
- Oscillator Start-up Timer (OST)
 - Ensures stability of crystal oscillator resources

PIC16(L)F18856/76

PIC16(L)F188XX Family Types

Device	Data Sheet Index	Program Flash Memory (Words)	Program Flash Memory (KB)	EEPROM (bytes)	Data SRAM (bytes)	I/O Pins ⁽¹⁾	10-Bit ADC ² (ch)	5-Bit DAC	Comparator	8-Bit (with HLT)/16-Bit Timers	SMT	Windowed Watchdog Timer	CRC and Memory Scan	CCP/10-Bit PWM	Zero-Cross Detect	CWG	NCO	CLC	DSM	EUSART/I ² C/SPI	Peripheral Pin Select	Peripheral Module Disable
PIC16(L)F18854	(1)	4096	7	256	512	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18855	(2)	8192	14	256	1024	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18856	(3)	16384	28	256	2048	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18857	(4)	32768	56	256	4096	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18875	(2)	8192	14	256	1024	36	35	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18876	(3)	16384	28	256	2048	36	35	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18877	(4)	32768	56	256	4096	36	35	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y

Note 1: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document)

- 1: DS40001826 [PIC16\(L\)F18854 Data Sheet, 28-Pin, Full-Featured 8-bit Microcontrollers](#)
- 2: DS40001802 [PIC16\(L\)F18855/75 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers](#)
- 3: DS40001824 [PIC16\(L\)F18856/76 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers](#)
- 4: DS40001825 [PIC16\(L\)F18857/77 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers](#)

Note: For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

PIC16(L)F18856/76

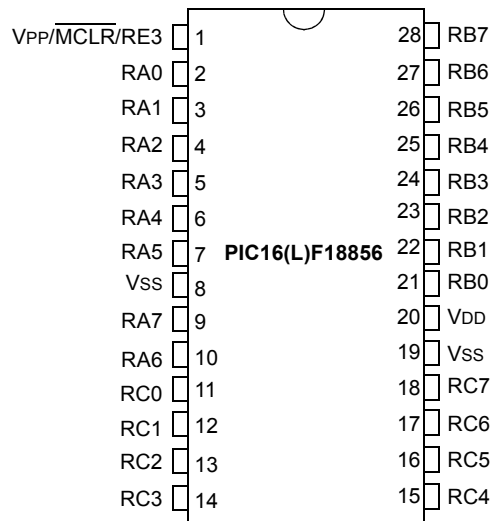
TABLE 1: PACKAGES

Packages	(S)PDIP	SOIC	SSOP	QFN (6x6)	UQFN (4x4)	TQFP	QFN (8x8)	UQFN (5x5)
PIC16(L)F18856	•	•	•	•	•			
PIC16(L)F18876	•					•	•	•

Note: Pin details are subject to change.

PIN DIAGRAMS

28-pin SPDIP, SOIC, SSOP

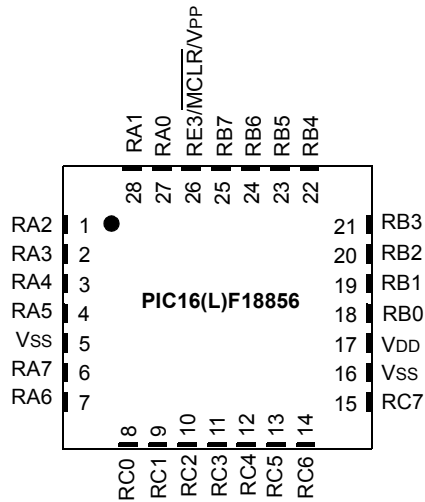


Note 1: See [Table 2](#) for location of all peripheral functions.

2: All VDD and all Vss pins must be connected at the circuit board level. Allowing one or more Vss or VDD pins to float may result in degraded electrical performance or non-functionality.

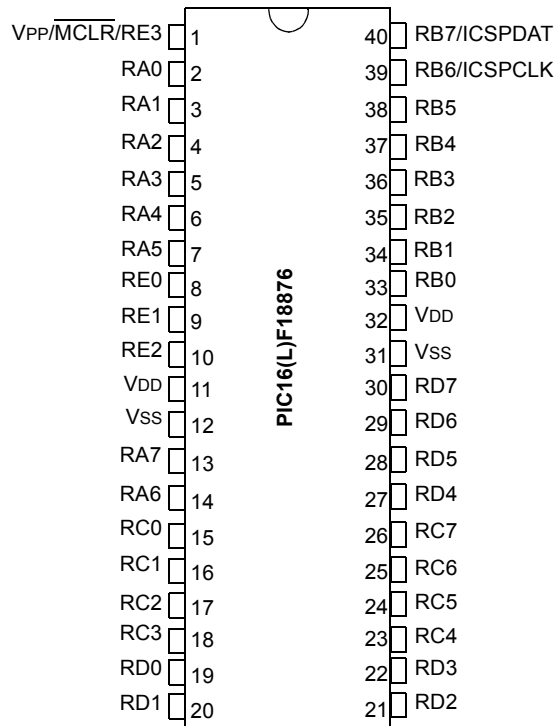
PIC16(L)F18856/76

28-pin QFN (6x6), UQFN (4x4)



- Note 1:** See [Table 2](#) for location of all peripheral functions.
- Note 2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.
- Note 3:** The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

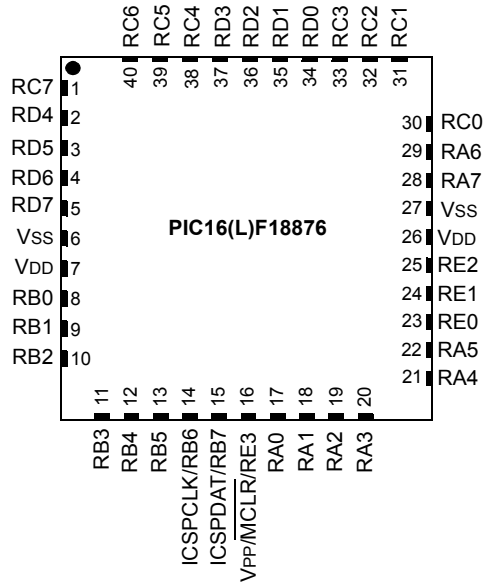
40-pin PDIP



- Note 1:** See [Table 3](#) for location of all peripheral function.
- Note 2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

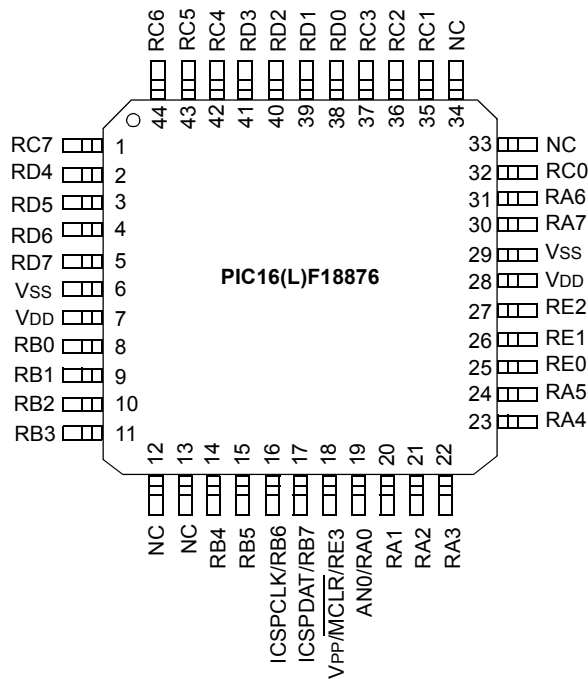
PIC16(L)F18856/76

40-pin UQFN (5x5)



- Note 1:** See [Table 3](#) for location of all peripheral functions.
- Note 2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.
- Note 3:** The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

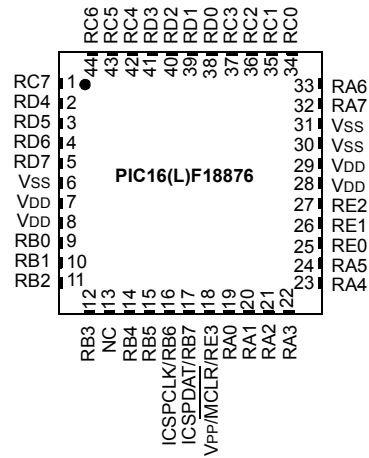
44-pin TQFP (10x10)



- Note 1:** See [Table 3](#) for location of all peripheral functions.
- Note 2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

PIC16(L)F18856/76

44-pin QFN (8x8)



- Note 1:** See [Table 3](#) for location of all peripheral functions.
- Note 2:** All VDD and all Vss pins must be connected at the circuit board level. Allowing one or more Vss or VDD pins to float may result in degraded electrical performance or non-functionality.
- Note 3:** The bottom pad of the QFN/UQFN package should be connected to Vss at the circuit board level.

PIN ALLOCATION TABLES

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16(L)F18856)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin (U) / QFN	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I ² C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	2	27	ANA0	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	CLCIN0 ⁽¹⁾	—	—	IOCA0	—
RA1	3	28	ANA1	—	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	CLCIN1 ⁽¹⁾	—	—	IOCA1	—
RA2	4	1	ANA2	VREF-	DAC1OUT1	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	IOCA2	—
RA3	5	2	ANA3	VREF+	—	C1IN1+	—	—	—	MDCARL ⁽¹⁾	—	—	—	—	—	—	IOCA3	—
RA4	6	3	ANA4	—	—	—	—	—	—	MDCARH ⁽¹⁾	T0CKI ⁽¹⁾	CCP5 ⁽¹⁾	—	—	—	—	IOCA4	—
RA5	7	4	ANA5	—	—	—	—	SS1 ⁽¹⁾	—	MDSRC ⁽¹⁾	—	—	—	—	—	—	IOCA5	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	OSC2 CLKOUT
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	OSC1 CLKIN
RB0	21	18	ANB0	—	—	C2IN1+	ZCD	SS2 ⁽¹⁾	—	—	—	CCP4 ⁽¹⁾	CWG1IN ⁽¹⁾	—	—	—	INT ⁽¹⁾ IOCB0	—
RB1	22	19	ANB1	—	—	C1IN3- C2IN3-	—	SCL2 ^(3,4) SCK2 ⁽¹⁾	—	—	—	—	CWG2IN ⁽¹⁾	—	—	—	IOCB1	—
RB2	23	20	ANB2	—	—	—	—	SDA2 ^(3,4) SDI2 ⁽¹⁾	—	—	—	—	CWG3IN ⁽¹⁾	—	—	—	IOCB2	—
RB3	24	21	ANB3	—	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	IOCB3	—
RB4	25	22	ANB4 ADCACT ⁽¹⁾	—	—	—	—	—	—	—	T5G ⁽¹⁾ SMTWIN2 ⁽¹⁾	—	—	—	—	—	IOCB4	—

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTX pins. Refer to [Table 13-1](#) for details on which port pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTX pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16(L)F18856) (CONTINUED)

O/I	28-Pin SPDIP/SOIC/SSOP	28-Pin (U)QFN	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I ² C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RB5	26	23	ANB5	—	—	—	—	—	—	—	T1G ⁽¹⁾ SMTSIG2 ⁽¹⁾	CCP3 ⁽¹⁾	—	—	—	—	IOCB5	—
RB6	27	24	ANB6	—	—	—	—	—	—	—	—	—	—	CLCIN2 ⁽¹⁾	—	—	IOCB6	ICSPCLK
RB7	28	25	ANB7	—	DAC1OUT2	—	—	—	—	—	T6IN ⁽¹⁾	—	—	CLCIN3 ⁽¹⁾	—	—	IOCB7	ICSPDAT
RC0	11	8	ANC0	—	—	—	—	—	—	—	T1CK1 ⁽¹⁾ T3CK1 ⁽¹⁾ T3G ⁽¹⁾ SMTWIN1 ⁽¹⁾	—	—	—	—	—	IOCC0	SOSCO
RC1	12	9	ANC1	—	—	—	—	—	—	—	SMTSIG1 ⁽¹⁾	CCP2 ⁽¹⁾	—	—	—	—	IOCC1	SOSCI
RC2	13	10	ANC2	—	—	—	—	—	—	—	T5CK1 ⁽¹⁾	CCP1 ⁽¹⁾	—	—	—	—	IOCC2	—
RC3	14	11	ANC3	—	—	—	—	SCL1 ^(3,4) SCK1 ⁽¹⁾	—	—	T2IN ⁽¹⁾	—	—	—	—	—	IOCC3	—
RC4	15	12	ANC4	—	—	—	—	SDA1 ^(3,4) SDI1 ⁽¹⁾	—	—	—	—	—	—	—	—	IOCC4	—
RC5	16	13	ANC5	—	—	—	—	—	—	—	T4IN ⁽¹⁾	—	—	—	—	—	IOCC5	—
RC6	17	14	ANC6	—	—	—	—	—	CK ⁽³⁾	—	—	—	—	—	—	—	IOCC6	—
RC7	18	15	ANC7	—	—	—	—	—	RX ⁽¹⁾ DT ⁽³⁾	—	—	—	—	—	—	—	IOCC7	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	MCLR VPP
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	8, 19	5, 16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTX pins. Refer to [Table 13-1](#) for details on which port pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTX pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16(L)F18856) (CONTINUED)

I/O	28-Pin SPDIP/SOIC/SSOP 28-Pin (U)QFN	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I ² C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
OUT ⁽²⁾	—	ADGRDA ADGRDB	—	—	C1OUT C2OUT	—	SDO1 SCK1 SDO2 SCK2	TX/ CK ⁽³⁾ DT ⁽³⁾	DSM	TMR0	CCP1 CCP2 CCP3 CCP4 CCP5 PWM6OUT PWM7OUT	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	NCO	CLKR	—	—

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTX pins. Refer to [Table 13-1](#) for details on which port pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTX pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16(L)F18876)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I ² C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	2	17	19	19	ANA0	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	CLCIN0 ⁽¹⁾	—	—	IOCA0	—
RA1	3	18	20	20	ANA1	—	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	CLCIN1 ⁽¹⁾	—	—	IOCA1	—
RA2	4	19	21	21	ANA2	VREF-	DAC1OUT1	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	IOCA2	—
RA3	5	20	22	22	ANA3	VREF+	—	C1IN1+	—	—	—	MDCARL ⁽¹⁾	—	—	—	—	—	—	IOCA3	—
RA4	6	21	23	23	ANA4	—	—	—	—	—	—	MDCARH ⁽¹⁾	T0CKI ⁽¹⁾	CCP5 ⁽¹⁾	—	—	—	—	IOCA4	—
RA5	7	22	24	24	ANA5	—	—	—	—	SS1 ⁽¹⁾	—	MDSRC ⁽¹⁾	—	—	—	—	—	—	IOCA5	—
RA6	14	29	33	31	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	OSC2 CLKOUT
RA7	13	28	32	30	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	OSC1 CLKIN
RB0	33	8	9	8	ANB0	—	—	C2IN1+	ZCD	SS2 ⁽¹⁾	—	—	—	CCP4 ⁽¹⁾	CWG1IN ⁽¹⁾	—	—	—	INT ⁽¹⁾ IOCB0	—
RB1	34	9	10	9	ANB1	—	—	C1IN3- C2IN3-	—	SCL2 ^(3,4) SCK2 ⁽¹⁾	—	—	—	—	CWG2IN ⁽¹⁾	—	—	—	IOCB1	—
RB2	35	10	11	10	ANB2	—	—	—	—	SDA2 ^(3,4) SDI2 ⁽¹⁾	—	—	—	—	CWG3IN ⁽¹⁾	—	—	—	IOCB2	—
RB3	36	11	12	11	ANB3	—	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	IOCB3	—
RB4	37	12	14	14	ANB4 ADCACT ⁽¹⁾	—	—	—	—	—	—	—	T5G ⁽¹⁾ SMTWIN2 ⁽¹⁾	—	—	—	—	—	IOCB4	—
RB5	38	13	15	15	ANB5	—	—	—	—	—	—	—	T1G ⁽¹⁾ SMTSIG2 ⁽¹⁾	CCP3(1)	—	—	—	—	IOCB5	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	—	—	—	—	CLCIN2 ⁽¹⁾	—	—	IOCB6	ICSPCLK
RB7	40	15	17	17	ANB7	—	DAC1OUT2	—	—	—	—	—	T6IN ⁽¹⁾	—	—	CLCIN3 ⁽¹⁾	—	—	IOCB7	ICSPDAT

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which port pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16(L)F18876) (CONTINUED)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I ² C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC0	15	30	34	32	ANC0	—	—	—	—	—	—	—	T1CKI ⁽¹⁾ T3CKI ⁽¹⁾ T3G ⁽¹⁾ SMTWIN1 ⁽¹⁾	—	—	—	—	—	IOCC0	SOSCO
RC1	16	31	35	35	ANC1	—	—	—	—	—	—	—	SMTSIG1 ⁽¹⁾	CCP2 ⁽¹⁾	—	—	—	—	IOCC1	SOSCI
RC2	17	32	36	36	ANC2	—	—	—	—	—	—	—	T5CKI ⁽¹⁾	CCP1 ⁽¹⁾	—	—	—	—	IOCC2	—
RC3	18	33	37	37	ANC3	—	—	—	—	SCL1 ^(3,4) SCK1 ⁽¹⁾	—	—	T2IN ⁽¹⁾	—	—	—	—	—	IOCC3	—
RC4	23	38	42	42	ANC4	—	—	—	—	SDA1 ^(3,4) SDI1 ⁽¹⁾	—	—	—	—	—	—	—	—	IOCC4	—
RC5	24	39	43	43	ANC5	—	—	—	—	—	—	—	T4IN ⁽¹⁾	—	—	—	—	—	IOCC5	—
RC6	25	40	44	44	ANC6	—	—	—	—	—	CK ⁽³⁾	—	—	—	—	—	—	—	IOCC6	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	RX ⁽¹⁾ DT ⁽³⁾	—	—	—	—	—	—	—	IOCC7	—
RD0	19	34	38	38	AND0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD1	20	35	39	39	AND1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD2	21	36	40	40	AND2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD3	22	37	41	41	AND3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE0	8	23	25	25	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE1	9	24	26	26	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE2	10	25	27	27	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which port pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16(L)F18876) (CONTINUED)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I ² C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	MCLR V _{PP}
V _{DD}	11, 32	7, 26	8, 28	7, 28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
V _{SS}	12, 31	6, 27	6, 31, 30	6, 29	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT ⁽²⁾	—	—	—	—	ADGRDA ADGRDB	—	—	C1OUT C2OUT	—	SDO1 SCK1 SDO2 SCK2	TX/ CK ⁽³⁾ DT ⁽³⁾	DSM	TMR0	CCP1 CCP2 CCP3 CCP4 CCP5 PWM6OUT PWM7OUT	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	NCO	CLKR	—	—

- Note** 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which port pins may be used for this signal.
- 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
- 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
- 4: These pins are configured for I²C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

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PIC16(L)F18856/76

1.0 DEVICE OVERVIEW

The PIC16(L)F18856/76 are described within this data sheet. The PIC16(L)F18856 devices are available in 28-pin SPDIP, SSOP, SOIC, and UQFN packages. The PIC16(L)F18876 devices are available in 40-pin PDIP and UQFN and 44-pin TQFP and QFN packages.

Figure 1-1 shows a block diagram of the PIC16(L)F18856/76 devices. Table 1-2 and Table 1-3 show the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral	PIC16(L)F18856	PIC16(L)F18876	
Analog-to-Digital Converter with Computation (ADC ²)	•	•	
Cyclic Redundancy Check (CRC)	•	•	
Digital-to-Analog Converter (DAC)	•	•	
Fixed Voltage Reference (FVR)	•	•	
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART1)	•	•	
Digital Signal Modulator (DSM)	•	•	
Numerically Controlled Oscillator (NCO1)	•	•	
Temperature Indicator	•	•	
Zero-Cross Detect (ZCD)	•	•	
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	•	•
	CCP2	•	•
	CCP3	•	•
	CCP4	•	•
	CCP5	•	•
Comparators			
	C1	•	•
	C2	•	•
Configurable Logic Cell (CLC)			
	CLC1	•	•
	CLC2	•	•
	CLC3	•	•
	CLC4	•	•
Complementary Waveform Generator (CWG)			
	CWG1	•	•
	CWG2	•	•
	CWG3	•	•
Master Synchronous Serial Ports			
	MSSP1	•	•
	MSSP2	•	•
Pulse-Width Modulator (PWM)			
	PWM6	•	•
	PWM7	•	•
Signal Measure Timer (SMT)			
	SMT1	•	•
	SMT2	•	•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	•	•
	Timer3	•	•
	Timer4	•	•
	Timer5	•	•
	Timer6	•	•

PIC16(L)F18856/76

1.1 Register and Bit naming conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW ~(1<<G1MD1)
ANDWF COG1CON0,F
MOVLW 1<<G1MD2 | 1<<G1MD0
IORWF COG1CON0,F
```

Example 2:

```
BSF COG1CON0,G1MD2
BCF COG1CON0,G1MD1
BSF COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt, and Mirror Bits

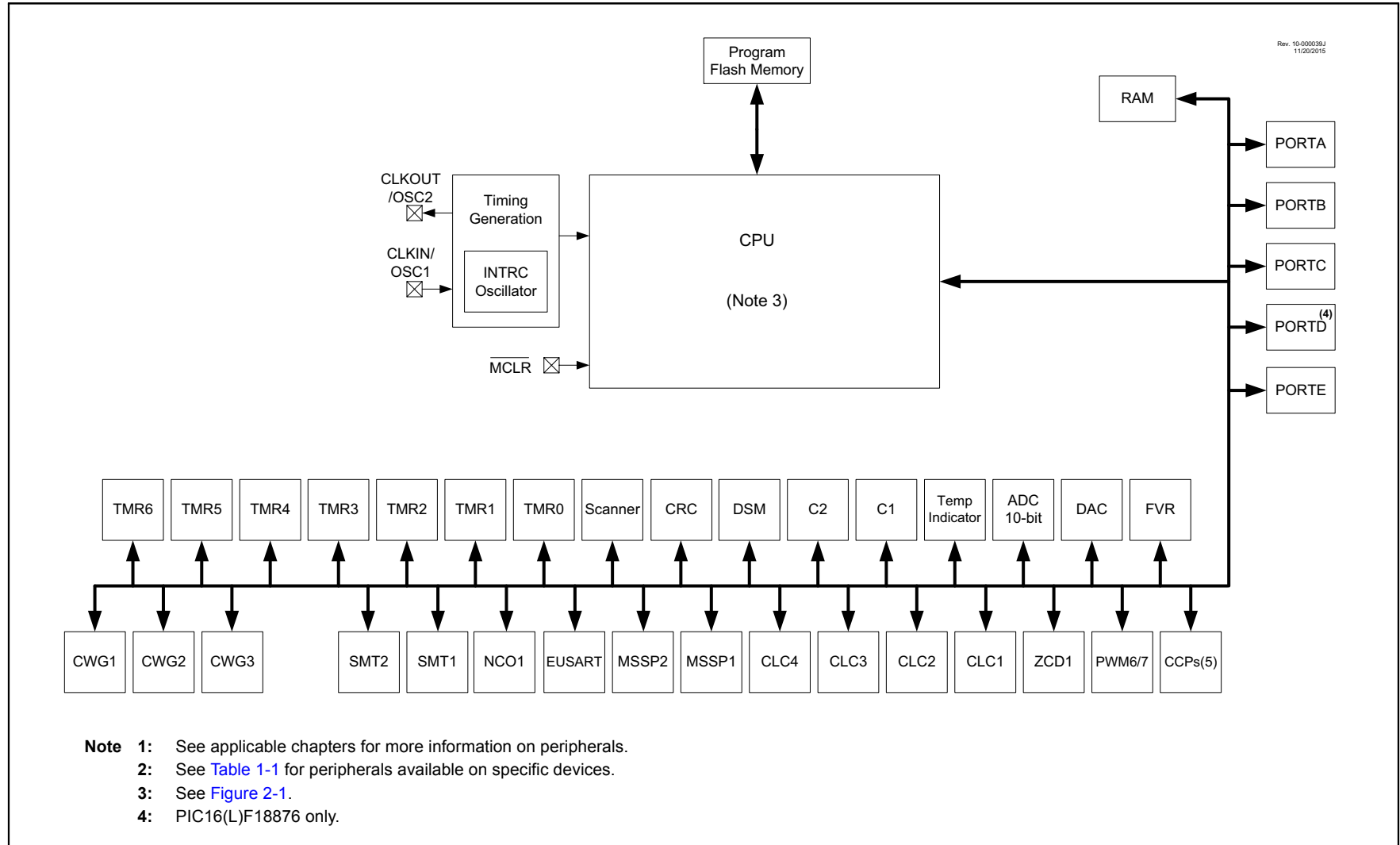
Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

- EUSART
- MSSP

FIGURE 1-1: PIC16(L)F18856/76 BLOCK DIAGRAM



- Note**
- 1: See applicable chapters for more information on peripherals.
 - 2: See [Table 1-1](#) for peripherals available on specific devices.
 - 3: See [Figure 2-1](#).
 - 4: PIC16(L)F18876 only.

PIC16(L)F18856/76

TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0-/C2IN0-/CLCIN0 ⁽¹⁾ /IOCA0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0-	AN	—	Comparator negative input.
	C2IN0-	AN	—	Comparator negative input.
	CLCIN0 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
RA1/ANA1/C1IN1-/C2IN1-/CLCIN1 ⁽¹⁾ /IOCA1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
	CLCIN1 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
RA2/ANA2/C1IN0+/C2IN0+/VREF-/DAC1OUT1/IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	C1IN0+	AN	—	Comparator positive input.
	C2IN0+	AN	—	Comparator positive input.
	VREF-	AN	—	External ADC and/or DAC negative reference input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
RA3/ANA3/C1IN1+/VREF+/MDCARL ⁽¹⁾ /IOCA3	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	ANA3	AN	—	ADC Channel A3 input.
	C1IN1+	AN	—	Comparator positive input.
	VREF+	AN	—	External ADC and/or DAC positive reference input.
	MDCARL ⁽¹⁾	TTL/ST	—	Modular Carrier input 1.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
RA4/ANA4/MDCARH ⁽¹⁾ /T0CKI ⁽¹⁾ /CCP5 ⁽¹⁾ /IOCA4	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	MDCARH ⁽¹⁾	TTL/ST	—	Modular Carrier input 2.
	T0CKI ⁽¹⁾	TTL/ST	—	Timer0 clock input.
	CCP5 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM5 (default input location for capture function).
	IOCA4	TTL/ST	—	Interrupt-on-change input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

PIC16(L)F18856/76

TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/ANA5/SS1 ⁽¹⁾ /MDSRC ⁽¹⁾ /IOCA5	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	SS1 ⁽¹⁾	TTL/ST	—	MSSP1 SPI slave select input.
	MDSRC ⁽¹⁾	TTL/ST	—	Modulator Source input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.
RA6/ANA6/OSC2/CLKOUT/IOCA6	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN	—	ADC Channel A6 input.
	OSC2	—	XTAL	External Crystal/Resonator (LP, XT, HS modes) driver output.
	CLKOUT	—	CMOS/OD	Fosc/4 digital output (in non-crystal/resonator modes).
	IOCA6	TTL/ST	—	Interrupt-on-change input.
RA7/ANA7/OSC1/CLKIN/IOCA7	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN	—	ADC Channel A7 input.
	OSC1	XTAL	—	External Crystal/Resonator (LP, XT, HS modes) driver input.
	CLKIN	TTL/ST	—	External digital clock input.
	IOCA7	TTL/ST	—	Interrupt-on-change input.
RB0/ANB0/C2IN1+/ZCD/SS2 ⁽¹⁾ /CCP4 ⁽¹⁾ /CWG1IN ⁽¹⁾ /INT ⁽¹⁾ /IOCB0	RB0	TTL/ST	CMOS/OD	General purpose I/O.
	ANB0	AN	—	ADC Channel B0 input.
	C2IN1+	AN	—	Comparator positive input.
	ZCD	AN	AN	Zero-cross detect input pin (with constant current sink/source).
	SS2 ⁽¹⁾	TTL/ST	—	MSSP2 SPI slave select input.
	CCP4 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM4 (default input location for capture function).
	CWG1IN ⁽¹⁾	TTL/ST	—	Complementary Waveform Generator 1 input.
	INT ⁽¹⁾	TTL/ST	—	External interrupt request input.
	IOCB0	TTL/ST	—	Interrupt-on-change input.
RB1/ANB1/C1IN3-/C2IN3-/SCL2 ^(3,4) /SCK2 ⁽¹⁾ /CWG2IN ⁽¹⁾ /IOCB1	RB1	TTL/ST	CMOS/OD	General purpose I/O.
	ANB1	AN	—	ADC Channel B1 input.
	C1IN3-	AN	—	Comparator negative input.
	C2IN3-	AN	—	Comparator negative input.
	SCL2 ^(3,4)	I ² C/ SMBus	OD	MSSP2 I ² C clock input/output.
	SCK2 ⁽¹⁾	TTL/ST	CMOS/OD	MSSP2 SPI serial clock (default input location, SCK2 is a PPS remappable input and output).
	CWG2IN ⁽¹⁾	TTL/ST	—	Complementary Waveform Generator 2 input.
	IOCB1	TTL/ST	—	Interrupt-on-change input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

PIC16(L)F18856/76

TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB2/ANB2/SDA2 ^(3,4) /SDI2 ⁽¹⁾ / CWG3IN ⁽¹⁾ /IOCB2	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	ANB2	AN	—	ADC Channel B2 input.
	SDA2 ^(3,4)	I ² C/ SMBus	OD	MSSP2 I ² C serial data input/output.
	SDI2 ⁽¹⁾	TTL/ST	—	MSSP2 SPI serial data input.
	CWG3IN ⁽¹⁾	TTL/ST	—	Complementary Waveform Generator 3 input.
	IOCB2	TTL/ST	—	Interrupt-on-change input.
RB3/ANB3/C1IN2-/C2IN2-/IOCB3	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	ANB3	AN	—	ADC Channel B3 input.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
	IOCB3	TTL/ST	—	Interrupt-on-change input.
RB4/ANB4/ADCACT ⁽¹⁾ /T5G ⁽¹⁾ / SMTWIN2 ⁽¹⁾ /IOCB4	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	ANB4	AN	—	ADC Channel B4 input.
	ADCACT ⁽¹⁾	TTL/ST	—	ADC Auto-Conversion Trigger input.
	T5G ⁽¹⁾	TTL/ST	—	Timer5 gate input.
	SMTWIN2 ⁽¹⁾	TTL/ST	—	Signal Measurement Timer 2 (SMT2) window input.
	IOCB4	TTL/ST	—	Interrupt-on-change input.
RB5/ANB5/T1G ⁽¹⁾ /SMTSIG2 ⁽¹⁾ / CCP3 ⁽¹⁾ /IOCB5	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	ANB5	AN	—	ADC Channel B5 input.
	T1G ⁽¹⁾	TTL/ST	—	Timer1 gate input.
	SMTSIG2 ⁽¹⁾	TTL/ST	—	Signal Measurement Timer 2 (SMT2) signal input.
	CCP3 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM3 (default input location for capture function).
	IOCB5	TTL/ST	—	Interrupt-on-change input.
RB6/ANB6/CLCIN2 ⁽¹⁾ /IOCB6/ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	ANB6	AN	—	ADC Channel B6 input.
	CLCIN2 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	IOCB6	TTL/ST	—	Interrupt-on-change input.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

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TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB7/ANB7/DAC1OUT2/T6IN ⁽¹⁾ / CLCIN3 ⁽¹⁾ /IOCB7/ICSPDAT	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	ANB7	AN	—	ADC Channel B7 input.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	T6IN ⁽¹⁾	TTL/ST	—	Timer6 external digital clock input.
	CLCIN3 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	IOCB7	TTL/ST	—	Interrupt-on-change input.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ and debugging data input/output.
RC0/ANC0/T1CKI ⁽¹⁾ /T3CKI ⁽¹⁾ /T3G ⁽¹⁾ / SMTWIN1 ⁽¹⁾ /IOCC0/SOSCO	RC0	TTL/ST	CMOS/OD	General purpose I/O.
	ANC0	AN	—	ADC Channel C0 input.
	T1CKI ⁽¹⁾	TTL/ST	—	Timer1 external digital clock input.
	T3CKI ⁽¹⁾	TTL/ST	—	Timer3 external digital clock input.
	T3G ⁽¹⁾	TTL/ST	—	Timer3 gate input.
	SMTWIN1 ⁽¹⁾	TTL/ST	—	Signal Measurement Timer1 (SMT1) input.
	IOCC0	TTL/ST	—	Interrupt-on-change input.
RC1/ANC1/SMTSIG1 ⁽¹⁾ /CCP2 ⁽¹⁾ / IOCC1/SOSCI	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	ANC1	AN	—	ADC Channel C1 input.
	SMTSIG1 ⁽¹⁾	TTL/ST	—	Signal Measurement Timer1 (SMT1) signal input.
	CCP2 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM2 (default input location for capture function).
	IOCC1	TTL/ST	—	Interrupt-on-change input.
	SOSCI	AN	—	32.768 kHz secondary oscillator crystal driver input.
	RC2/ANC2/T5CKI ⁽¹⁾ /CCP1 ⁽¹⁾ /IOCC2	RC2	TTL/ST	CMOS/OD
ANC2		AN	—	ADC Channel C2 input.
T5CKI ⁽¹⁾		TTL/ST	—	Timer5 external digital clock input.
CCP1 ⁽¹⁾		TTL/ST	CMOS/OD	Capture/compare/PWM1 (default input location for capture function).
IOCC2		TTL/ST	—	Interrupt-on-change input.
RC3/ANC3/SCL1 ^(3,4) /SCK1 ⁽¹⁾ /T2IN ⁽¹⁾ / IOCC3	RC3	TTL/ST	CMOS/OD	General purpose I/O.
	ANC3	AN	—	ADC Channel C3 input.
	SCL1 ^(3,4)	I ² C/ SMBus	OD	MSSP1 I ² C clock input/output.
	SCK1 ⁽¹⁾	TTL/ST	CMOS/OD	MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output).
	T2IN ⁽¹⁾	TTL/ST	—	Timer2 external input.
	IOCC3	TTL/ST	—	Interrupt-on-change input.

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TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

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TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/ANC4/SDA1 ^(3,4) /SDI1 ⁽¹⁾ /IOCC4	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
	SDA1 ^(3,4)	I ² C/ SMBus	OD	MSSP1 I ² C serial data input/output.
	SDI1 ⁽¹⁾	TTL/ST	—	MSSP1 SPI serial data input.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
RC5/ANC5/T4IN ⁽¹⁾ /IOCC5	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	T4IN ⁽¹⁾	TTL/ST	—	Timer4 external input.
	IOCC5	TTL/ST	—	Interrupt-on-change input.
RC6/ANC6/CK ⁽³⁾ /IOCC6	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	ANC6	AN	—	ADC Channel C6 input.
	CK ⁽³⁾	TTL/ST	CMOS/OD	EUSART synchronous mode clock input/output.
	IOCC6	TTL/ST	—	Interrupt-on-change input.
RC7/ANC7/RX ⁽¹⁾ /DT ⁽³⁾ /IOCC7	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	ANC7	AN	—	ADC Channel C7 input.
	RX ⁽¹⁾	TTL/ST	—	EUSART Asynchronous mode receiver data input.
	DT ⁽³⁾	TTL/ST	CMOS/OD	EUSART Synchronous mode data input/output.
	IOCC7	TTL/ST	—	Interrupt-on-change input.
RE3/IOCE3/MCLR/VPP	RE3	TTL/ST	—	General purpose input only (when MCLR is disabled by the Configuration bit).
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	MCLR	ST	—	Master clear input with internal weak pull up resistor.
	VPP	HV	—	ICSP™ High-Voltage Programming mode entry input.
VDD	VDD	Power	—	Positive supply voltage input.

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- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 13-1](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 13-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

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TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
Vss	Vss	Power	—	Ground reference.
OUT ⁽²⁾	ADGRDA	—	CMOS/OD	ADC Guard Ring A output.
	ADGRDB	—	CMOS/OD	ADC Guard Ring B output.
	C1OUT	—	CMOS/OD	Comparator 1 output.
	C2OUT	—	CMOS/OD	Comparator 2 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	SDO2	—	CMOS/OD	MSSP2 SPI serial data output.
	SCK2	—	CMOS/OD	MSSP2 SPI serial clock output.
	TX	—	CMOS/OD	EUSART Asynchronous mode transmitter data output.
	CK ⁽³⁾	—	CMOS/OD	EUSART Synchronous mode clock output.
	DT ⁽³⁾	—	CMOS/OD	EUSART Synchronous mode data output.
	DSM	—	CMOS/OD	Data Signal Modulator output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	Capture/Compare/PWM1 output (compare/PWM functions).
	CCP2	—	CMOS/OD	Capture/Compare/PWM2 output (compare/PWM functions).
	CCP3	—	CMOS/OD	Capture/Compare/PWM3 output (compare/PWM functions).
	CCP4	—	CMOS/OD	Capture/Compare/PWM4 output (compare/PWM functions).
	CCP5	—	CMOS/OD	Capture/Compare/PWM5 output (compare/PWM functions).
	PWM6OUT	—	CMOS/OD	PWM6 output.
	PWM7OUT	—	CMOS/OD	PWM7 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CWG2A	—	CMOS/OD	Complementary Waveform Generator 2 output A.
	CWG2B	—	CMOS/OD	Complementary Waveform Generator 2 output B.
	CWG2C	—	CMOS/OD	Complementary Waveform Generator 2 output C.
	CWG2D	—	CMOS/OD	Complementary Waveform Generator 2 output D.
	CWG3A	—	CMOS/OD	Complementary Waveform Generator 3 output A.
	CWG3B	—	CMOS/OD	Complementary Waveform Generator 3 output B.

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TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT ⁽²⁾	CWG3C	—	CMOS/OD	Complementary Waveform Generator 3 output C.
	CWG3D	—	CMOS/OD	Complementary Waveform Generator 3 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
	CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.
	NCO1	—	CMOS/OD	Numerically Controller Oscillator output.
	CLKR	—	CMOS/OD	Clock Reference module output.

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 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.