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PIC16(L)F19195/6/7

Full-Featured 64-Pin Microcontrollers

Description

PIC16(L)F19195/6/7 microcontrollers offer eXtreme Low-Power (XLP) LCD drive coupled with Core Independent Peripherals (CIPs) and Intelligent Analog. They are especially suited for battery-powered LCD applications due to an integrated charge pump, high current I/O drive for backlighting, and battery backup of the Real-Time Clock/Calendar (RTCC). Active clock tuning of the HFINTOSC provides a highly accurate clock source over voltage and temperature. The family also features a new 12-bit ADC controller which can automate Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and automatic threshold comparison. Other new features include low-power Idle and Doze modes, Device Information Area (DIA), and Memory Access Partition (MAP). These low-power products are available in 64 pins to support the customer in various LCD and general purpose applications.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - Two 8-bit (TMR2/4) Timer with Hardware Limit Timer Extension (HLT)
  - 16-bit (TMR0/1)
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software
- Programmable Code Protection

Memory

- Up to 56KB Flash Program Memory
- Up to 4KB Data SRAM Memory
- 256 bytes DataEE
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Bootloader write-protect
  - Custom partition
- Device Information Area (DIA):
  - Temp sensor factory calibrated data
  - Fixed Voltage Reference
  - Device ID

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF19195/6/7)
  - 2.3V to 5.5V (PIC16F19195/6/7)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze mode: Ability to run CPU core slower than the system clock
- Idle mode: Ability to halt CPU core while internal peripherals continue operating
- Sleep mode: Lowest power consumption
- Peripheral Module Disable (PMD): Ability to disable hardware module to minimize power consumption of unused peripherals

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 µA @ 32 kHz, 1.8V, typical
  - 32 µA/MHz @ 1.8V, typical

Digital Peripherals

- LCD Controller:
  - Up to 360 segments
  - Charge pump for low-voltage operation
  - Contrast control
- Four Configurable Logic Cell Modules (CLC):
  - Integrated combinational and sequential logic

- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
    - Multiple signal sources
- Two Capture/Compare/PWM (CCP) module
- Two 10-Bit PWMs
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Communication:
  - Two EUSART, RS-232, RS-485, LIN compatible
  - One SPI/I^2C, SMBus, PMBus™ compatible
- Up to 59 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC^2):
  - 12-bit with up to 45 external channels
  - Automates math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
  - Conversion available during Sleep
- Two Comparators:
  - (1) Low-Power Clocked Comparator
  - (1) High-Speed Comparator
  - Fixed Voltage Reference at (non)inverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detect Module:
  - AC high-voltage zero-crossing detection for simplifying TRIAC control
  - Synchronized switching control and timing

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Active Clock Tuning of HFINTOSC over voltage and temperature (ACT)
  - Selectable frequency range up to 32 MHz ±1% typical
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 31 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
  - Oscillator Start-up Timer (OST)
  - Ensures stability of crystal oscillator source
- External Oscillator Block with:
  - Three external clock modes up to 32 MHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripherals clock stops

TABLE 1: PIC16(L)F191XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (kW/KB)	DataEE (bytes)	Data SRAM (bytes)	I/O Pins	12-bit ADC (ch)	5-bit DAC	Comparator	8-bit/ (with HLT) Timer	16-bit Timer	Window Watchdog Timer (WWDT)	CCP/10-bit PWM	CWG	CLC	Zero-Cross Detect	Temperature Sensor	Memory Access Partition	Device Information Area	EUSART/ I^2C/SPI	Peripheral Pin Select	Peripheral Module Disable	Debug(1)	LCD Segments (Max)	LCD Charge Pump/ Bias Generator
PIC16(L)F19155	(A)	8/14	256	1024	24	20	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	96	Y/Y
PIC16(L)F19156	(A)	16/28	256	2048	24	20	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	96	Y/Y
PIC16(L)F19175	(A)	8/14	256	1024	35	31	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	184	Y/Y
PIC16(L)F19176	(A)	16/28	256	2048	35	31	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	184	Y/Y
PIC16(L)F19185	(A)	8/14	256	1024	43	39	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	248	Y/Y
PIC16(L)F19186	(A)	16/28	256	2048	43	39	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	248	Y/Y
PIC16(L)F19195	(B)	8/14	256	1024	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y
PIC16(L)F19196	(B)	16/28	256	2048	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y
PIC16(L)F19197	(B)	32/56	256	4096	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y

Note 1: I – Debugging integrated on chip.

Data Sheet Index (Unshaded devices are described in this document):

A. DS40001923 PIC16(L)F19155/56/75/76/85/86 Data Sheet, 28/40/44/48-Pin

B. DS40001873 PIC16(L)F19195/6/7 Data Sheet, Full-Featured 64-Pin Microcontrollers

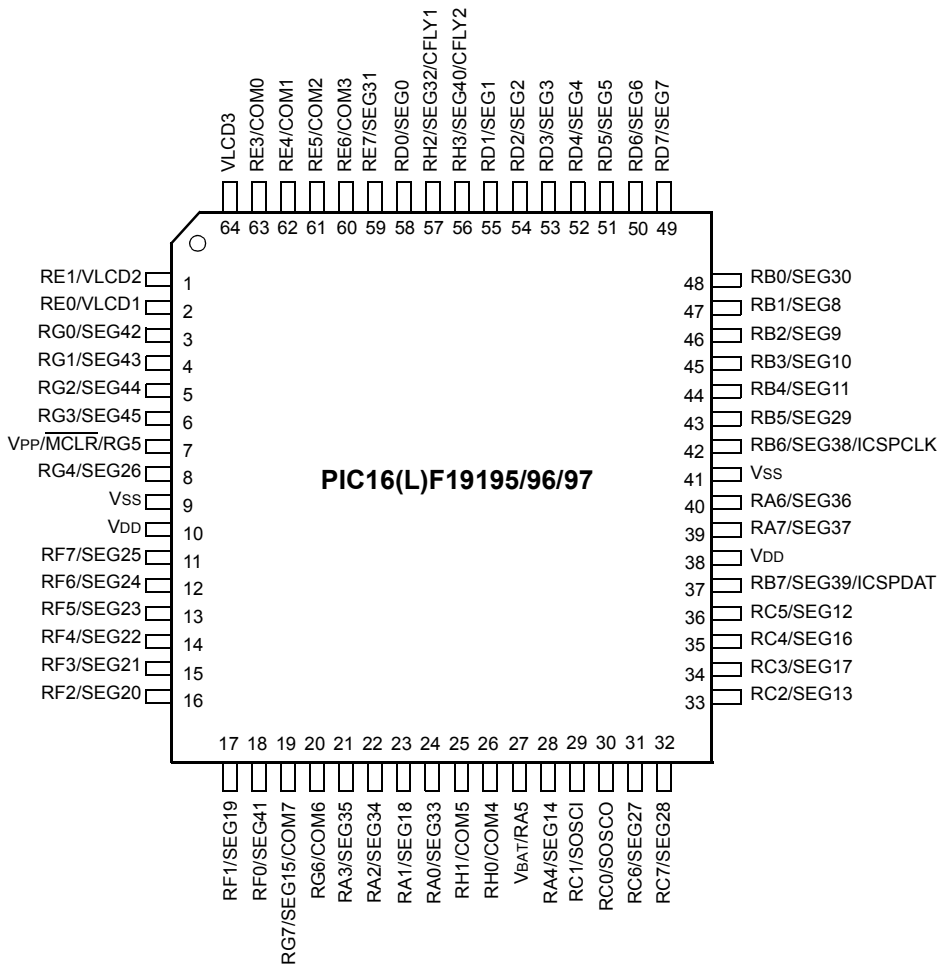
Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

TABLE 2: PACKAGES

Device	64-Pin TQFP (10x10)	64-Pin QFN (9x9)
PIC16(L)F19195	X	X
PIC16(L)F19196	X	X
PIC16(L)F19197	X	X

Note: Pin details are subject to change.

FIGURE 1: 64-PIN TQFP (10X10X1)/QFN (9X9X0.9) PIN DIAGRAM FOR PIC16(L)F19195/6/7



Note 1: QFN package orientation is the same. No leads are present on the QFN package.

2: See Table 3 for location of all peripheral functions.

PIN ALLOCATION TABLES

TABLE 3: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/6/7)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RA0	24	ANA0	—	C1IN4- C2IN4-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	SEG33	—	—	Y	—
RA1	23	ANA1	—	—	—	—	T2IN(1)	—	—	—	—	—	CLCIN1(1)	—	SEG18	—	—	Y	—
RA2	22	ANA2	—	C1IN1+ C2IN1+	—	—	—	—	—	—	—	—	—	—	SEG34	—	—	Y	—
RA3	21	ANA3	V_{REF+}	—	—	$DAC1_{REF+}$	—	—	—	—	—	—	—	—	SEG35	—	—	Y	—
RA4	28	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	SEG14	—	—	Y	—
RA5	27	—	—	—	—	—	—	—	—	—	—		—	—	—	—	—	Y	V_{BAT}
RA6	40	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	SEG36	—	—	Y	CLKOUT
RA7	39	ANA7	—	—	—	—	—	—	—	—	—		—	—	SEG37	—	—	Y	CLKIN
RB0	48	ANB0	—	—	ZCD	—	—	—	—	—	—	—	—	—	SEG30	INT(1)	—	Y	—
RB1	47	ANB1	—	—	—	—	—	—	—	—	SCL, SDA(1,3,4,5,6)		—	—	SEG8	IOCB1	—	Y	—
RB2	46	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1,3,4,5,6)	—	—	—	SEG9	IOCB2	—	Y	—
RB3	45	ANB3	—	—	—	—	—	—	—	—	—	—	—	—	SEG10	IOCB3	—	Y	—
RB4	44	ANB4	—	—	—	—	—	—	—	—	—	—	—	—	SEG11	IOCB4	—	Y	—
RB5	43	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	SEG29	IOCB5	—	Y	—
RB6	42	ANB6	—	—	—	—	—	—	—	—	—	—	CLCIN2(1)	—	SEG38	IOCB6	—	Y	ICDCLK/ ICSPCLK
RB7	37	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	—	CLCIN3(1)	—	SEG39	IOCB7	—	Y	ICDDAT/ ICSPDAT
RC0	30	—	—	—	—	—	T1CKI(1)	—	—	—	—	—	—	—	—	IOCC0	—	Y	SOSCO

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL or SDA pins.

TABLE 3: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/6/7) (CONTINUED)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RC1	29	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC1	—	Y	SOSCI
RC2	33	—	—	—	—	—	—	—	—	CWG1IN(1)	—	—	—	—	SEG13	IOCC2	—	Y	—
RC3	34	—	—	—	—	—	—	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	SEG17	IOCC3	—	Y	—
RC4	35	—	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	SEG16	IOCC4	—	Y	—
RC5	36	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG12	IOCC5	—	Y	—
RC6	31	—	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	SEG27	IOCC6	—	Y	—
RC7	32	—	—	—	—	—	—	—	—	—	—	RX1(1) DT1 (1)	—	—	SEG28	IOCC7	—	Y	—
RD0	58	AND0	—	—	—	—	—	—	—	—	—	—	—	—	SEG0	—	—	Y	—
RD1	55	AND1	—	—	—	—	—	—	—	—	—	—	—	—	SEG1	—	—	Y	—
RD2	54	AND2	—	—	—	—	—	—	—	—	—	—	—	—	SEG2	—	—	Y	—
RD3	53	AND3	—	—	—	—	—	—	—	—	—	—	—	—	SEG3	—	—	Y	—
RD4	52	AND4	—	—	—	—	—	—	—	—	—	—	—	—	SEG4	—	—	Y	—
RD5	51	AND5	—	—	—	—	—	—	—	—	—	—	—	—	SEG5	—	—	Y	—
RD6	50	AND6	—	—	—	—	—	—	—	—	—	—	—	—	SEG6	—	—	Y	—
RD7	49	AND7	—	—	—	—	—	—	—	—	—	—	—	—	SEG7	—	—	Y	—
RE0	2	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	VLCD1	—	—	Y	—
RE1	1	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	VLCD2	—	—	Y	—
RE3	63	ANE3	—	—	—	—	—	—	—	—	—	—	—	—	COM0	IOCE3	—	Y	—
RE4	62	ANE4	—	—	—	—	T4IN(1)	CCP2(1)	—	—	—	—	—	—	COM1	IOCE4	—	Y	—
RE5	61	ANE5	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	COM2	IOCE5	—	Y	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL or SDA pins.

TABLE 3: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/6/7) (CONTINUED)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RE6	60	ANE6	—	—	—	—	SMTWIN1(1)	—	—	—	—	—	—	—	COM3	IOCE6	—	Y	—
RE7	59	ANE7	—	—	—	—	SMTSIG1(1)	—	—	—	—	—	—	—	SEG31	IOCE7	—	Y	—
RF0	18	ANF0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	SEG41	—	—	Y	—
RF1	17	ANF1	—	—	—	—	—	—	—	—	—	—	—	—	SEG19	—	—	Y	—
RF2	16	ANF2	—	—	—	—	—	—	—	—	—	—	—	—	SEG20	—	—	Y	—
RF3	15	ANF3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	SEG21	—	—	Y	—
RF4	14	ANF4	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	SEG22	—	—	Y	—
RF5	13	ANF5	—	C1IN1- C2IN1-	—	DAC1OUT1	—	—	—	—	—	—	—	—	SEG23	—	—	Y	—
RF6	12	ANF6	—	C1IN0+	—	—	—	—	—	—	—	—	—	—	SEG24	—	—	Y	—
RF7	11	ANF7	—	C1IN3- C2IN3-	—	—	—	—	—	—	SS(1)	—	—	—	SEG25	—	HIDF7	Y	—
RG0	3	ANG0	—	—	—	—	—	—	—	—	—	—	—	—	SEG42	—	—	Y	—
RG1	4	ANG1	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	—	—	SEG43	—	—	Y	—
RG2	5	ANG2	—	—	—	—	—	—	—	—	—	RX2(1) DT2(1)	—	—	SEG44	—	—	Y	—
RG3	6	ANG3	—	—	—	—	—	—	—	—	—	—	—	—	SEG45	—	—	Y	—
RG4	8	ANG4	—	—	—	—	—	—	—	—	—	—	—	—	SEG26	—	—	Y	—
RG5	7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOG5	—	Y	$\overline{MCLR}$ VPP
RG6	20	ANG6	—	—	—	—	—	—	—	—	—	—	—	—	COM6	—	—	Y	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL or SDA pins.

TABLE 3: 64-PIN ALLOCATION TABLE (PIC16(L)F19195/6/7) (CONTINUED)

I/O(2)	64-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RG7	19	ANG7	—	—	—	—	—	—	—	—	—	—	—	—	SEG15 COM7	—	—	Y	—
RH0	26	—	—	—	—	—	—	—	—	—	—	—	—	—	COM4	—	—	Y	—
RH1	25	ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	COM5	—	—	Y	—
RH2	57	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG32 CFLY1	—	—	Y	—
RH3	56	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG40 CFLY2	—	—	Y	—
VLCD3	64	—	—	—	—	—	—	—	—	—	—	—	—	—	VLCD3	—	—	—	—
VDD	10	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VDD	38	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
VSS	41	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	—	—	—	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL or SDA pins.

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To determine if an errata sheet exists for a particular device, please check with one of the following:

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1.0 DEVICE OVERVIEW

The PIC16(L)F19195/6/7 are described within this data sheet. The PIC16(L)F19195/6/7 devices are available in 64-pin TQFP and QFN packages. Figure 1-1 shows a block diagram of the PIC16(L)F19195/6/7 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F19195/6/7
Analog-to-Digital Converter with Computation (ADC^2)		•
Digital-to-Analog Converter (DAC1)		•
Fixed Voltage Reference (FVR)		•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1 and EUSART2)		•
Temperature Indicator Module (TIM)		•
Zero-Cross Detect (ZCD1)		•
Real-Time Calendar and Clock (RTCC)		•
Liquid Crystal Display (LCD)		•
Capture/Compare/PWM Modules (CCP)		
	CCP1	•
	CCP2	•
Comparator Module (Cx)		
	C1	•
	C2	•
Configurable Logic Cell (CLC)		
	CLC1	•
	CLC2	•
	CLC3	•
	CLC4	•
Complementary Waveform Generator (CWG)		
	CWG1	•
Master Synchronous Serial Ports (MSSP)		
	MSSP1	•
Pulse-Width Modulator (PWM)		
	PWM3	•
	PWM4	•
Signal Measure Timer (SMT)		
	SMT1	•
Timers		
	Timer0	•
	Timer1	•
	Timer2	•
	Timer4	•

1.1 Register and Bit Naming Conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral, thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

Example 2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt, and Mirror Bits

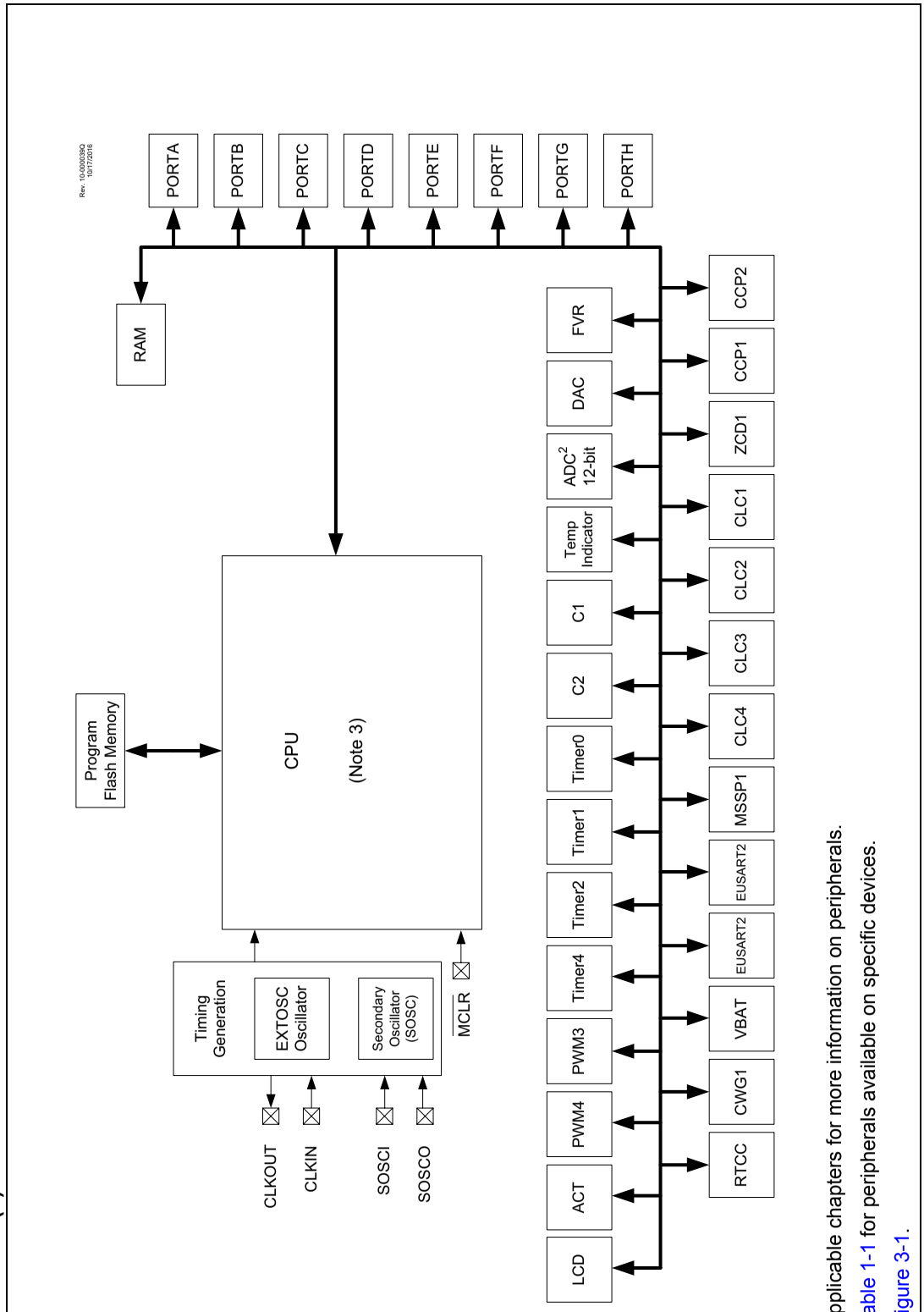
Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

- EUSART
- MSSP

FIGURE 1-1: PIC16(L)F19195/6/7 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

2: See Table 1-1 for peripherals available on specific devices.

3: See Figure 3-1.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/C2IN4-/C1IN4-/ANA0/CLCIN0(1)/SEG33	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN4-	AN		Comparator negative input.
	C1IN4-	AN		Comparator negative input.
	ANA0	AN		ADC Channel input.
	CLCIN0(1)	—		Configurable Logic Cell source input.
	SEG33	AN		LCD Analog output.
RA1/ANA1/CLCIN1(1)/T2IN(1)/SEG18	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN		ADC Channel input.
	CLCIN1(1)	—		Configurable Logic Cell source input.
	T2IN(1)	—		Timer2 external input.
	SEG18	AN		LCD Analog output.
RA2/C2IN1+/C1IN1+/ANA2/SEG34	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN1+	AN		Comparator positive input.
	C1IN1+	AN		Comparator positive input.
	ANA2	AN		ADC Channel input.
	SEG34	AN		LCD Analog output.
RA3/ANA3/SEG35/VREF+ (ADC)/VREF+ (DAC1)	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	ANA3	AN		ADC Channel input.
	SEG35	AN		LCD Analog output.
	VREF+ (ADC)	AN		ADC positive reference.
	VREF+ (DAC1)	AN		DAC positive reference.
RA4/ANA4/T0CKI(1)/SEG14	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN		ADC Channel input.
	T0CKI(1)	—		Timer0 clock input.
	SEG14	AN		LCD Analog output.
RA5/VBAT	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	VBAT	AN		RTCC Back-up Battery.
RA6/ANA6/SEG36/CLKOUT	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN		ADC Channel input.
	SEG36	AN		LCD Analog output.
	CLKOUT	TTL/ST		FOSC/4 digital output.
RA7/ANA7/SEG37/CLKIN	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN		ADC Channel input.
	SEG37	AN		LCD Analog output.
	CLKIN	ST		External Clock input.
RB0/IOCB0/ANB0/SEG30/ZCD	RB0	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB0	TTL/ST		Interrupt-on-change input.
	ANB0	AN		ADC Channel input.
	SEG30	AN		LCD Analog output.
	ZCD	—		Zero-cross detect input pin (with constant current sink/source).

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB1/IOCB1/SCL(3)(4)/SCK(1)/ANB1/SEG8	RB1	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB1	TTL/ST	—	Interrupt-on-change input.
	SCL(3)(4)	I^2C	OD	MSSPI^2C clock input/output.
	SCK(1)	—	—	MSSP SPI clock input/output.
	ANB1	AN	—	ADC Channel input.
	SEG8	AN	—	LCD Analog output.
RB2/IOCB2/SDA(3)(4)/SDI(1)/ANB2/SEG9	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB2	TTL/ST	—	Interrupt-on-change input.
	SDA(3)(4)	I^2C	OD	MSSP I^2C data input/output.
	SDI(1)	—	—	MSSP SPI serial data in.
	ANB2	AN	—	ADC Channel input.
	SEG9	AN	—	LCD Analog output.
RB3/IOCB3/ANB3/SEG10	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB3	TTL/ST		Interrupt-on-change input.
	ANB3	AN		ADC Channel input.
	SEG10	AN		LCD Analog output.
RB4/IOCB4/ANB4/SEG11	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB4	TTL/ST		Interrupt-on-change input.
	ANB4	AN		ADC Channel input.
	SEG11	AN		LCD Analog output.
RB5/IOCB5/ANB5/T1G(1)/SEG29	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB5	TTL/ST		Interrupt-on-change input.
	ANB5	AN		ADC Channel input.
	T1G(1)	—		Timer1 Gate input.
	SEG29	AN		LCD Analog output.
RB6/IOCB6/ANB6/CLCIN2(1)/SEG38/ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB6	TTL/ST		Interrupt-on-change input.
	ANB6	AN		ADC Channel input.
	CLCIN2(1)			Configurable Logic Cell source input.
	SEG38	AN		LCD Analog output.
	ICSPCLK	ST		In-Circuit Serial Programming™ and debugging clock input.
RB7/IOCB7/ANB7/CLCIN3(1)/SEG39/ DAC1OUT2/ICSPDAT	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB7	TTL/ST	—	Interrupt-on-change input.
	ANB7	AN	—	ADC Channel input.
	CLCIN3(1)	—	—	Configurable Logic Cell source input.
	SEG39	AN	—	LCD Analog output.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	TTL/ST	—	In-Circuit Serial Programming™ and debugging data input/output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC0/IOCC0/T1CKI(1)/SOSCO	RC0	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC0	TTL/ST	—	Interrupt-on-change input.
	T1CKI(1)	—	—	Timer1 clock input.
	SOSCO	—	AN	32.768 kHz secondary oscillator crystal driver output.
RC1/IOCC1/SOSCI	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC1	TTL/ST		Interrupt-on-change input.
	SOSCI	—		32.768 kHz secondary oscillator crystal driver input.
RC2/IOCC2/SEG13/CWG1IN(1)	RC2	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC2	TTL/ST		Interrupt-on-change input.
	SEG13	AN		LCD Analog output.
	CWG1IN(1)	TTL/ST	—	Complementary Waveform Generator 1 input.
RC3/IOCC3/SCL(3)(4)/SCK(1)/SEG17	RC3	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC3	TTL/ST	—	Interrupt-on-change input.
	SCL(3)(4)	I^2C	OD	MSSP I^2C clock input/output.
	SCK(1)	—	—	MSSP SPI clock input/output
	SEG17	AN	—	LCD Analog output.
RC4/IOCC4/SDA(3)(4)/SDI(1)/SEG16	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
	SDA(3)(4)	—	—	MSSP I^2C data input/output.
	SDI(1)	I^2C	OD	MSSP SPI serial data in.
	SEG16	AN	—	LCD Analog output.
RC5/IOCC5/SEG12	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC5	TTL/ST		Interrupt-on-change input.
	SEG12	AN		LCD Analog output.
RC6/IOCC6/CK1(3)/TX1(1)/SEG27	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC6	TTL/ST		Interrupt-on-change input.
	CK1(3)	—		EUSART synchronous clock out.
	TX1(1)	—		EUSART asynchronous TX data out.
	SEG27	AN		LCD Analog output.
RC7/IOCC7/DT1(3)/RX1(1)/SEG28	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	IOCC7	TTL/ST		Interrupt-on-change input.
	DT1(3)	—		EUSART synchronous data output.
	RX1(1)	—		EUSART receive input.
	SEG28	AN		LCD Analog output.
RD0/AND0/SEG0	RD0	TTL/ST	CMOS/OD	General purpose I/O.
	AND0	AN		ADC Channel input.
	SEG0	AN		LCD Analog output.
RD1/AND1/SEG1	RD1	TTL/ST	CMOS/OD	General purpose I/O.
	AND1	AN		ADC Channel input.
	SEG1	AN		LCD Analog output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD2/AND2/SEG2	RD2	TTL/ST	CMOS/OD	General purpose I/O.
	AND2	AN		ADC Channel input.
	SEG2	AN		LCD Analog output.
RD3/AND3/SEG3	RD3	TTL/ST	CMOS/OD	General purpose I/O.
	AND3	AN		ADC Channel input.
	SEG3	AN		LCD Analog output.
RD4/AND4/SEG4	RD4	TTL/ST	CMOS/OD	General purpose I/O.
	AND4	AN		ADC Channel input.
	SEG4	AN		LCD Analog output.
RD5/AND5/SEG5	RD5	TTL/ST	CMOS/OD	General purpose I/O.
	AND5	AN		ADC Channel input.
	SEG5	AN		LCD Analog output.
RD6/AND6/SEG6	RD6	TTL/ST	CMOS/OD	General purpose I/O.
	AND6	AN		ADC Channel input.
	SEG6	AN		LCD Analog output.
RD7/AND7/SEG7	RD7	TTL/ST	CMOS/OD	General purpose I/O.
	AND7	AN		ADC Channel input.
	SEG7	AN		LCD Analog output.
RE0/ANE0/VLCD1	RE0	TTL/ST	CMOS/OD	General purpose I/O.
	ANE0	AN		ADC Channel input.
	VLCD1	AN		LCD analog input.
RE1/ANE1/VLCD2	RE1	TTL/ST	CMOS/OD	General purpose I/O.
	ANE1	AN		ADC Channel input.
	VLCD2	AN		LCD analog input.
RE3/IOCE3/ANE3/COM0	RE3	TTL/ST	CMOS/OD	General purpose I/O.
	IOCE3	TTL/ST		Interrupt-on-change input.
	ANE3	AN		ADC Channel input.
	COM0	AN		LCD Driver Common Outputs.
RE4/IOCE4/ANE4/T4IN(1)/CCP2(1)/COM1	RE4	TTL/ST	CMOS/OD	General purpose I/O.
	IOCE4	TTL/ST		Interrupt-on-change input.
	ANE4	AN		ADC Channel input.
	T4IN(1)	—		Timer4 external input.
	CCP2(1)	—		CCP Capture Input.
	COM1	AN		LCD Driver Common Outputs.
RE5/IOCE5/ANE5/CCP1(1)/COM2	RE5	TTL/ST	CMOS/OD	General purpose I/O.
	IOCE5	TTL/ST		Interrupt-on-change input.
	ANE5	AN		ADC Channel input.
	CCP1(1)	—		CCP Capture Input.
	COM2	AN		LCD Driver Common Outputs.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RE6/IOCE6/ANE6/SMTWIN1(1)/COM3	RE6	TTL/ST	CMOS/OD	General purpose I/O.
	IOCE6	TTL/ST		Interrupt-on-change input.
	ANE6	AN		ADC Channel input.
	SMTWIN1(1)	—		SMT window input.
	COM3	AN		LCD Driver Common Outputs.
RE7/IOCE7/ANE7/SMTSIG1(1)/SEG31	RE7	TTL/ST	CMOS/OD	General purpose I/O.
	IOCE7	TTL/ST		Interrupt-on-change input.
	ANE7	AN		ADC Channel input.
	SMTSIG1(1)	—		SMT signal input.
	SEG31	AN		LCD Analog output.
RF0/C2IN0-/C1IN0-/ANF0/SEG41	RF0	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN0-	AN		Comparator negative input.
	C1IN0-	AN		Comparator negative input.
	ANF0	AN		ADC Channel input.
	SEG41	AN		LCD Analog output.
RF1/ANF1/SEG19	RF1	TTL/ST	CMOS/OD	General purpose I/O.
	ANF1	AN		ADC Channel input.
	SEG19	AN		LCD Analog output.
RF2/ANF2/SEG20	RF2	TTL/ST	CMOS/OD	General purpose I/O.
	ANF2	AN		ADC Channel input.
	SEG20	AN		LCD Analog output.
RF3/C2IN2-/C1IN2-/ANF3/SEG21	RF3	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN2-	AN		Comparator negative input.
	C1IN2-	AN		Comparator negative input.
	ANF3	AN		ADC Channel input.
	SEG21	AN		LCD Analog output.
RF4/C2IN0+/ANF4/SEG22	RF4	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN0+	AN		Comparator positive input.
	ANF4	AN		ADC Channel input.
	SEG22	AN		LCD Analog output.
RF5/C2IN1-/C1IN1-/ANF5/SEG23/DAC1OUT1	RF5	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN1-	AN		Comparator negative input.
	C1IN1-	AN		Comparator negative input.
	ANF5	AN		ADC Channel input.
	SEG23	AN		LCD Analog output.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
RF6/C1IN0+/ANF6/SEG24	RF6	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN0+	AN		Comparator positive input.
	ANF6	AN		ADC Channel input.
	SEG24	AN		LCD Analog output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RF7/HIDF7/C2IN3-/C1IN3-/ANF7/SS(1)/SEG25	RF7	TTL/ST	CMOS/OD	General purpose I/O.
	HIDF7	TTL/ST		High current output.
	C2IN3-	AN		Comparator negative input.
	C1IN3-	AN		Comparator negative input.
	ANF7	AN		ADC Channel input.
	SS(1)	—		MSSP SPI slave select input.
	SEG25	AN		LCD Analog output.
RG0/ANG0/SEG42	RG0	TTL/ST	CMOS/OD	General purpose I/O.
	ANG0	AN		ADC Channel input.
	SEG42	AN		LCD Analog output.
RG1/ANG1/CK2(3)/TX2(1)/SEG43	RG1	TTL/ST	CMOS/OD	General purpose I/O.
	ANG1	AN		ADC Channel input.
	CK2(3)	—		EUSART synchronous clock out.
	TX2(1)	—		EUSART asynchronous TX data out.
	SEG43	AN		LCD Analog output.
RG2/ANG2/DK2(3)/RX2(1)/SEG44	RG2	TTL/ST	CMOS/OD	General purpose I/O.
	ANG2	AN		ADC Channel input.
	DK2(3)	—		EUSART synchronous data output.
	RX2(1)	—		EUSART receive input.
	SEG44	AN		LCD Analog output.
RG3/ANG3/SEG45	RG3	TTL/ST	CMOS/OD	General purpose I/O.
	ANG3	AN		ADC Channel input.
	SEG45	AN		LCD Analog output.
RG4/ANG4/SEG26	RG4	TTL/ST	CMOS/OD	General purpose I/O.
	ANG4	AN		ADC Channel input.
	SEG26	AN		LCD Analog output.
RG5/IOCG5/$\overline{MCLR}$/VPP	RG5	TTL/ST	CMOS/OD	General purpose I/O.
	IOCG5	TTL/ST		Interrupt-on-change input.
	$\overline{MCLR}$	ST		Master clear input with internal weak pull up resistor.
	VPP	—	—	ICSP™ High-Voltage Programming mode entry input.
RG6/ANG6/COM6	RG6	TTL/ST	CMOS/OD	General purpose I/O.
	ANG6	AN		ADC Channel input.
	COM6	AN		LCD Driver Common Outputs.
RG7/ANG7/COM7/SEG15	RG7	TTL/ST	CMOS/OD	General purpose I/O.
	ANG7	AN		ADC Channel input.
	COM7	AN		LCD Driver Common Outputs.
	SEG15	AN		LCD Analog output.
RH0/COM4	RH0	TTL/ST	CMOS/OD	General purpose I/O.
	COM4	AN		LCD Driver Common Outputs.
RH1/COM5/ADCACT(1)	RH1	TTL/ST	CMOS/OD	General purpose I/O.
	COM5	AN		LCD Driver Common Outputs.
	ADCACT(1)	TTL/ST	—	ADC Auto-Conversion Trigger input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RH2/SEG32/CFLY1	RH2	TTL/ST	CMOS/OD	General purpose I/O.
	SEG32	AN		LCD Analog output.
	CFLY1	AN		LCD Drive Charge Pump Capacitor Inputs.
RH3/SEG40/CFLY2	RH3	TTL/ST	CMOS/OD	General purpose I/O.
	SEG40	AN		LCD Analog output.
	CFLY2	AN		LCD Drive Charge Pump Capacitor Inputs.
VLCD3	VLCD3	AN	—	LCD analog input.
V_{DD}	V_{DD}	Power	P	Positive supply voltage input.
V_{SS}	V_{DD}	Power	P	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

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4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1OUT	—	CMOS/OD	Comparator 1 output.
	C2OUT	—	CMOS/OD	Comparator 2 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	ADGRDA	—	CMOS/OD	ADC Guard Ring A output.
	ADGRDB	—	CMOS/OD	ADC Guard Ring B output.
	TX1	—	CMOS/OD	EUSART1 Asynchronous mode transmitter data output.
	CK1(3)	—	CMOS/OD	EUSART1 Synchronous mode clock output.
	TX2	—	CMOS/OD	EUSART2 Asynchronous mode transmitter data output.
	CK2(3)	—	CMOS/OD	EUSART2 Synchronous mode clock output.
	DT(3)	—	CMOS/OD	EUSART Synchronous mode data output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	CCP2 output (compare/PWM functions).
	CCP2	—	CMOS/OD	CCP2 output (compare/PWM functions).
	PWM3OUT	—	CMOS/OD	PWM3 output.
	PWM4OUT	—	CMOS/OD	PWM4 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
	CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.
	RTCC	—	CMOS/OD	RTCC Second Clock output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

2.0 GUIDELINES FOR GETTING STARTED WITH PIC16(L)F19195/6/7 MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC16(L)F19195/6/7 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Power Supply Pins"**)
- MCLR pin (when configured for external operation) (see **Section 2.3 "Master Clear (MCLR) Pin"**)

These pins must also be connected if they are being used in the end application:

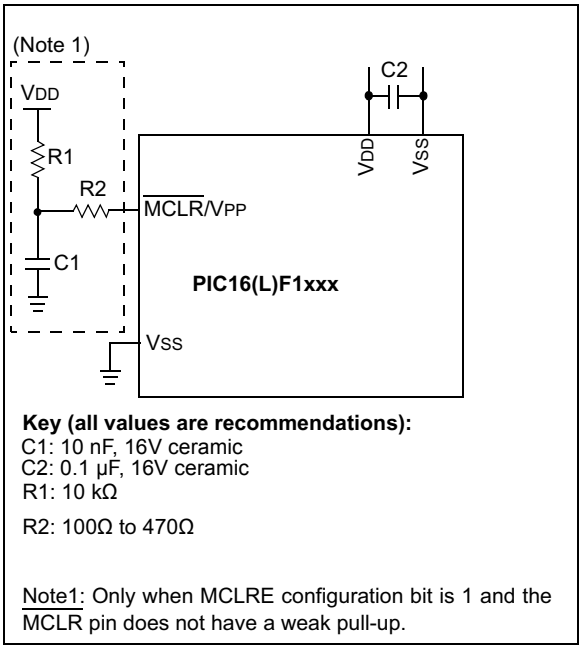
- ICSPCLK/ICSPDAT pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.4 "ICSP™ Pins"**)
- OSC1, OSC2, SOSCO and SOSCI pins when an external oscillator source is used (see **Section 2.5 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+ pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):
C1: 10 nF, 16V ceramic
C2: 0.1 µF, 16V ceramic
R1: 10 kΩ
R2: 100Ω to 470Ω

Note1: Only when MCLRE configuration bit is 1 and the MCLR pin does not have a weak pull-up.

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins (VDD and VSS) is required. All VDD and VSS pins must be connected. None can be left floating.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 µF (100 nF), 10-25V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 µF in parallel with 0.001 µF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides three specific device functions:

- Device Reset (when MCLRE = 1)
- Digital input pin (when MCLRE = 0)
- Device Programming and Debugging

If programming and debugging are not required in the end application then either set the MCLRE Configuration bit to '1' and use the pin as a digital input or clear the MCLRE Configuration bit and leave the pin open to use the internal weak pull-up. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, the programmer $\overline{MCLR}/V_{PP}$ output should be connected directly to the pin so that R1 isolates the capacitor, C1 from the $\overline{MCLR}$ pin during programming and debugging operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

2.4 ICSP™ Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be isolated from the programmer by resistors between the application and the device pins or removed from the circuit during programming. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/ emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 41.0 "Development Support"**.

2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-2. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

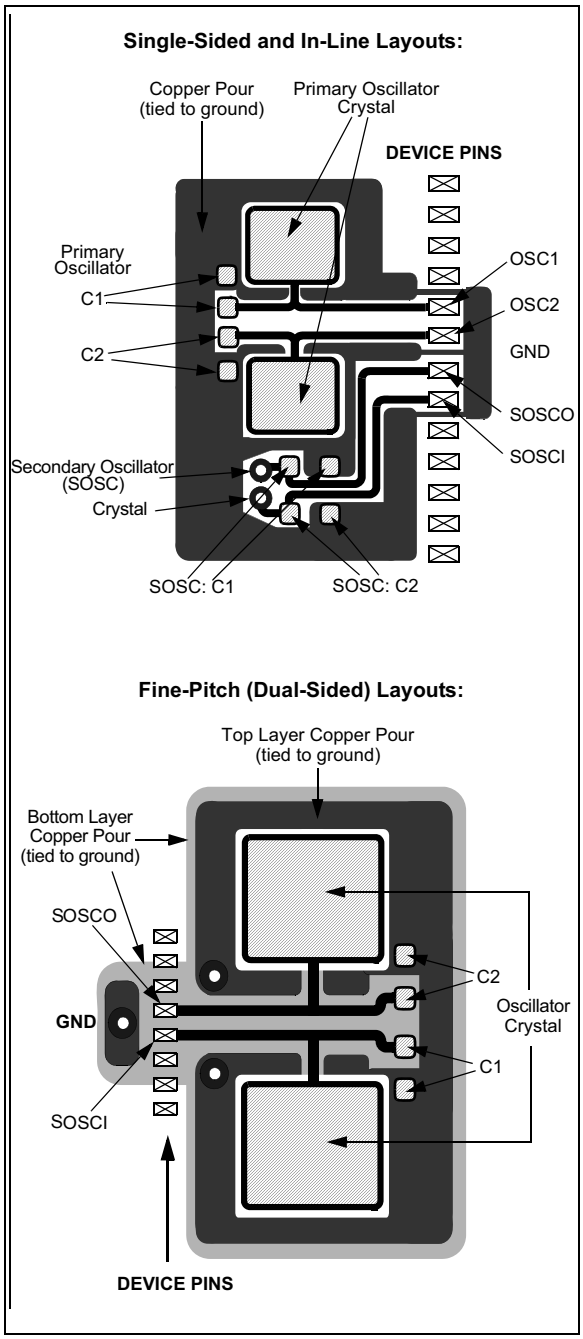
For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- AN826, *"Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- AN849, *"Basic PICmicro® Oscillator Design"*
- AN943, *"Practical PICmicro® Oscillator Analysis and Design"*
- AN949, *"Making Your Oscillator Work"*

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output logic low.

FIGURE 2-2: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



3.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 48 instructions. Interrupt capability includes automatic context saving.

The hardware stack is 16-levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

FIGURE 3-1: CORE DATA PATH DIAGRAM