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PIC16(L)F1946/47

64-Pin Flash-Based, 8-Bit CMOS Microcontrollers with LCD Driver and XLP Technology

High-Performance RISC CPU

- Only 49 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 32 MHz oscillator/clock input
  - DC – 125 ns instruction cycle
- Up to 16K x 14 Words of Flash Program Memory
- Up to 1024 Bytes of Data Memory (RAM)
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes
- Processor Read Access to Program Memory

Special Microcontroller Features

- Precision Internal Oscillator:
  - Factory-calibrated to ±1%, typical
  - Software-selectable frequency range from 32 MHz to 31 kHz
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR):
  - Selectable between two trip points
  - Disable in Sleep option
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- High Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years
- Wide Operating Voltage Range:
  - 1.8V-5.5V (PIC16F1946/47)
  - 1.8V-3.6V (PIC16LF1946/47)

PIC16LF1946/47 Low-Power Features

- Standby Current:
  - 60 nA @ 1.8V, typical
- Operating Current:
  - 7.0 μA @ 32 kHz, 1.8V, typical
  - 35 μA/MHz, 1.8V, typical
- Timer1 Oscillator Current:
  - 600 nA @ 32 kHz, 1.8V, typical
- Low-Power Watchdog Timer Current:
  - 500 nA @ 1.8V, typical

Peripheral Features

- 54 I/O Pins (One Input-only pin):
  - High-current source/sink for direct LED drive
  - Individually programmable Interrupt-on-pin change pins
  - Individually programmable weak pull-ups
- Integrated LCD Controller:
  - Up to 184 segments
  - Variable clock input
  - Contrast control
  - Internal voltage reference selections
- Capacitive Sensing (CSM) Module (mTouch®):
  - 17 selectable channels
- A/D Converter:
  - 10-bit resolution and 17 channels
  - Selectable 1.024/2.048/4.096V voltage reference
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - Dedicated low-power 32 kHz oscillator driver
  - 16-bit timer/counter with prescaler
  - External Gate Input mode with toggle and single shot modes
  - Interrupt-on-gate completion
- Timer2, 4, 6: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture, Compare, PWM Modules (CCP):
  - 16-bit Capture, max. resolution 125 ns
  - 16-bit Compare, max. resolution 125 ns
  - 10-bit PWM, max. frequency 31.25 kHz
- Three Enhanced Capture, Compare, PWM Modules (ECCP):
  - Three PWM time-base options
  - Auto-shutdown and auto-restart
  - PWM steering
  - Programmable dead-band delay

Peripheral Features (Continued)

- Two Master Synchronous Serial Ports (MSSPs) with SPI and I^2C with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
  - Auto-wake-up on start
- Two Enhanced Universal Synchronous: Asynchronous Receiver Transmitters (EUSARTs)
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
- SR Latch (555 Timer):
  - Multiple Set/Reset input options
  - Emulates 555 Timer applications
- Three Comparators:
  - Rail-to-rail inputs/outputs
  - Power mode control
  - Software enable hysteresis
- Voltage Reference Module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

PIC16(L)F193X/194X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	Data SRAM (bytes)	I/Os(2)	10-bit ADC (ch)	CapSense (ch)	Comparators	Timers (8/16-bit)	EUSART	MSSP (I^2C/SPI)	ECCP	CCP	LCD (Com/Seg/Total)	Debug(1)	XLP
PIC16(L)F1933	(1)	4096	256	256	25	11	8	2	4/1	1	1	3	2	4/16/60(3)	I/H	Y
PIC16(L)F1934	(2)	4096	256	256	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H	Y
PIC16(L)F1936	(2)	8192	256	512	25	11	8	2	4/1	1	1	3	2	4/16/60(3)	I/H	Y
PIC16(L)F1937	(2)	8192	256	512	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H	Y
PIC16(L)F1938	(3)	16384	256	1024	25	11	8	2	4/1	1	1	3	2	4/16/60(3)	I/H	Y
PIC16(L)F1939	(3)	16384	256	1024	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H	Y
PIC16(L)F1946	(4)	8192	256	512	54	17	17	3	4/1	2	2	3	2	4/46/184	I	Y
PIC16(L)F1947	(4)	16384	256	1024	54	17	17	3	4/1	2	2	3	2	4/46/184	I	Y

Note 1: I – Debugging, Integrated on Chip; H – Debugging, Requires Debug Header.

2: One pin is input-only.

3: COM3 and SEG15 share the same physical pin, therefore SEG15 is not available when using 1/4 multiplex displays.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS41575 PIC16(L)F1933 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.

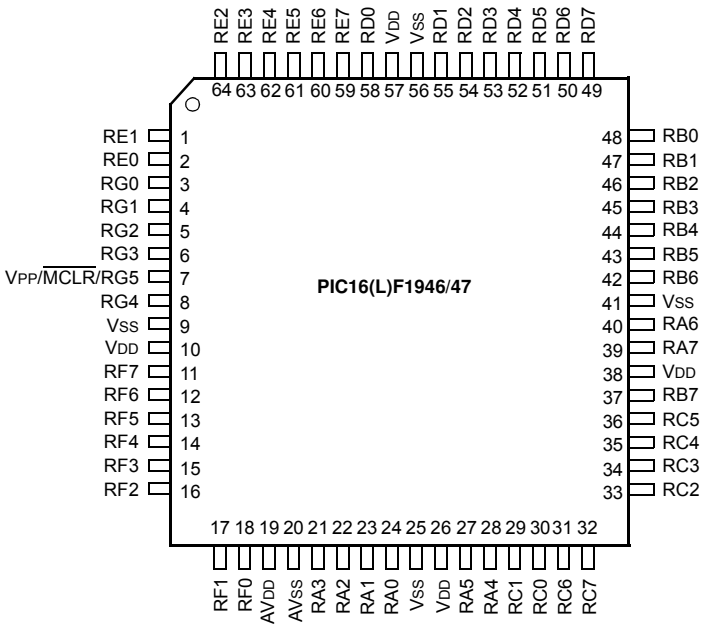
2: DS41364 PIC16(L)F1934/6/7 Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers.

3: DS40001574 PIC16(L)F1938/9 Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers.

4: DS41414 PIC16(L)F1946/1947 Data Sheet, 64-Pin Flash, 8-bit Microcontrollers.

Pin Diagram – 64-Pin TQFP/QFN (PIC16(L)F1946/47)

64-pin TQFP, QFN



Note 1: Pin location selected by APFCON register setting. Default location.

2: Pin function can be moved using the APFCON register. Alternate location.

3: QFN package orientation is the same. No leads are present on the QFN package.

Note: AVDD and AVSS are dedicated power connection pins for the on-board analog circuits of the PIC® microcontroller. The separate power pins help eliminate digital switching noise interference with the analog circuitry inside the device, especially on larger devices with more I/O pins and larger switching currents on the VDD/VSS pins. Customers typically connect these to the appropriate VDD or VSS connections on the PCB, unless there is a lot of noise on the external power rails. In those situations, they will add additional noise filtering components (like capacitors) on the AVDD/AVSS pins to help ensure good solid supply to the analog modules inside the device.

TABLE 1: 64-PIN SUMMARY(PIC16(L)F1946/47)

I/O	64-Pin TQFP, QFN	ANSEL	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	CCP	USART	MSSP	LCD	Interrupt	Pull-up	Basic
RA0	24	Y	AN0	—	CPS0	—	—	—	—	—	—	SEG33	—	—	—
RA1	23	Y	AN1	—	CPS1	—	—	—	—	—	—	SEG18	—	—	—
RA2	22	Y	AN2	VREF-	CPS2	—	—	—	—	—	—	SEG34	—	—	—
RA3	21	Y	AN3	VREF+	CPS3	—	—	—	—	—	—	SEG35	—	—	—
RA4	28	—	—	—	—	—	—	T0CKI	—	—	—	SEG14	—	—	—
RA5	27	Y	AN4	—	CPS4	—	—	—	—	—	—	SEG15	—	—	—
RA6	40	—	—	—	—	—	—	—	—	—	—	SEG36	—	—	OSC2/ CLKOUT
RA7	39	—	—	—	—	—	—	—	—	—	—	SEG37	—	—	OSC1/ CLKIN
RB0	48	—	—	—	—	—	SRI	—	FLT0	—	—	SEG30	INT/ IOC	Y	—
RB1	47	—	—	—	—	—	—	—	—	—	—	SEG8	IOC	Y	—
RB2	46	—	—	—	—	—	—	—	—	—	—	SEG9	IOC	Y	—
RB3	45	—	—	—	—	—	—	—	—	—	—	SEG10	IOC	Y	—
RB4	44	—	—	—	—	—	—	—	—	—	—	SEG11	IOC	Y	—
RB5	43	—	—	—	—	—	—	T1G	—	—	—	SEG29	IOC	Y	—
RB6	42	—	—	—	—	—	—	—	—	—	—	SEG38	IOC	Y	ICSP-CLK/ ICDCLK
RB7	37	—	—	—	—	—	—	—	—	—	—	SEG39	IOC	Y	ICSP-DAT/ ICDDAT
RC0	30	—	—	—	—	—	—	T1OSO/ T1CKI	—	—	—	SEG40	—	—	—
RC1	29	—	—	—	—	—	—	T1OSI	CCP2(1)/ P2A(1)	—	—	SEG32	—	—	—
RC2	33	—	—	—	—	—	—	—	CCP1/ P1A	—	—	SEG13	—	—	—
RC3	34	—	—	—	—	—	—	—	—	—	SCK1/ SCL1	SEG17	—	—	—
RC4	35	—	—	—	—	—	—	—	—	—	SDI1/ SDA1	SEG16	—	—	—
RC5	36	—	—	—	—	—	—	—	—	—	SDO1	SEG12	—	—	—
RC6	31	—	—	—	—	—	—	—	—	TX1/ CK1	—	SEG27	—	—	—
RC7	32	—	—	—	—	—	—	—	—	RX1/ DT1	—	SEG28	—	—	—
RD0	58	—	—	—	—	—	—	—	P2D(2)	—	—	SEG0	—	—	—
RD1	55	—	—	—	—	—	—	—	P2C(2)	—	—	SEG1	—	—	—
RD2	54	—	—	—	—	—	—	—	P2B(2)	—	—	SEG2	—	—	—
RD3	53	—	—	—	—	—	—	—	P3C(2)	—	—	SEG3	—	—	—
RD4	52	—	—	—	—	—	—	—	P3B(2)	—	SDO2	SEG4	—	—	—
RD5	51	—	—	—	—	—	—	—	P1C(2)	—	SDI2 SDA2	SEG5	—	—	—
RD6	50	—	—	—	—	—	—	—	P1B(2)	—	SCK2/ SCL2	SEG6	—	—	—
RD7	49	—	—	—	—	—	—	—	—	—	$\overline{SS2}$	SEG7	—	—	—

Note 1: Pin functions can be moved using the APFCON register(s). Default location.

2: Pin function can be moved using the APFCON register. Alternate location.

3: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

4: See **Section 8.0 "Low Dropout (LDO) Voltage Regulator"**.

TABLE 1: 64-PIN SUMMARY(PIC16(L)F1946/47) (Continued)

I/O	64-Pin TQFP, QFN	ANSEL	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	CCP	USART	MSSP	LCD	Interrupt	Pull-up	Basic
RE0	2	Y	—	—	—	—	—	—	P2D(1)	—		VLCD1	—	—	—
RE1	1	Y	—	—	—	—	—	—	P2C(1)	—	—	VLCD2	—	—	—
RE2	64	Y	—	—	—	—	—	—	P2B(1)	—	—	VLCD3	—	—	—
RE3	63	—	—	—	—	—	—	—	P3C(1)	—	—	COM0	—	—	—
RE4	62	—	—	—	—	—	—	—	P3B(1)	—	—	COM1	—	—	—
RE5	61	—	—	—	—	—	—	—	P1C(1)	—	—	COM2	—	—	—
RE6	60	—	—	—	—	—	—	—	P1B(1)	—	—	COM3	—	—	—
RE7	59	—	—	—	—	—	—	—	CCP2(2)/ P2A(2)	—	—	SEG31	—	—	—
RF0	18	Y	AN16	—	CPS16	C1IN0- C2IN0-	—	—	—	—	—	SEG41	—	—	VCAP(4)
RF1	17	Y	AN6	—	CPS6	C2OUT	SRNQ	—	—	—	—	SEG19	—	—	—
RF2	16	Y	AN7	—	CPS7	C1OUT	SRQ	—	—	—	—	SEG20	—	—	—
RF3	15	Y	AN8		CPS8	C1IN2- C2IN2- C3IN2-	—	—	—	—	—	SEG21	—	—	—
RF4	14	Y	AN9	—	CPS9	C2IN+	—	—	—	—	—	SEG22	—	—	—
RF5	13	Y	AN10	DACOUT	CPS10	C1IN1- C2IN1-	—		—	—	—	SEG23	—	—	—
RF6	12	Y	AN11	—	CPS11	C1IN+	—	—	—	—	—	SEG24	—	—	—
RF7	11	Y	AN5	—	CPS5	C1IN3- C2IN3- C3IN3-	—	—	—	—	$\overline{SS1}$	SEG25	—	—	—
RG0	3	—	—	—	—	—	—	—	CCP3 P3A	—	—	SEG42	—	—	—
RG1	4	Y	AN15	—	CPS15	C3OUT	—	—	—	TX2/ CK2	—	SEG43	—	—	—
RG2	5	Y	AN14	—	CPS14	C3IN+	—	—	—	RX2/ DT2	—	SEG44	—	—	—
RG3	6	Y	AN13	—	CPS13	C3IN0-	—	—	CCP4 P3D	—	—	SEG45	—	—	—
RG4	8	Y	AN12	—	CPS12	C3IN1-	—	—	CCP5 P1D	—	—	SEG26	—	—	—
RG5	7	—	—	—	—	—	—	—	—	—	—	—	—	Y(3)	$\overline{MCLR}$/VPP
VDD	10 26 38 57	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	9 25 41 56	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
AVDD	19	—	—	—	—	—	—	—	—	—	—	—	—	—	AVDD
AVSS	20	—	—	—	—	—	—	—	—	—	—	—	—	—	AVSS

Note 1: Pin functions can be moved using the APFCON register(s). Default location.

2: Pin function can be moved using the APFCON register. Alternate location.

3: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

4: See **Section 8.0 "Low Dropout (LDO) Voltage Regulator"**.

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1.0 DEVICE OVERVIEW

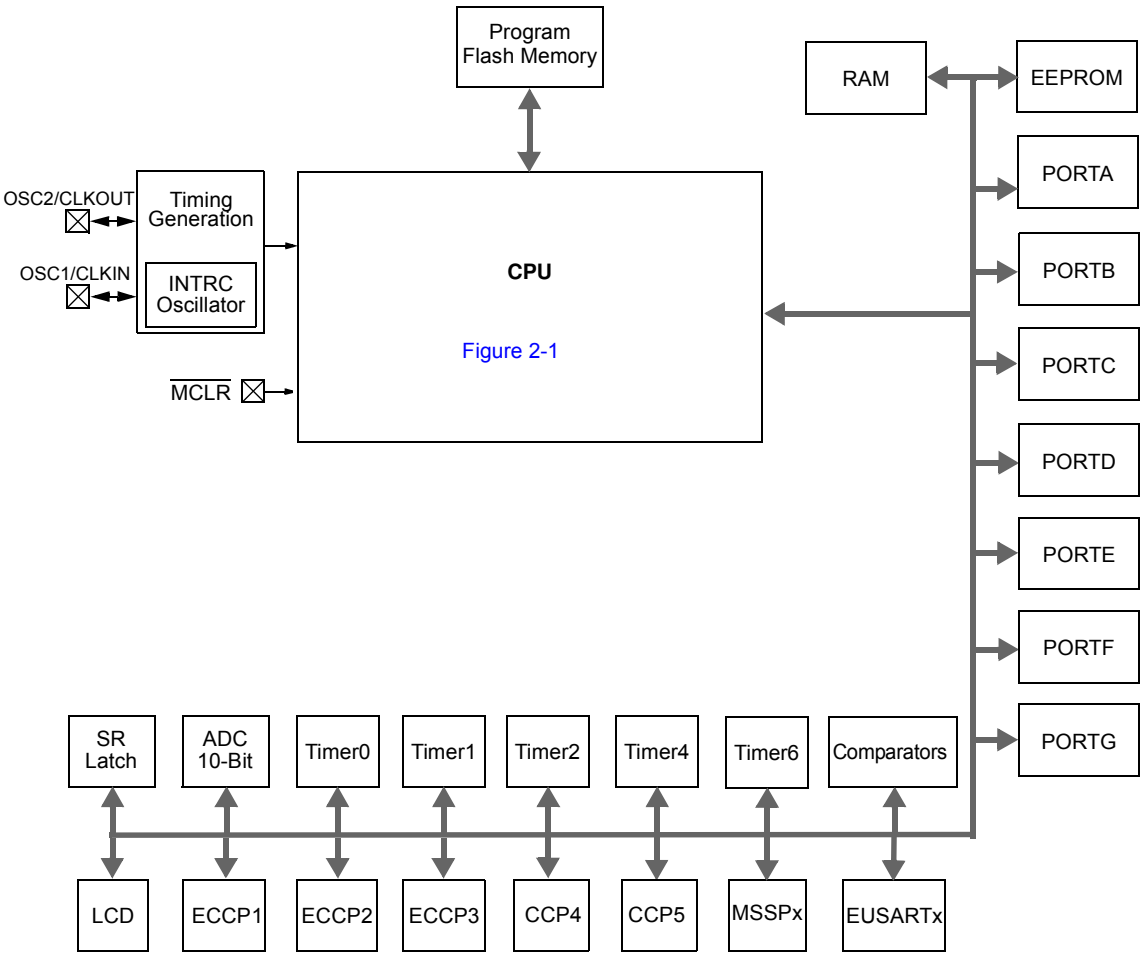
The PIC16(L)F1946/47 are described within this data sheet. They are available in 64-pin packages. Figure 1-1 shows a block diagram of the PIC16(L)F1946/47 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1946	PIC16(L)F1947
ADC		●	●
Capacitive Sensing (CPS) Module		●	●
Data EEPROM		●	●
Digital-to-Analog Converter (DAC)		●	●
Fixed Voltage Reference (FVR)		●	●
LCD		●	●
SR Latch		●	●
Capture/Compare/PWM Modules			
	ECCP1	●	●
	ECCP2	●	●
	ECCP3	●	●
	CCP4	●	●
	CCP5	●	●
Comparators			
	C1	●	●
	C2	●	●
	C3	●	●
EUSARTS			
	EUSART1	●	●
	EUSART2	●	●
Master Synchronous Serial Ports			
	MSSP1	●	●
	MSSP2	●	●
Timers			
	Timer0	●	●
	Timer1	●	●
	Timer2	●	●
	Timer4	●	●
	Timer6	●	●

FIGURE 1-1: PIC16(L)F1946/47 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1946/47 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/SEG33	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel input.
	CPS0	AN	—	Capacitive sensing input 0.
	SEG33	—	AN	LCD Analog output.
RA1/AN1/CPS1/SEG18	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel input.
	CPS1	AN	—	Capacitive sensing input.
	SEG18	—	AN	LCD Analog output.
RA2/AN2/VREF-/CPS2/SEG34	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel input.
	VREF-	AN	—	A/D Negative Voltage Reference input.
	CPS2	AN	—	Capacitive sensing input.
	SEG34	—	AN	LCD Analog output.
RA3/AN3/VREF+/CPS3/SEG35	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel input.
	VREF+	AN	—	A/D Voltage Reference input.
	CPS3	AN	—	Capacitive sensing input.
	SEG35	—	AN	LCD Analog output.
RA4/T0CKI/SEG14	RA4	TTL	CMOS	General purpose I/O.
	T0CKI	ST	—	Timer0 clock input.
	SEG14	—	AN	LCD Analog output.
RA5/AN4/CPS4/SEG15	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel input.
	CPS4	AN	—	Capacitive sensing input.
	SEG15	—	AN	LCD Analog output.
RA6/OSC2/CLKOUT/SEG36	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	SEG36	—	AN	LCD Analog output.
RA7/OSC1/CLKIN/SEG37	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	SEG37	—	AN	LCD Analog output.
RB0/INT/SRI/FLT0/SEG30	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	INT	ST	—	External interrupt.
	SRI	—	ST	SR Latch input.
	FLT0	ST	—	ECCP Auto-shutdown Fault input.
	SEG30	—	AN	LCD analog output.
RB1/SEG8	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	SEG8	—	AN	LCD Analog output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin function is selectable via the APFCON register.

TABLE 1-2: PIC16(L)F1946/47 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB2/SEG9	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	SEG9	—	AN	LCD Analog output.
RB3/SEG10	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	SEG10	—	AN	LCD Analog output.
RB4/SEG11	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	SEG11	—	AN	LCD Analog output.
RB5/T1G/SEG29	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	T1G	ST	—	Timer1 Gate input.
	SEG29	—	AN	LCD Analog output.
RB6/ICSPCLK/ICDCLK/SEG38	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
	SEG38	—	AN	LCD Analog output.
RB7/ICSPDAT/ICDDAT/SEG39	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
	SEG39	—	AN	LCD Analog output.
RC0/T1OSO/T1CKI/SEG40	RC0	ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
	SEG40	—	AN	LCD Analog output.
RC1/T1OSI/P2A(1)/CCP2(1)/ SEG32	RC1	ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	P2A	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM.
	SEG32	—	AN	LCD Analog output.
RC2/CCP1/P1A/SEG13	RC2	ST	CMOS	General purpose I/O.
	CCP1	ST	CMOS	Capture/Compare/PWM.
	P1A	—	CMOS	PWM output.
	SEG13	—	AN	LCD Analog output.
RC3/SCK1/SCL1/SEG17	RC3	ST	CMOS	General purpose I/O.
	SCK1	ST	CMOS	SPI clock.
	SCL1	I^2C	OD	I^2C clock.
	SEG17	—	AN	LCD Analog output.
RC4/SDI1/SDA1/SEG16	RC4	ST	CMOS	General purpose I/O.
	SDI1	ST	—	SPI data input.
	SDA1	I^2C	OD	I^2C data input/output.
	SEG16	—	AN	LCD Analog output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin function is selectable via the APFCON register.

TABLE 1-2: PIC16(L)F1946/47 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC5/SDO1/SEG12	RC5	ST	CMOS	General purpose I/O.
	SDO1	—	CMOS	SPI data output.
	SEG12	—	AN	LCD Analog output.
RC6/TX1/CK1/SEG27	RC6	ST	CMOS	General purpose I/O.
	TX1	—	CMOS	USART1 asynchronous transmit.
	CK1	ST	CMOS	USART1 synchronous clock.
	SEG27	—	AN	LCD Analog output.
RC7/RX1/DT1/SEG28	RC7	ST	CMOS	General purpose I/O.
	RX1	ST	—	USART1 asynchronous input.
	DT1	ST	CMOS	USART1 synchronous data.
	SEG28	—	AN	LCD Analog output.
RD0/P2D(1)/SEG0	RD0	ST	CMOS	General purpose I/O.
	P2D	—	CMOS	PWM output.
	SEG0	—	AN	LCD Analog output.
RD1/P2C(1)/SEG1	RD1	ST	CMOS	General purpose I/O.
	P2C	—	CMOS	PWM output.
	SEG1	—	AN	LCD Analog output.
RD2/P2B(1)/SEG2	RD2	ST	CMOS	General purpose I/O.
	P2B	—	CMOS	PWM output.
	SEG2	—	AN	LCD Analog output.
RD3/P3C(1)/SEG3	RD3	ST	CMOS	General purpose I/O.
	P3C	—	CMOS	PWM output.
	SEG3	—	AN	LCD analog output.
RD4/SDO2/P3B(1)/SEG4	RD4	ST	CMOS	General purpose I/O.
	SDO2	—	CMOS	SPI data output.
	P3B	—	CMOS	PWM output.
	SEG4	—	AN	LCD analog output.
RD5/SDI2/SDA2/P1C(1)/SEG5	RD5	ST	CMOS	General purpose I/O.
	SDI2	ST	—	SPI data input.
	SDA2	I^2C	OD	I^2C data input/output.
	P1C	—	CMOS	PWM output.
	SEG5	—	AN	LCD analog output.
RD6/SCK2/SCL2/P1B(1)/SEG6	RD6	ST	CMOS	General purpose I/O.
	SCK2	ST	CMOS	SPI clock.
	SCL2	I^2C	OD	I^2C clock.
	P1B	—	CMOS	PWM output.
	SEG6	—	AN	LCD analog output.
RD7/$\overline{SS2}$/SEG7	RD7	ST	CMOS	General purpose I/O.
	$\overline{SS2}$	ST	—	Slave Select input.
	SEG7	—	AN	LCD analog output.
RE0/P2D(1)/VLCD1	RE0	ST	CMOS	General purpose I/O.
	P2D	—	CMOS	PWM output.
	VLCD1	AN	—	LCD analog input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin function is selectable via the APFCON register.

TABLE 1-2: PIC16(L)F1946/47 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RE1/P2C(1)/VLCD2	RE1	ST	CMOS	General purpose I/O.
	P2C	—	CMOS	PWM output.
	VLCD2	AN	—	LCD analog input.
RE2/P2B(1)/VLCD3	RE2	ST	CMOS	General purpose I/O.
	P2B	—	CMOS	PWM output.
	VLCD3	AN	—	LCD analog input.
RE3/P3C(1)/COM0	RE3	ST	CMOS	General purpose I/O.
	P3C	—	CMOS	PWM output.
	COM0	—	AN	LCD Analog output.
RE4/P3B(1)/COM1	RE4	ST	CMOS	General purpose I/O.
	P3B	—	CMOS	PWM output.
	COM1	—	AN	LCD Analog output.
RE5/P1C(1)/COM2	RE5	ST	CMOS	General purpose I/O.
	P1C	—	CMOS	PWM output.
	COM2	—	AN	LCD Analog output.
RE6/P1B(1)/COM3	RE6	ST	—	General purpose I/O.
	P1B	—	CMOS	PWM output.
	COM3	—	AN	LCD Analog output.
RE7/CCP2(1)/P2A(1)/SEG31	RE7	ST	CMOS	General purpose I/O.
	CCP2	ST	CMOS	Capture/Compare/PWM.
	P2A	—	CMOS	PWM output.
	SEG31	—	AN	LCD analog output.
RF0/AN16/CPS16/C1IN0-/C2IN0 /SEG41/VCAP	RF0	ST	CMOS	General purpose I/O.
	AN16	AN	—	A/D Channel input.
	CPS16	AN	—	Capacitive sensing input.
	C1IN0-	AN	—	Comparator negative input.
	C2IN0-	AN	—	Comparator negative input.
	SEG41	—	AN	LCD Analog output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator.
RF1/AN6/CPS6/C2OUT/SRNQ/ SEG19	RF1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel input.
	CPS6	AN	—	Capacitive sensing input.
	C2OUT	—	CMOS	Comparator output.
	SRNQ	—	CMOS	SR Latch inverting output.
	SEG19	—	AN	LCD Analog output.
RF2/AN7/CPS7/C1OUT/SRQ/ SEG20	RF2	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel input.
	CPS7	AN	—	Capacitive sensing input.
	C1OUT	—	CMOS	Comparator output.
	SRQ	—	CMOS	SR Latch non-inverting output.
	SEG20	—	AN	LCD Analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin function is selectable via the APFCON register.

TABLE 1-2: PIC16(L)F1946/47 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RF3/AN8/CPS8/C123IN2-/ SEG21	RF3	ST	CMOS	General purpose I/O.
	AN8	AN	—	A/D Channel input.
	CPS8	AN	—	Capacitive sensing input.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
	C3IN2-	AN	—	Comparator negative input.
	SEG21	—	AN	LCD Analog output.
RF4/AN9/CPS9/C2IN+/SEG22	RF4	ST	CMOS	General purpose I/O.
	AN9	AN	—	A/D Channel input.
	CPS9	AN	—	Capacitive sensing input.
	C2IN+	AN	—	Comparator positive input.
	SEG22	—	AN	LCD Analog output.
RF5/AN10/CPS10/C12IN1-/ DACOUT/SEG23	RF5	ST	CMOS	General purpose I/O.
	AN10	AN	—	A/D Channel input.
	CPS10	AN	—	Capacitive sensing input.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
	DACOUT	—	AN	Voltage Reference output.
	SEG23	—	AN	LCD Analog output.
RF6/AN11/CPS11/C1IN+/SEG24	RF6	ST	CMOS	General purpose I/O.
	AN11	AN	—	A/D Channel input.
	CPS11	AN	—	Capacitive sensing input.
	C1IN+	AN	—	Comparator positive input.
	SEG24	—	AN	LCD Analog output.
RF7/AN5/CPS5/C123IN3-/$\overline{SS1}$/ SEG25	RF7	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel input.
	CPS5	AN	—	Capacitive sensing input.
	C1IN3-	AN	—	Comparator negative input.
	C2IN3-	AN	—	Comparator negative input.
	C3IN3-	AN	—	Comparator negative input.
	$\overline{SS1}$	ST	—	Slave Select input.
	SEG25	—	AN	LCD Analog output.
RG0/CCP3/P3A/SEG42	RG0	ST	CMOS	General purpose I/O.
	CCP3	ST	CMOS	Capture/Compare/PWM.
	P3A	—	CMOS	PWM output.
	SEG42	—	AN	LCD Analog output.
RG1/AN15/CPS15/TX2/CK2/ C3OUT/SEG43	RG1	ST	CMOS	General purpose I/O.
	AN15	AN	—	A/D Channel input.
	CPS15	AN	—	Capacitive sensing input.
	TX2	—	CMOS	USART2 asynchronous transmit.
	CK2	ST	CMOS	USART2 synchronous clock.
	C3OUT	—	CMOS	Comparator output.
	SEG43	—	AN	LCD Analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin function is selectable via the APFCON register.

TABLE 1-2: PIC16(L)F1946/47 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RG2/AN14/CPS14/RX2/DT2/ C3IN+/SEG44	RG2	ST	CMOS	General purpose I/O.
	AN14	AN	—	A/D Channel input.
	CPS14	AN	—	Capacitive sensing input.
	RX2	ST	—	USART2 asynchronous input.
	DT2	ST	CMOS	USART2 synchronous data.
	C3IN+	AN	—	Comparator positive input.
	SEG44	—	AN	LCD Analog output.
RG3/AN13/CPS13/C3IN0-/ CCP4/P3D/SEG45	RG3	ST	CMOS	General purpose I/O.
	AN13	AN	—	A/D Channel input.
	CPS13	AN	—	Capacitive sensing input.
	C3IN0-	AN	—	Comparator negative input.
	CCP4	ST	CMOS	Capture/Compare/PWM.
	P3D	—	CMOS	PWM output.
	SEG45	—	AN	LCD Analog output.
RG4/AN12/CPS12/C3IN1-/ CCP5/P1D/SEG26	RG4	ST	CMOS	General purpose I/O.
	AN12	AN	—	A/D Channel input.
	CPS12	AN	—	Capacitive sensing input.
	C3IN1-	AN	—	Comparator negative input.
	CCP5	ST	CMOS	Capture/Compare/PWM.
	P1D	—	CMOS	PWM output.
	SEG26	—	AN	LCD Analog output.
RG5/$\overline{\text{MCLR}}$/V_{PP}	RG5	ST	—	General purpose input.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	V_{PP}	HV	—	Programming voltage.
V_{DD}	V_{DD}	Power	—	Positive supply.
V_{SS}	V_{SS}	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin function is selectable via the APFCON register.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15-bit wide and 16-word deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See section **Section 3.5 "Stack"** for more details.

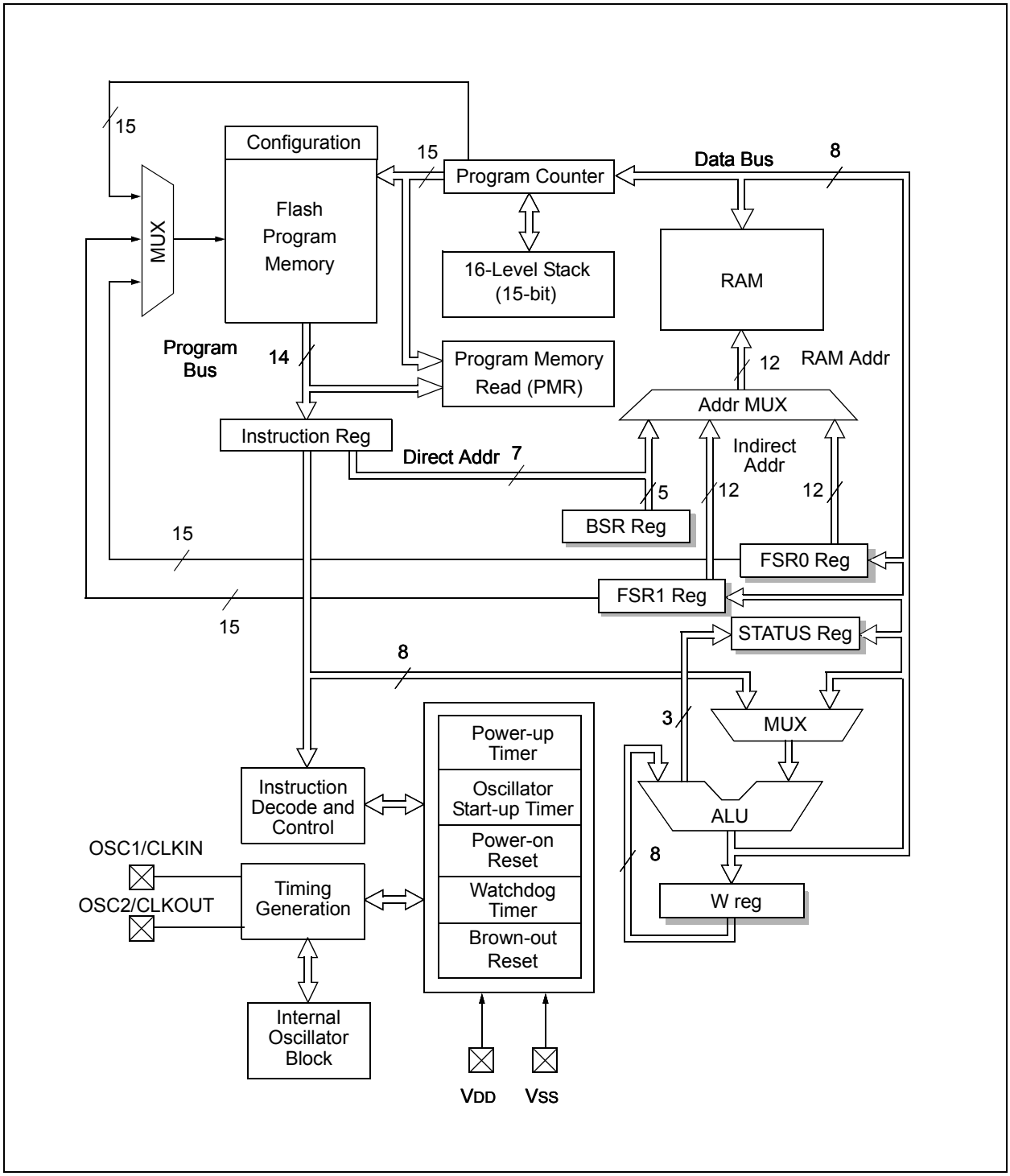
2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, one additional instruction cycle is required to fetch the data at that address. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.6 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 29.0 "Instruction Set Summary"** for more details.

FIGURE 2-1: CORE BLOCK DIAGRAM



3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
- Data EEPROM memory(1)

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in **Section 11.0 "Data EEPROM and Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1946/47 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1 and 3-2).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
PIC16(L)F1946	8,192	1FFFh
PIC16(L)F1947	16,384	3FFFh

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1946

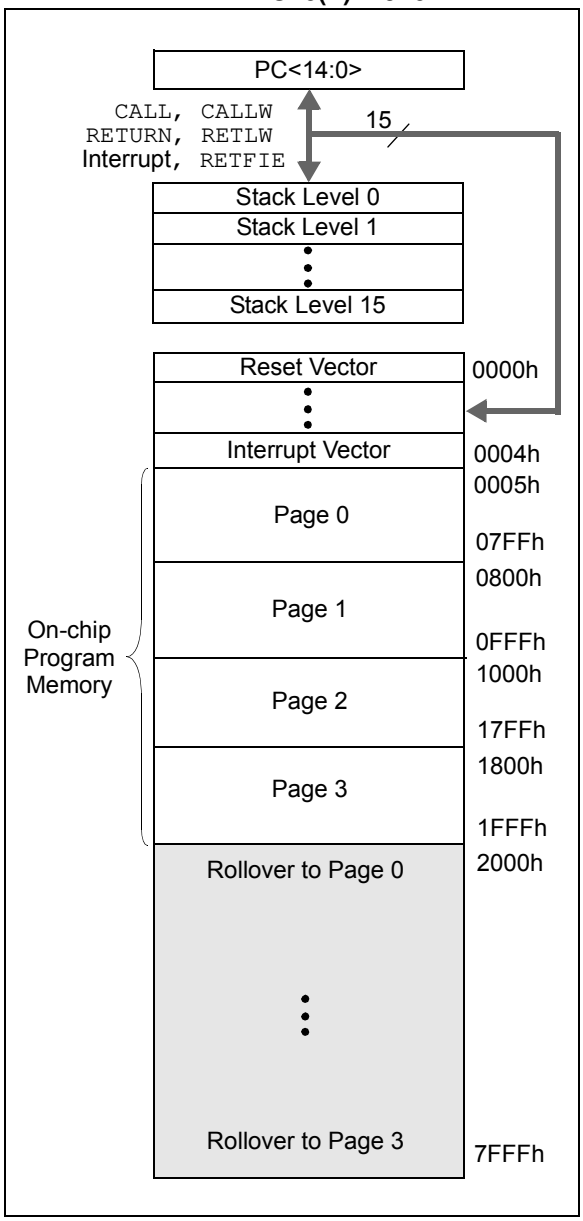
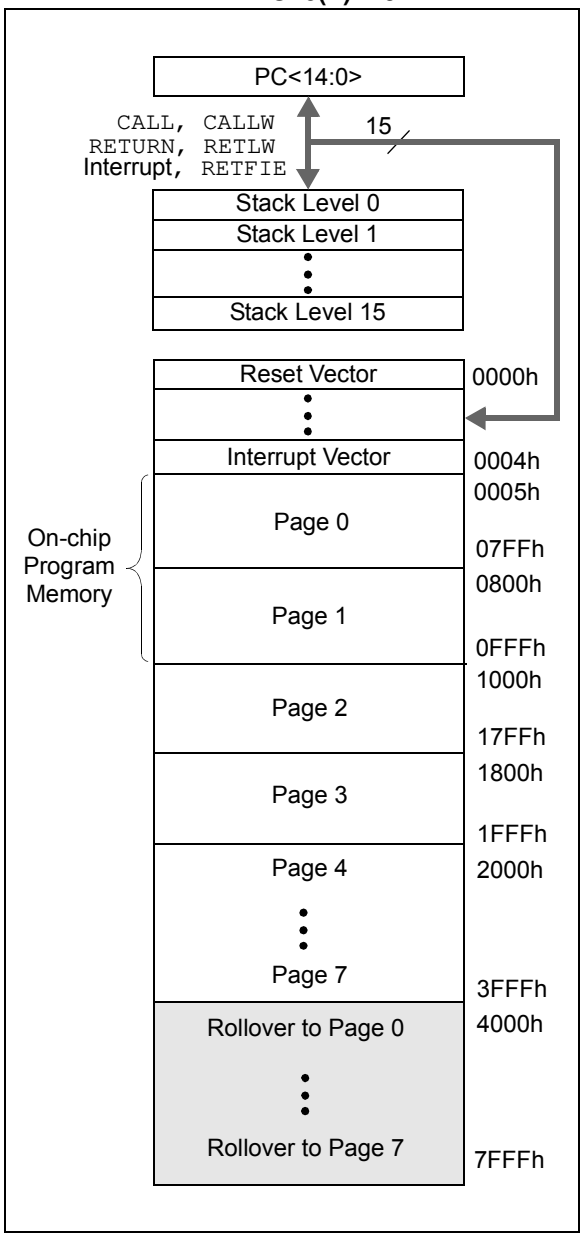


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1947



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    CALL constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    DW          DATA0       ;First constant
    DW          DATA1       ;Second constant
    DW          DATA2
    DW          DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   DATA_INDEX
    ADDLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constant ;MSb is set
automatically
    MOVWF   FSR1H
    BTFSC   STATUS,C    ;cary from ADDLW?
    INCF    FSR1H,f     ;yes
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.6 "Indirect Addressing"** for more information.

Data Memory uses a 12-bit address. The upper five bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-4.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 29.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

3.3 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC(1):** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C(1):** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

3.3.1 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.3.2 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

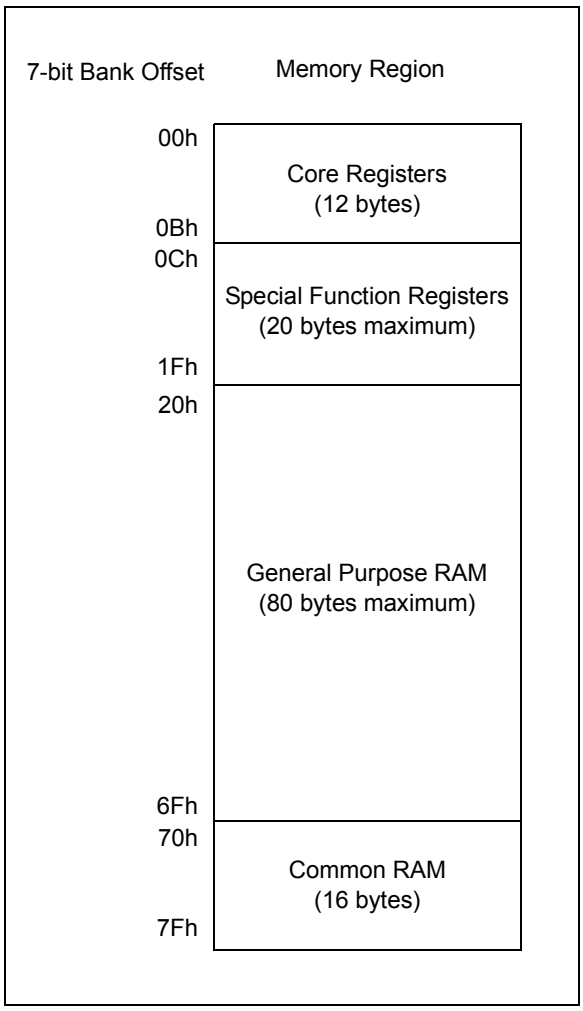
3.3.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.6.2 "Linear Data Memory"** for more information.

3.3.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.3.4 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Table 3-3.

TABLE 3-3: MEMORY MAP TABLES

Device	Banks	Table No.
PIC16(L)F1946/47	0-7	Table 3-4
	8-15	Table 3-5, Table 3-8
	16-23	Table 3-6
	23-31	Table 3-7, Table 3-9

TABLE 3-4: PIC16(L)F1946/47 MEMORY MAP, BANKS 0-7

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	INDF0	080h	INDF0	100h	INDF0	180h	INDF0	200h	INDF0	280h	INDF0	300h	INDF0	380h	INDF0
001h	INDF1	081h	INDF1	101h	INDF1	181h	INDF1	201h	INDF1	281h	INDF1	301h	INDF1	381h	INDF1
002h	PCL	082h	PCL	102h	PCL	182h	PCL	202h	PCL	282h	PCL	302h	PCL	382h	PCL
003h	STATUS	083h	STATUS	103h	STATUS	183h	STATUS	203h	STATUS	283h	STATUS	303h	STATUS	383h	STATUS
004h	FSR0L	084h	FSR0L	104h	FSR0L	184h	FSR0L	204h	FSR0L	284h	FSR0L	304h	FSR0L	384h	FSR0L
005h	FSR0H	085h	FSR0H	105h	FSR0H	185h	FSR0H	205h	FSR0H	285h	FSR0H	305h	FSR0H	385h	FSR0H
006h	FSR1L	086h	FSR1L	106h	FSR1L	186h	FSR1L	206h	FSR1L	286h	FSR1L	306h	FSR1L	386h	FSR1L
007h	FSR1H	087h	FSR1H	107h	FSR1H	187h	FSR1H	207h	FSR1H	287h	FSR1H	307h	FSR1H	387h	FSR1H
008h	BSR	088h	BSR	108h	BSR	188h	BSR	208h	BSR	288h	BSR	308h	BSR	388h	BSR
009h	WREG	089h	WREG	109h	WREG	189h	WREG	209h	WREG	289h	WREG	309h	WREG	389h	WREG
00Ah	PCLATH	08Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH	20Ah	PCLATH	28Ah	PCLATH	30Ah	PCLATH	38Ah	PCLATH
00Bh	INTCON	08Bh	INTCON	10Bh	INTCON	18Bh	INTCON	20Bh	INTCON	28Bh	INTCON	30Bh	INTCON	38Bh	INTCON
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	—	28Ch	PORTF	30Ch	TRISF	38Ch	LATF
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	—	20Dh	WPUB	28Dh	PORTG	30Dh	TRISG	38Dh	LATG
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	—	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	PORTD	08Fh	TRISD	10Fh	LATD	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	LATE	190h	ANSELE	210h	—	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	EEADRL	211h	SSP1BUF	291h	CCPR1L	311h	CCPR3L	391h	—
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	EEADRH	212h	SSP1ADD	292h	CCPR1H	312h	CCPR3H	392h	—
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	EEDATL	213h	SSP1MSK	293h	CCP1CON	313h	CCP3CON	393h	—
014h	PIR4	094h	PIE4	114h	CM2CON1	194h	EEDATH	214h	SSP1STAT	294h	PWM1CON	314h	PWM3CON	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	EECON1	215h	SSP1CON1	295h	CCP1AS	315h	CCP3AS	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	SSP1CON2	296h	PSTR1CON	316h	PSTR3CON	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	SSP1CON3	297h	—	317h	—	397h	—
018h	T1CON	098h	OSCTUNE	118h	DACCON0	198h	—	218h	—	298h	CCPR2L	318h	CCPR4L	398h	—
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	RC1REG	219h	SSP2BUF	299h	CCPR2H	319h	CCPR4H	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	SRCON0	19Ah	TX1REG	21Ah	SSP2ADD	29Ah	CCP2CON	31Ah	CCP4CON	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	SRCON1	19Bh	SP1BRGL	21Bh	SSP2MSK	29Bh	PWM2CON	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SP1BRGH	21Ch	SSP2STAT	29Ch	CCP2AS	31Ch	CCPR5L	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON	19Dh	RC1STA	21Dh	SSP2CON1	29Dh	PSTR2CON	31Dh	CCPR5H	39Dh	—
01Eh	CPSCON0	09Eh	ADCON1	11Eh	CM3CON0	19Eh	TX1STA	21Eh	SSP2CON2	29Eh	CCPTMRS0	31Eh	CCP5CON	39Eh	—
01Fh	CPSCON1	09Fh	—	11Fh	CM3CON1	19Fh	BAUD1CON	21Fh	SSP2CON3	29Fh	CCPTMRS1	31Fh	—	39Fh	—
020h 06Fh	General Purpose Register 96 Bytes	0A0h 0EFh	General Purpose Register 80 Bytes	120h 16Fh	General Purpose Register 80 Bytes	1A0h 1EFh	General Purpose Register 80 Bytes	220h 26Fh	General Purpose Register 80 Bytes	2A0h 2EFh	General Purpose Register 80 Bytes	320h 32Fh 330h 36Fh	General Purpose Register 16 Bytes General Purpose Register 64 Bytes(1)	3A0h 3EFh	General Purpose Register 80 Bytes(1)
070h 07Fh		0F0h 0FFh	Accesses 70h – 7Fh	170h 17Fh	Accesses 70h – 7Fh	1F0h 1FFh	Accesses 70h – 7Fh	270h 27Fh	Accesses 70h – 7Fh	2F0h 2FFh	Accesses 70h – 7Fh	370h 37Fh	Accesses 70h – 7Fh	3F0h 3FFh	Accesses 70h – 7Fh

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Not available on PIC16F1946.

TABLE 3-5: PIC16(L)F1946/47 MEMORY MAP, BANKS 8-15

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	INDF0	480h	INDF0	500h	INDF0	580h	INDF0	600h	INDF0	680h	INDF0	700h	INDF0	780h	INDF0
401h	INDF1	481h	INDF1	501h	INDF1	581h	INDF1	601h	INDF1	681h	INDF1	701h	INDF1	781h	INDF1
402h	PCL	482h	PCL	502h	PCL	582h	PCL	602h	PCL	682h	PCL	702h	PCL	782h	PCL
403h	STATUS	483h	STATUS	503h	STATUS	583h	STATUS	603h	STATUS	683h	STATUS	703h	STATUS	783h	STATUS
404h	FSR0L	484h	FSR0L	504h	FSR0L	584h	FSR0L	604h	FSR0L	684h	FSR0L	704h	FSR0L	784h	FSR0L
405h	FSR0H	485h	FSR0H	505h	FSR0H	585h	FSR0H	605h	FSR0H	685h	FSR0H	705h	FSR0H	785h	FSR0H
406h	FSR1L	486h	FSR1L	506h	FSR1L	586h	FSR1L	606h	FSR1L	686h	FSR1L	706h	FSR1L	786h	FSR1L
407h	FSR1H	487h	FSR1H	507h	FSR1H	587h	FSR1H	607h	FSR1H	687h	FSR1H	707h	FSR1H	787h	FSR1H
408h	BSR	488h	BSR	508h	BSR	588h	BSR	608h	BSR	688h	BSR	708h	BSR	788h	BSR
409h	WREG	489h	WREG	509h	WREG	589h	WREG	609h	WREG	689h	WREG	709h	WREG	789h	WREG
40Ah	PCLATH	48Ah	PCLATH	50Ah	PCLATH	58Ah	PCLATH	60Ah	PCLATH	68Ah	PCLATH	70Ah	PCLATH	78Ah	PCLATH
40Bh	INTCON	48Bh	INTCON	50Bh	INTCON	58Bh	INTCON	60Bh	INTCON	68Bh	INTCON	70Bh	INTCON	78Bh	INTCON
40Ch	ANSELF	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	ANSELG	48Dh	WPUG	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	—	490h	—	510h	—	590h	—	610h	—	690h	—	710h	—	790h	—
411h	—	491h	RC2REG	511h	—	591h	—	611h	—	691h	—	711h	—	791h	See Table 3-8
412h	—	492h	TX2REG	512h	—	592h	—	612h	—	692h	—	712h	—	792h	
413h	—	493h	SP2BRGL	513h	—	593h	—	613h	—	693h	—	713h	—	793h	
414h	—	494h	SP2BRGH	514h	—	594h	—	614h	—	694h	—	714h	—	794h	
415h	TMR4	495h	RC2STA	515h	—	595h	—	615h	—	695h	—	715h	—	795h	
416h	PR4	496h	TX2STA	516h	—	596h	—	616h	—	696h	—	716h	—	796h	
417h	T4CON	497h	BAUD2CON	517h	—	597h	—	617h	—	697h	—	717h	—	797h	
418h	—	498h	—	518h	—	598h	—	618h	—	698h	—	718h	—	798h	
419h	—	499h	—	519h	—	599h	—	619h	—	699h	—	719h	—	799h	
41Ah	—	49Ah	—	51Ah	—	59Ah	—	61Ah	—	69Ah	—	71Ah	—	79Ah	
41Bh	—	49Bh	—	51Bh	—	59Bh	—	61Bh	—	69Bh	—	71Bh	—	79Bh	
41Ch	TMR6	49Ch	—	51Ch	—	59Ch	—	61Ch	—	69Ch	—	71Ch	—	79Ch	
41Dh	PR6	49Dh	—	51Dh	—	59Dh	—	61Dh	—	69Dh	—	71Dh	—	79Dh	
41Eh	T6CON	49Eh	—	51Eh	—	59Eh	—	61Eh	—	69Eh	—	71Eh	—	79Eh	
41Fh	—	49Fh	—	51Fh	—	59Fh	—	61Fh	—	69Fh	—	71Fh	—	79Fh	
420h	General Purpose Register 80 Bytes(1)	4A0h	General Purpose Register 80 Bytes(1)	520h	General Purpose Register 80 Bytes(1)	5A0h	General Purpose Register 80 Bytes(1)	620h	General Purpose Register 48 Bytes(1)	6A0h	Unimplemented Read as '0'	720h	Unimplemented Read as '0'	7A0h	
46Fh		4EFh		56Fh		5EFh		66Fh	Unimplemented Read as '0'	6EFh		76Fh		7EFh	
470h	Accesses 70h – 7Fh	4F0h	Accesses 70h – 7Fh	570h	Accesses 70h – 7Fh	5F0h	Accesses 70h – 7Fh	670h	Accesses 70h – 7Fh	6F0h	Accesses 70h – 7Fh	770h	Accesses 70h – 7Fh	7F0h	Accesses 70h – 7Fh
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

Legend: = Unimplemented data memory locations, read as '0'

Note 1: Not available on PIC16F1946.