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PIC16(L)F722/3/4/6/7

28/40/44-Pin Flash Microcontrollers with XLP Technology

Devices Included In This Data Sheet:

PIC16F722/3/4/6/7 Devices:

- PIC16F722
- PIC16F723
- PIC16F724
- PIC16F726
- PIC16F727

PIC16LF722/3/4/6/7 Devices:

- PIC16LF722
- PIC16LF723
- PIC16LF724
- PIC16LF726
- PIC16LF727

High-Performance RISC CPU:

- Only 35 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Up to 8K x 14 Words of Flash Program Memory
- Up to 368 Bytes of Data Memory (RAM)
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes
- Processor Read Access to Program Memory
- Pinout Compatible to other 28/40-pin PIC16CXXX and PIC16FXXX Microcontrollers

Special Microcontroller Features:

- Precision Internal Oscillator:
  - 16 MHz or 500 kHz operation
  - Factory calibrated to ±1%, typical
  - Software tunable
  - Software selectable ÷1, ÷2, ÷4 or ÷8 divider
- 1.8V-5.5V Operation – PIC16F722/3/4/6/7
- 1.8V-3.6V Operation – PIC16LF722/3/4/6/7
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR):
  - Selectable between two trip points
  - Disable in Sleep option
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- Multiplexed Master Clear with Pull-up/Input Pin
- Industrial and Extended Temperature Range
- High-Endurance Flash Cell:
  - 1,000 write Flash endurance (typical)
  - Flash retention: > 40 years
- Power-Saving Sleep mode

Extreme Low-Power Management PIC16LF722/3/4/6/7 with XLP:

- Sleep Mode: 20 nA
- Watchdog Timer: 500 nA
- Timer1 Oscillator: 600 nA @ 32 kHz

Analog Features:

- A/D Converter:
  - 8-bit resolution and up to 14 channels
  - Conversion available during Sleep
  - Selectable 1.024/2.048/4.096V voltage reference
- On-chip 3.2V Regulator (PIC16F722/3/4/6/7 devices only)

Peripheral Highlights:

- Up to 35 I/O Pins and One Input-only Pin:
  - High-current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - Dedicated low-power 32 kHz oscillator
  - 16-bit timer/counter with prescaler
  - External Gate Input mode with Toggle and Single Shot modes
  - Interrupt-on-gate completion
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture, Compare, PWM (CCP) Modules:
  - 16-bit Capture, max. resolution 12.5 ns
  - 16-bit Compare, max. resolution 200 ns
  - 10-bit PWM, max. frequency 20 kHz
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART)
- Synchronous Serial Port (SSP):
  - SPI (Master/Slave)
  - I^2C (Slave) with Address Mask
- mTouch® Sensing Oscillator Module:
  - Up to 16 input channels

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PIC16(L)F72X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash Memory (bytes)	I/O's(2)	8-bit ADC (ch)	CapSense (ch)	Timers (8/16-bit)	AUSART	SSP (I^2C/SPI)	CCP	Debug(1)	XLP
PIC16(L)F707	(1)	8192	363	0	36	14	32	4/2	1	1	2	I	Y
PIC16(L)F720	(2)	2048	128	128	18	12	—	2/1	1	1	1	I	Y
PIC16(L)F721	(2)	4096	256	128	18	12	—	2/1	1	1	1	I	Y
PIC16(L)F722	(4)	2048	128	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F722A	(3)	2048	128	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F723	(4)	4096	192	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F723A	(3)	4096	192	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F724	(4)	4096	192	0	36	14	16	2/1	1	1	2	I	Y
PIC16(L)F726	(4)	8192	368	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F727	(4)	8192	368	0	36	14	16	2/1	1	1	2	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS41418 PIC16(L)F707 Data Sheet, 40/44-Pin Flash, 8-bit Microcontrollers

2: DS41430 PIC16(L)F720/721 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers

3: DS41417 PIC16(L)F722A/723A Data Sheet, 28-Pin Flash, 8-bit Microcontrollers

4: DS41341 PIC16(L)F72X Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers

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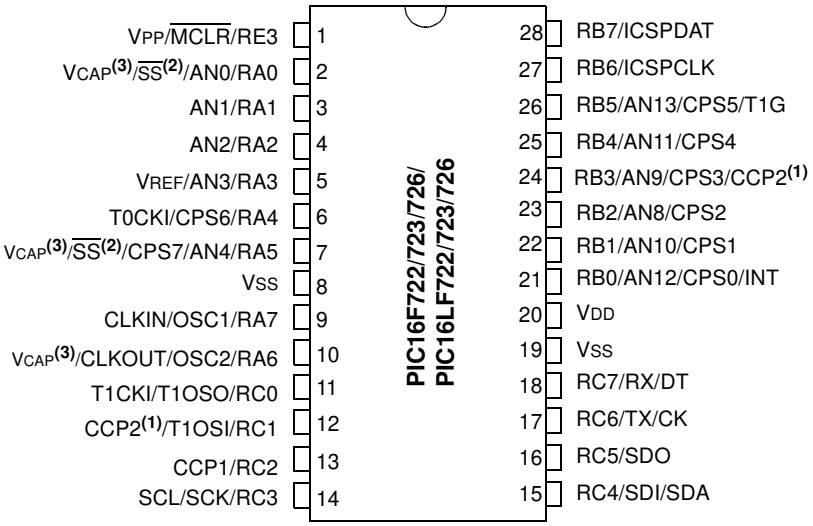
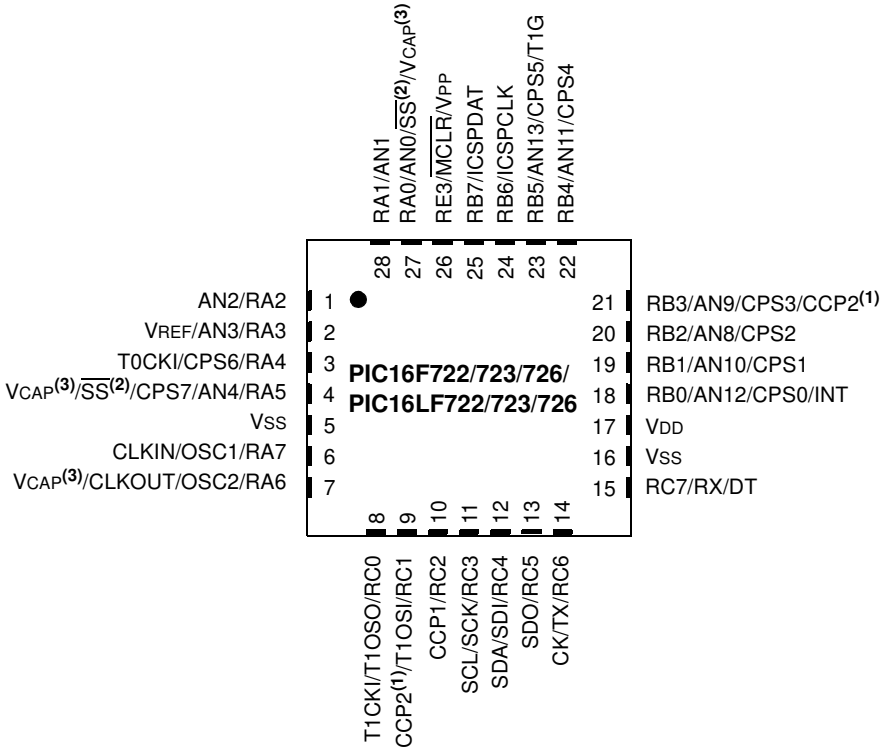
Pin Diagrams – 28-PIN PDIP/SOIC/SSOP/QFN/UQFN (PIC16F722/723/726/PIC16LF722/723/726)

PDIP, SOIC, SSOP



QFN, UQFN



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: $\overline{SS}$ pin location may be selected as RA5 or RA0.
3: PIC16F722/723/726 devices only.

TABLE 1: 28-PIN PDIP/SOIC/SSOP/QFN/UQFN SUMMARY (PIC16F722/723/726/PIC16LF722/723/726)

I/O	28-Pin PDIP, SOIC, SSOP	28-Pin QFN, UQFN	A/D	Cap Sensor	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	27	AN0	—	—	—	—	$\overline{SS}$(3)	—	—	VCAP(4)
RA1	3	28	AN1	—	—	—	—	—	—	—	—
RA2	4	1	AN2	—	—	—	—	—	—	—	—
RA3	5	2	AN3/VREF	—	—	—	—	—	—	—	—
RA4	6	3	—	CPS6	T0CKI	—	—	—	—	—	—
RA5	7	4	AN4	CPS7	—	—	—	$\overline{SS}$(3)	—	—	VCAP(4)
RA6	10	7	—	—	—	—	—	—	—	—	OSC2/CLKOUT/VCAP(4)
RA7	9	6	—	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	21	18	AN12	CPS0	—	—	—	—	IOC/INT	Y	—
RB1	22	19	AN10	CPS1	—	—	—	—	IOC	Y	—
RB2	23	20	AN8	CPS2	—	—	—	—	IOC	Y	—
RB3	24	21	AN9	CPS3	—	CCP2(2)	—	—	IOC	Y	—
RB4	25	22	AN11	CPS4	—	—	—	—	IOC	Y	—
RB5	26	23	AN13	CPS5	T1G	—	—	—	IOC	Y	—
RB6	27	24	—	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	28	25	—	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	11	8	—	—	T1OSO/T1CKI	—	—	—	—	—	—
RC1	12	9	—	—	T1OSI	CCP2(2)	—	—	—	—	—
RC2	13	10	—	—	—	CCP1	—	—	—	—	—
RC3	14	11	—	—	—	—	—	SCK/SCL	—	—	—
RC4	15	12	—	—		—	—	SDI/SDA	—	—	—
RC5	16	13	—	—	—	—	—	SDO	—	—	—
RC6	17	14	—	—	—	—	TX/CK	—	—	—	—
RC7	18	15	—	—	—	—	RX/DT	—	—	—	—
RE3	1	26	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	20	17	—	—	—	—	—	—	—	—	VDD
—	8,19	5,16	—	—	—	—	—	—	—	—	VSS

Note 1: Pull-up enabled only with external $\overline{MCLR}$ Configuration.
2: RC1 is the default pin location for CCP2. RB3 may be selected by changing the CCP2SEL bit in the APFCON register.
3: RA5 is the default pin location for $\overline{SS}$. RA0 may be selected by changing the SSSEL bit in the APFCON register.
4: PIC16F724/727/PIC16LF724/727 devices only.

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available VCAP pins to stabilize the regulator. For more information, see **Section 5.0 "Low Dropout (LDO) Voltage Regulator"**. The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

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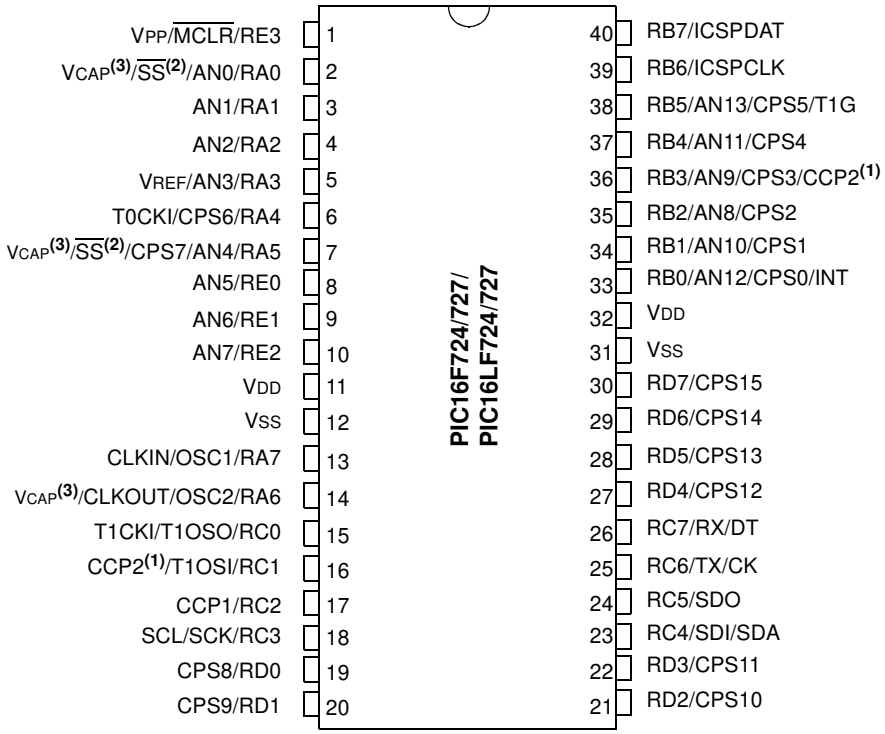
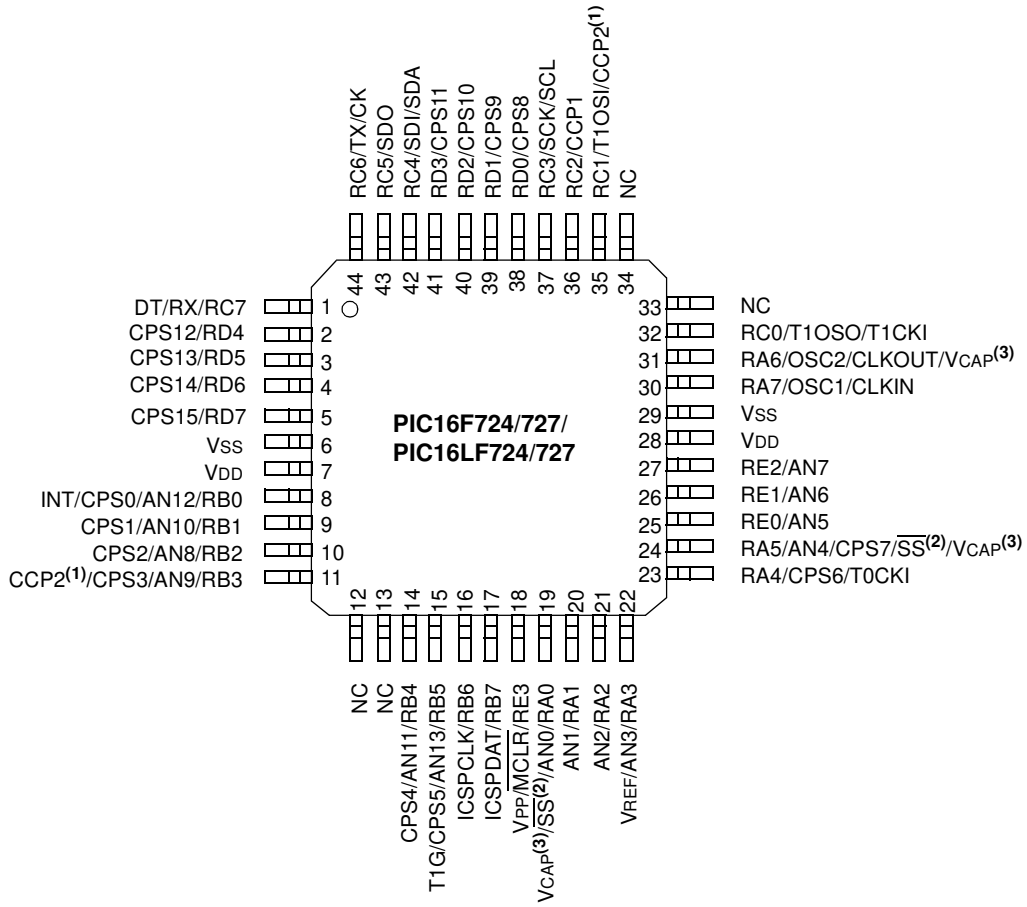
Pin Diagrams – 40-PIN PDIP (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: SS pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

Pin Diagrams – 44-PIN TQFP (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: $\overline{SS}$ pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

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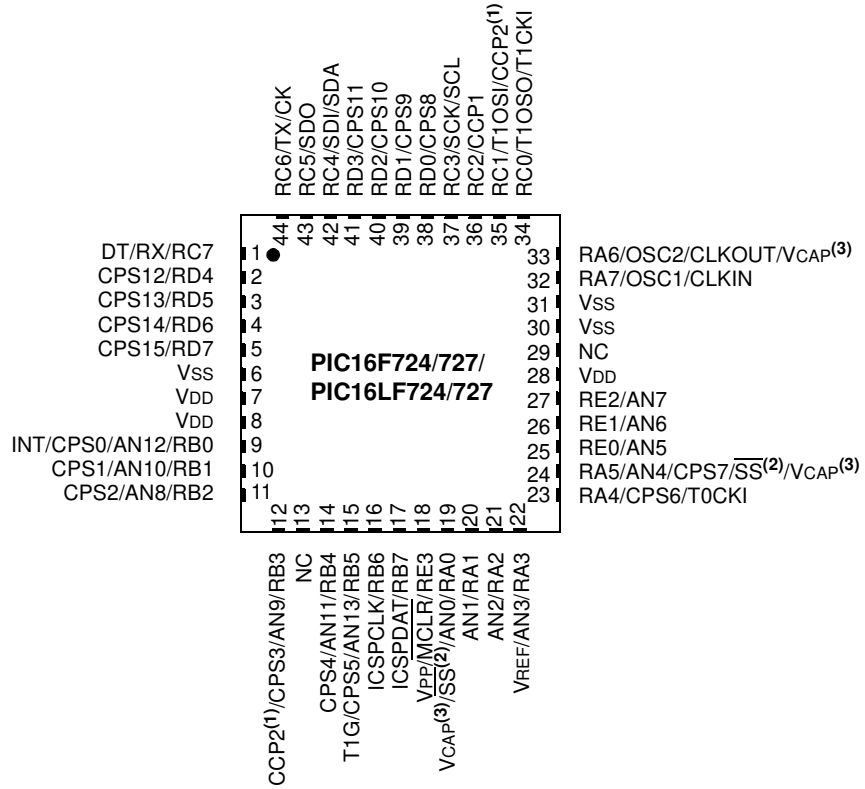
Pin Diagrams – 44-PIN QFN (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: $\overline{SS}$ pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

TABLE 2: 40/44-PIN PDIP/TQFP/QFN SUMMARY (PIC16F724/727/PIC16LF724/727)

I/O	40-Pin PDIP	44-Pin TQFP	44-Pin QFN	A/D	Cap Sensor	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	19	19	AN0	—	—	—	—	$\overline{SS}$(3)	—	—	VCAP(4)
RA1	3	20	20	AN1	—	—	—	—	—	—	—	—
RA2	4	21	21	AN2	—	—	—	—	—	—	—	—
RA3	5	22	22	AN3/VREF	—	—	—	—	—	—	—	—
RA4	6	23	23	—	CPS6	T0CKI	—	—	—	—	—	—
RA5	7	24	24	AN4	CPS7	—	—	—	$\overline{SS}$(3)	—	—	VCAP(4)
RA6	14	31	33	—	—	—	—	—	—	—	—	OSC2/CLKOUT/VCAP(4)
RA7	13	30	32	—	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	33	8	9	AN12	CPS0	—	—	—	—	IOC/INT	Y	—
RB1	34	9	10	AN10	CPS1	—	—	—	—	IOC	Y	—
RB2	35	10	11	AN8	CPS2	—	—	—	—	IOC	Y	—
RB3	36	11	12	AN9	CPS3	—	CCP2(2)	—	—	IOC	Y	—
RB4	37	14	14	AN11	CPS4	—	—	—	—	IOC	Y	—
RB5	38	15	15	AN13	CPS5	T1G	—	—	—	IOC	Y	—
RB6	39	16	16	—	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	40	17	17	—	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	15	32	34	—	—	T1OSO/ T1CKI	—	—	—	—	—	—
RC1	16	35	35	—	—	T1OSI	CCP2(2)	—	—	—	—	—
RC2	17	36	36	—	—	—	CCP1	—	—	—	—	—
RC3	18	37	37	—	—	—	—	—	SCK/SCL	—	—	—
RC4	23	42	42	—	—		—	—	SDI/SDA	—	—	—
RC5	24	43	43	—	—		—	—	SDO	—	—	—
RC6	25	44	44	—	—	—	—	TX/CK	—	—	—	—
RC7	26	1	1	—	—	—	—	RX/DT	—	—	—	—
RD0	19	38	38	—	CPS8	—	—	—	—	—	—	—
RD1	20	39	39	—	CPS9	—	—	—	—	—	—	—
RD2	21	40	40	—	CPS10	—	—	—	—	—	—	—
RD3	22	41	41	—	CPS11	—	—	—	—	—	—	—
RD4	27	2	2	—	CPS12	—	—	—	—	—	—	—
RD5	28	3	3	—	CPS13	—	—	—	—	—	—	—
RD6	29	4	4	—	CPS14	—	—	—	—	—	—	—
RD7	30	5	5	—	CPS15	—	—	—	—	—	—	—
RE0	8	25	25	AN5	—	—	—	—	—	—	—	—
RE1	9	26	26	AN6	—	—	—	—	—	—	—	—
RE2	10	27	27	AN7	—	—	—	—	—	—	—	—
RE3	1	18	18	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	11,32	7,28	7,8,28	—	—	—	—	—	—	—	—	VDD
—	12,13	6,29	6,30,31	—	—	—	—	—	—	—	—	VSS

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.
2: RC1 is the default pin location for CCP2. RB3 may be selected by changing the CCP2SEL bit in the APFCON register.
3: RA5 is the default pin location for $\overline{SS}$. RA0 may be selected by changing the SSSEL bit in the APFCON register.
4: PIC16F722/3/4/6/7 devices only.

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available VCAP pins to stabilize the regulator. For more information, see **Section 5.0 "Low Dropout (LDO) Voltage Regulator"**. The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

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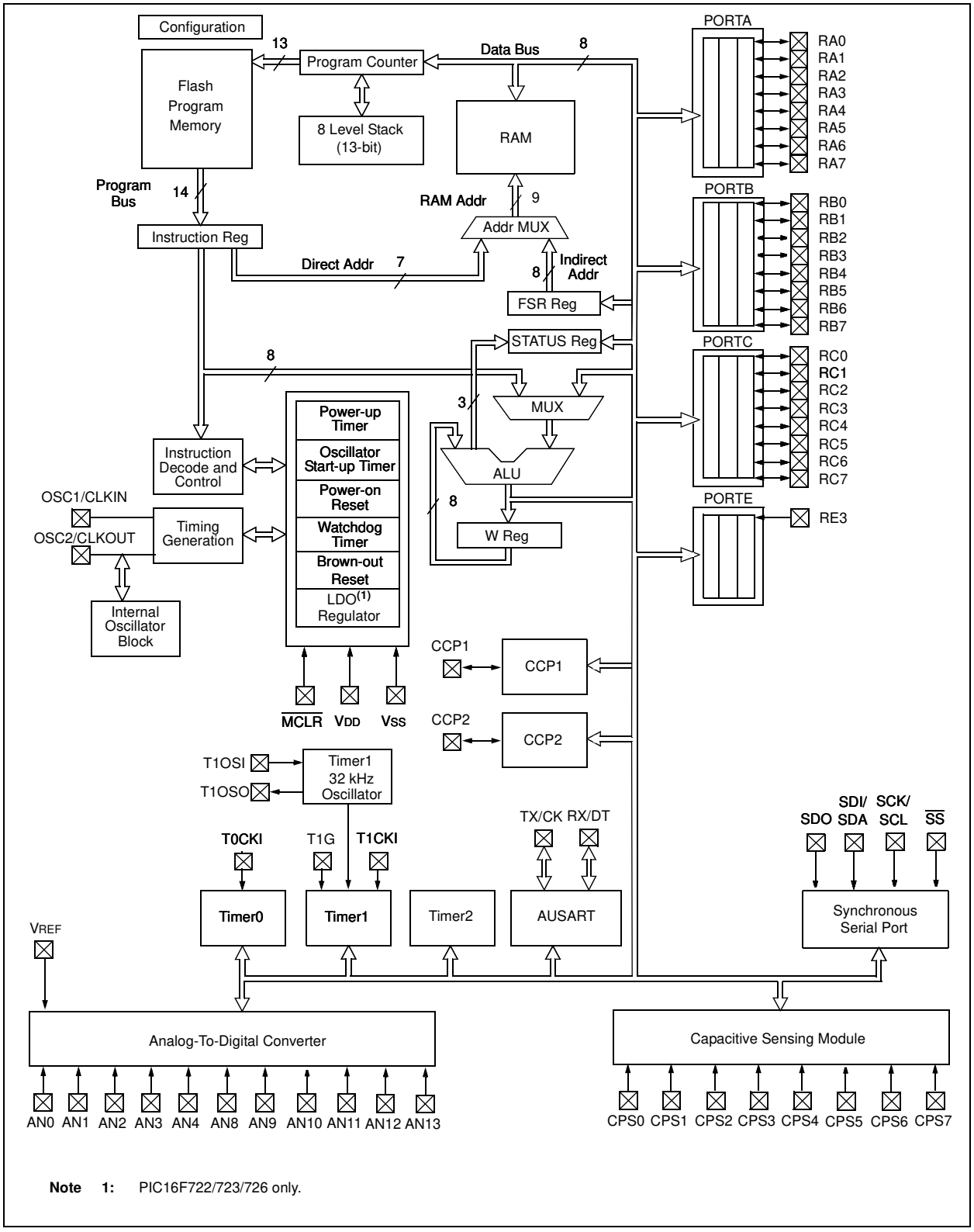
1.0 DEVICE OVERVIEW

The PIC16(L)F722/3/4/6/7 devices are covered by this data sheet. They are available in 28/40/44-pin packages. Figure 1-1 shows a block diagram of the PIC16F722/723/726/PIC16LF722/723/726 devices and Figure 1-2 shows a block diagram of the PIC16F724/727/PIC16LF724/727 devices. Table 1-1 shows the pinout descriptions.

FIGURE 1-1: PIC16F722/723/726/PIC16LF722/723/726 BLOCK DIAGRAM



Note 1: PIC16F722/723/726 only.

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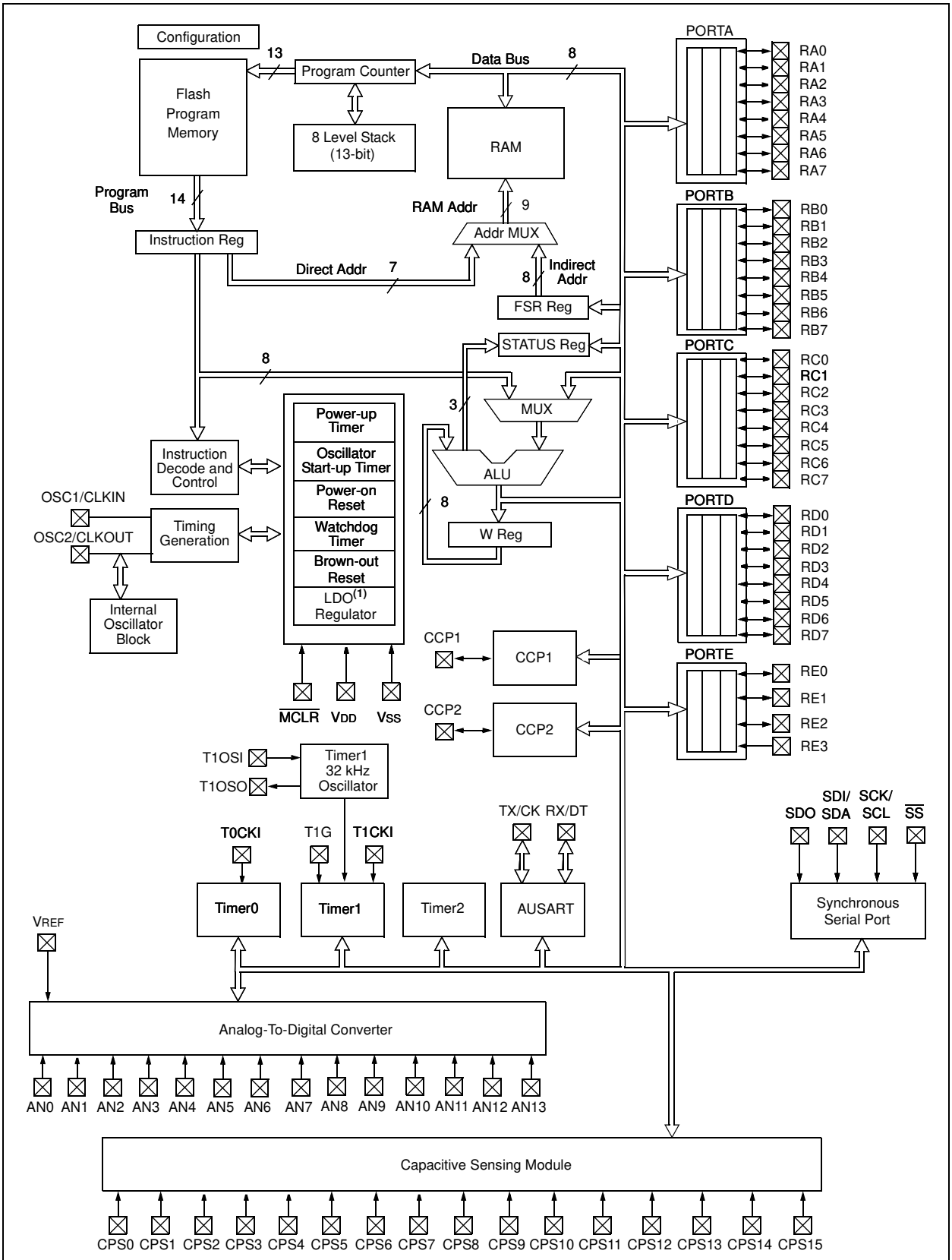
FIGURE 1-2: PIC16F724/727/PIC16LF724/727 BLOCK DIAGRAM



Note 1: PIC16F724/727 only.

TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/$\overline{SS}$/VCAP	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	$\overline{SS}$	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA1/AN1	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
RA2/AN2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
RA3/AN3/VREF	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	VREF	AN	—	A/D Voltage Reference input.
RA4/CPS6/T0CKI	RA4	TTL	CMOS	General purpose I/O.
	CPS6	AN	—	Capacitive sensing input 6.
	T0CKI	ST	—	Timer0 clock input.
RA5/AN4/CPS7/$\overline{SS}$/VCAP	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS7	AN	—	Capacitive sensing input 7.
	$\overline{SS}$	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA6/OSC2/CLKOUT/VCAP	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA7/OSC1/CLKIN	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	CLKIN	ST	—	RC oscillator connection (RC mode).
RB0/AN12/CPS0/INT	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12 input.
	CPS0	AN	—	Capacitive sensing input 0.
	INT	ST	—	External interrupt.
RB1/AN10/CPS1	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	CPS1	AN	—	Capacitive sensing input 1.
RB2/AN8/CPS2	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8 input.
	CPS2	AN	—	Capacitive sensing input 2.
RB3/AN9/CPS3/CCP2	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9 input.
	CPS3	AN	—	Capacitive sensing input 3.
	CCP2	ST	CMOS	Capture/Compare/PWM2.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

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TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB4/AN11/CPS4	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN11	AN	—	A/D Channel 11 input.
	CPS4	AN	—	Capacitive sensing input 4.
RB5/AN13/CPS5/T1G	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN13	AN	—	A/D Channel 13 input.
	CPS5	AN	—	Capacitive sensing input 5.
	T1G	ST	—	Timer1 Gate input.
RB6/ICSPCLK/ICDCLK	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RB7/ICSPDAT/ICDDAT	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	—	In-Circuit Data I/O.
RC0/T1OSO/T1CKI	RC0	ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
RC1/T1OSI/CCP2	RC1	ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/CCP1	RC2	ST	CMOS	General purpose I/O.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/SCK/SCL	RC3	ST	CMOS	General purpose I/O.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C clock.
RC4/SDI/SDA	RC4	ST	CMOS	General purpose I/O.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C data input/output.
RC5/SDO	RC5	ST	CMOS	General purpose I/O.
	SDO	—	CMOS	SPI data output.
RC6/TX/CK	RC6	ST	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
RC7/RX/DT	RC7	ST	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
RD0/CPS8	RD0	ST	CMOS	General purpose I/O.
	CPS8	AN	—	Capacitive sensing input 8.
RD1/CPS9	RD1	ST	CMOS	General purpose I/O.
	CPS9	AN	—	Capacitive sensing input 9.
RD2/CPS10	RD2	ST	CMOS	General purpose I/O.
	CPS10	AN	—	Capacitive sensing input 10.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD3/CPS11	RD3	ST	CMOS	General purpose I/O.
	CPS11	AN	—	Capacitive sensing input 11.
RD4/CPS12	RD4	ST	CMOS	General purpose I/O.
	CPS12	AN	—	Capacitive sensing input 12.
RD5/CPS13	RD5	ST	CMOS	General purpose I/O.
	CPS13	AN	—	Capacitive sensing input 13.
RD6/CPS14	RD6	ST	CMOS	General purpose I/O.
	CPS14	AN	—	Capacitive sensing input 14.
RD7/CPS15	RD7	ST	CMOS	General purpose I/O.
	CPS15	AN	—	Capacitive sensing input 15.
RE0/AN5	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
RE1/AN6	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
RE2/AN7	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
RE3/$\overline{MCLR}$/VPP	RE3	TTL	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available VCAP pins to stabilize the regulator. For more information, see **Section 5.0 "Low Dropout (LDO) Voltage Regulator"**. The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

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2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16(L)F722/3/4/6/7 has a 13-bit program counter capable of addressing a 2K x 14 program memory space for the PIC16F722/LF722 (0000h-07FFh), a 4K x 14 program memory space for the PIC16F723/LF723 and PIC16F724/LF724 (0000h-0FFFh) and an 8K x 14 program memory space for the PIC16F726/LF726 and PIC16F727/LF727 (0000h-1FFFh). Accessing a location above the memory boundaries for the PIC16F722/LF722 will cause a wrap-around within the first 2K x 14 program memory space. Accessing a location above the memory boundaries for the PIC16F723/LF723 and PIC16F724/LF724 will cause a wrap-around within the first 4K x 14 program memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F722/LF722

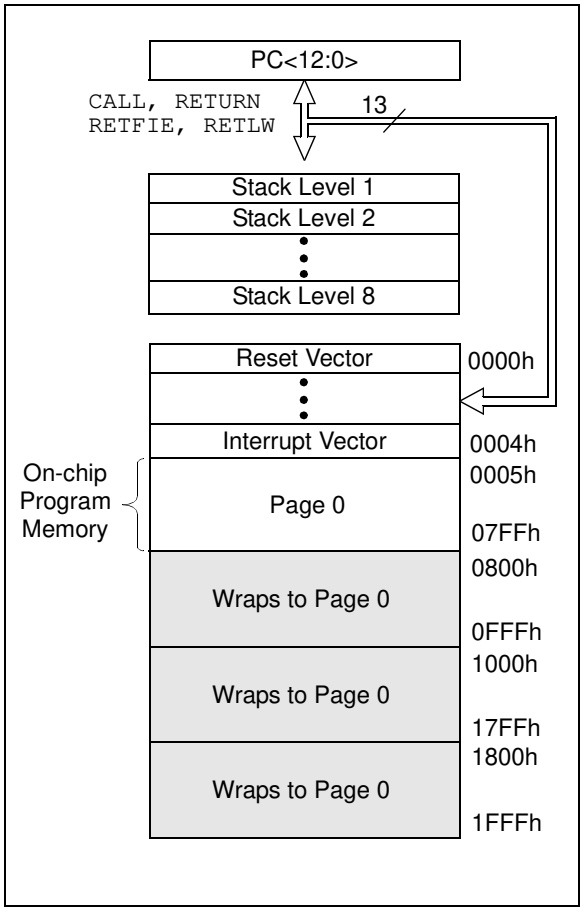


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F723/LF723 AND PIC16F724/LF724

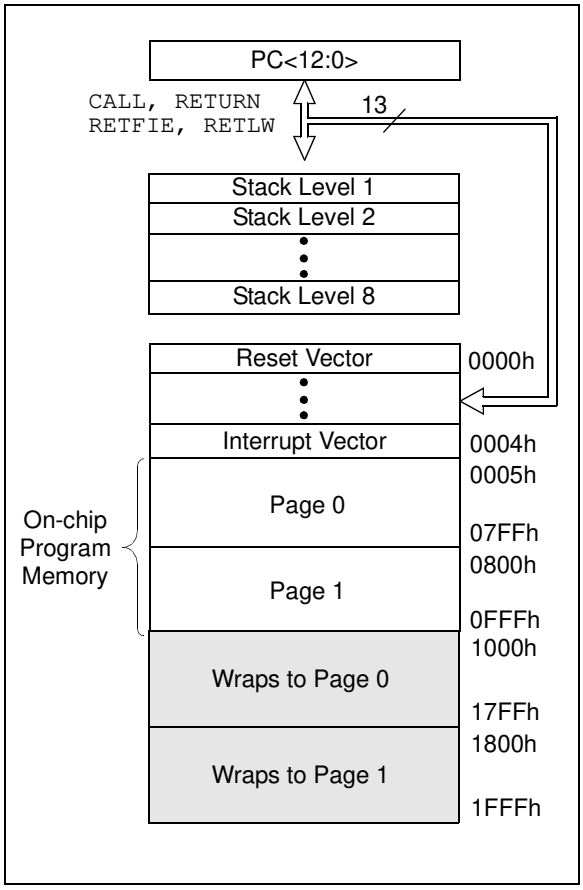
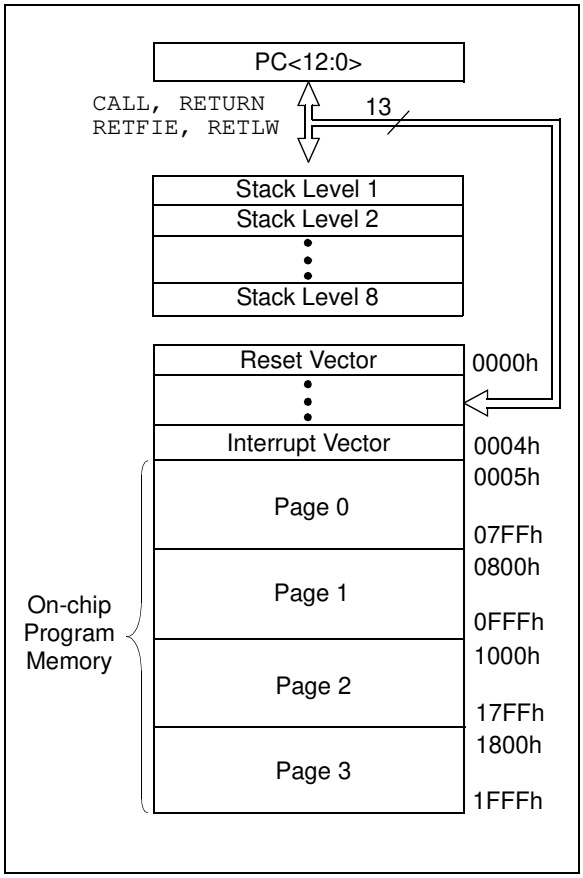


FIGURE 2-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F726/LF726 AND PIC16F727/LF727



2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers (GPRs) and the Special Function Registers (SFRs). Bits RP0 and RP1 are bank select bits.

RP1	RP0		
0	0	→	Bank 0 is selected
0	1	→	Bank 1 is selected
1	0	→	Bank 2 is selected
1	1	→	Bank 3 is selected

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 bits in the PIC16F722/LF722, 192 x 8 bits in the PIC16F723/LF723 and PIC16F724/LF724, and 368 x 8 bits in the PIC16F726/LF726 and PIC16F727/LF727. Each register is accessed either directly or indirectly through the File Select Register (FSR), (Refer to **Section 2.5 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (refer to Table 2-1). These registers are static RAM.

The Special Function Registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

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FIGURE 2-4: PIC16F722/LF722 SPECIAL FUNCTION REGISTERS

	Bank 0		Bank 1		Bank 2		Bank 3	
File Address								
	Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
	TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
	PCL	02h	PCL	82h	PCL	102h	PCL	182h
	STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
	FSR	04h	FSR	84h	FSR	104h	FSR	184h
	PORTA	05h	TRISA	85h		105h	ANSELA	185h
	PORTB	06h	TRISB	86h		106h	ANSELB	186h
	PORTC	07h	TRISC	87h		107h		187h
		08h		88h	CPSCON0	108h		188h
	PORTE	09h	TRISE	89h	CPSCON1	109h		189h
	PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
	INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
	PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
	PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
	TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
	TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
	T1CON	10h	OSCCON	90h		110h		190h
	TMR2	11h	OSCTUNE	91h		111h		191h
	T2CON	12h	PR2	92h		112h		192h
	SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
	SSPCON	14h	SSPSTAT	94h		114h		194h
	CCPR1L	15h	WPUB	95h		115h		195h
	CCPR1H	16h	IOCB	96h		116h		196h
	CCP1CON	17h		97h		117h		197h
	RCSTA	18h	TXSTA	98h		118h		198h
	TXREG	19h	SPBRG	99h		119h		199h
	RCREG	1Ah		9Ah		11Ah		19Ah
	CCPR2L	1Bh		9Bh		11Bh		19Bh
	CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
	CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
	ADRES	1Eh		9Eh		11Eh		19Eh
	ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
		7Fh		BFh		16Fh		1EFh
				C0h		170h		1F0h
			Accesses 70h-7Fh	EFh	Accesses 70h-7Fh		Accesses 70h-7Fh	
				F0h				
				FFh		17Fh		1FFh

Legend: = Unimplemented data memory locations, read as '0'.
* = Not a physical register.

FIGURE 2-5: PIC16F723/LF723 AND PIC16F724/LF724 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h	ANSELA	185h
PORTB	06h	TRISB	86h		106h	ANSELB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h	CPSCON0	108h	ANSELD(1)	188h
PORTE	09h	TRISE	89h	CPSCON1	109h	ANSELE(1)	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCCON	90h		110h		190h
TMR2	11h	OSCTUNE	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h	General Purpose Register 16 Bytes	120h		1A0h
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes			12Fh		
					130h		
			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses 70h-7Fh	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Legend: = Unimplemented data memory locations, read as '0'.
* = Not a physical register.

Note 1: PORTD, TRISD, ANSELD and ANSELE are not implemented on the PIC16F723/LF723, read as '0'

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FIGURE 2-6: PIC16F726/LF726 AND PIC16F727/LF727 SPECIAL FUNCTION REGISTERS

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h	ANSELA	185h
PORTB	06h	TRISB	86h		106h	ANSELB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h	CPSCON0	108h	ANSELD(1)	188h
PORTE	09h	TRISE	89h	CPSCON1	109h	ANSELE(1)	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCCON	90h	General Purpose Register 16 Bytes	110h	General Purpose Register 16 Bytes	190h
TMR2	11h	OSCTUNE	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h – 7Fh	General Purpose Register 80 Bytes	A0h – EFh	General Purpose Register 80 Bytes	120h – 16Fh	General Purpose Register 80 Bytes	1A0h – 1EFh
		Accesses 70h-7Fh	F0h – FFh	Accesses 70h-7Fh	170h – 17Fh	Accesses 70h-7Fh	1F0h – 1FFh

Legend: = Unimplemented data memory locations, read as '0',
* = Not a physical register

Note 1: PORTD, TRISD, ANSELD and ANSELE are not implemented on the PIC16F726/LF726, read as '0'

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 0											
00h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
01h	TMR0	Timer0 Module Register								xxxx xxxx	105,37
02h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	28,37
03h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	25,37
04h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx	51,37
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	60,37
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	70,37
08h(3)	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	77,37
09h	PORTE	—	—	—	—	RE3	RE2(3)	RE1(3)	RE0(3)	---- xxxx	81,37
0Ah(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
0Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
0Ch	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	47,37
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	48,37
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	113,37
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	113,37
10h	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	—	TMR1ON	0000 00-0	117,37
11h	TMR2	Timer2 Module Register								0000 0000	120,37
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	121,37
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	161,37
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	178,37
15h	CCPR1L	Capture/Compare/PWM Register (LSB)								xxxx xxxx	130,37
16h	CCPR1H	Capture/Compare/PWM Register (MSB)								xxxx xxxx	130,37
17h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	129,37
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	148,37
19h	TXREG	USART Transmit Data Register								0000 0000	147,37
1Ah	RCREG	USART Receive Data Register								0000 0000	145,37
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	130,37
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	130,37
1Dh	CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	129,37
1Eh	ADRES	A/D Result Register								xxxx xxxx	100,37
1Fh	ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON	--00 0000	99,37

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
2: These registers can be addressed from any bank.
3: These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.
4: Accessible only when SSPM<3:0> = 1001.
5: Accessible only when SSPM<3:0> ≠ 1001.
6: This bit is always '1' as RE3 is input-only.

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TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 1											
80h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	26,37
82h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	28,37
83h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	25,37
84h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	51,37
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	60,37
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	70,37
88h(3)	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	78,37
89h	TRISE	—	—	—	—	TRISE3(6)	TRISE2(3)	TRISE1(3)	TRISE0(3)	---- 1111	81,37
8Ah(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
8Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
8Ch	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	45,37
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	46,37
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	27,38
8Fh	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{DONE}$	T1GVAL	T1GSS1	T1GSS0	0000 0x00	118,38
90h	OSCCON	—	—	IRCF1	IRCF0	ICSL	ICSS	—	—	--10 qq--	87,38
91h	OSCTUNE	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	--00 0000	88,38
92h	PR2	Timer2 Period Register								1111 1111	120,38
93h	SSPADD(5)	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	169,38
93h	SSPMSK(4)	Synchronous Serial Port (I^2C mode) Address Mask Register								1111 1111	180,38
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	179,38
95h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	1111 1111	61,38
96h	IOCB	IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0	0000 0000	61,38
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	147,38
99h	SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	149,38
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	50,38
9Dh	FVRCON	FVRRDY	FVREN	—	—	—	—	ADFVR1	ADFVR0	q0-- --00	104,38
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	ADREF1	ADREF0	0000 --00	100,38

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.

4: Accessible only when SSPM<3:0> = 1001.

5: Accessible only when SSPM<3:0> ≠ 1001.

6: This bit is always '1' as RE3 is input-only.

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 2											
100h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
101h	TMR0	Timer0 Module Register								xxxx xxxx	105,37
102h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	28,37
103h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	25,37
104h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
105h	—	Unimplemented								—	—
106h	—	Unimplemented								—	—
107h	—	Unimplemented								—	—
108h	CPSCON0	CPSON	—	—	—	CPSRNG1	CPSRNG0	CPSOUT	T0XCS	0--- 0000	126,38
109h	CPSCON1	—	—	—	—	CPSCH3	CPSCH2	CPSCH1	CPSCH0	---- 0000	127,38
10Ah(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
10Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
10Ch	PMDATL	Program Memory Read Data Register Low Byte								xxxx xxxx	181,38
10Dh	PMADRL	Program Memory Read Address Register Low Byte								xxxx xxxx	181,38
10Eh	PMDATH	—	—	Program Memory Read Data Register High Byte						--xx xxxx	181,38
10Fh	PMADRH	—	—	—	Program Memory Read Address Register High Byte					---x xxxx	181,38
Bank 3											
180h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	26,37
182h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	28,37
183h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	25,37
184h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
185h	ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	--11 1111	52,38
186h	ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	61,38
187h	—	Unimplemented								—	—
188h	ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	1111 1111	78,38
189h(3)	ANSELE	—	—	—	—	—	ANSE2	ANSE1	ANSE0	---- -111	82,38
18Ah(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
18Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	182,38
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
2: These registers can be addressed from any bank.
3: These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.
4: Accessible only when SSPM<3:0> = 1001.
5: Accessible only when SSPM<3:0> ≠ 1001.
6: This bit is always '1' as RE3 is input-only.

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2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 21.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h-1FFh)
`0` = Bank 0, 1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`00` = Bank 0 (00h-7Fh)
`01` = Bank 1 (80h-FFh)
`10` = Bank 2 (100h-17Fh)
`11` = Bank 3 (180h-1FFh)

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
`1` = A carry out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
`1` = A carry out from the Most Significant bit of the result occurred
`0` = No carry out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.