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# PIC16F7X Data Sheet

28/40-pin, 8-bit CMOS FLASH
Microcontrollers

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### 28/40-Pin 8-Bit CMOS FLASH Microcontrollers

#### **Devices Included in this Data Sheet:**

PIC16F73PIC16F74PIC16F77

### **High Performance RISC CPU:**

- · High performance RISC CPU
- · Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two-cycle
- Operating speed: DC 20 MHz clock input DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory, Up to 368 x 8 bytes of Data Memory (RAM)
- Pinout compatible to the PIC16C73B/74B/76/77
- Pinout compatible to the PIC16F873/874/876/877
- Interrupt capability (up to 12 sources)
- · Eight level deep hardware stack
- · Direct, Indirect and Relative Addressing modes
- Processor read access to program memory

#### **Special Microcontroller Features:**

- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- · Programmable code protection
- · Power saving SLEEP mode
- · Selectable oscillator options
- In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>) via two pins

#### **Peripheral Features:**

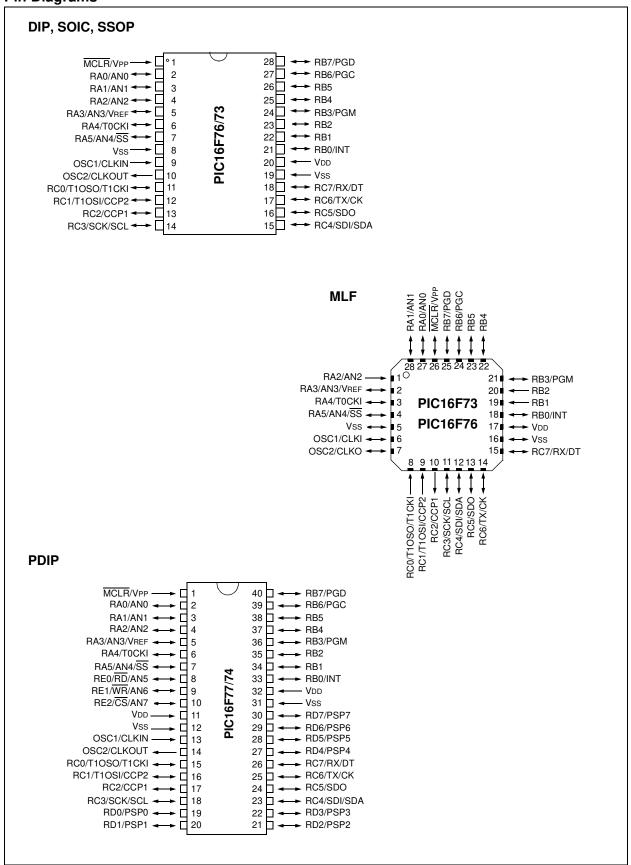
- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- 8-bit, up to 8-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI<sup>™</sup> (Master mode) and I<sup>2</sup>C<sup>™</sup> (Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP), 8-bits wide with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

#### **CMOS Technology:**

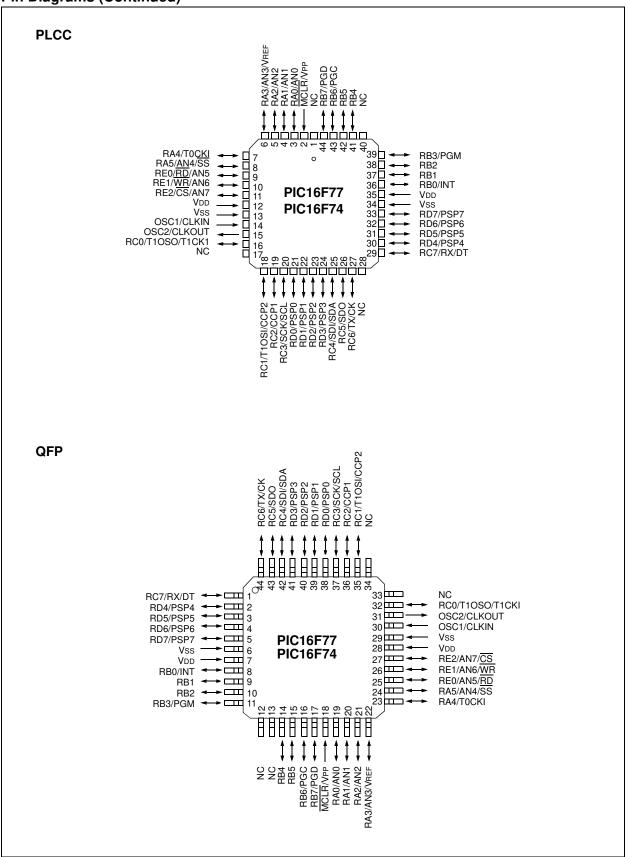
- · Low power, high speed CMOS FLASH technology
- · Fully static design
- · Wide operating voltage range: 2.0V to 5.5V
- · High Sink/Source Current: 25 mA
- · Industrial temperature range
- · Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 20 μA typical @ 3V, 32 kHz
  - < 1 μA typical standby current

	Program Memory	Data			O his	CCD	SS	P		Timero
Device	(# Single Word Instructions)	SRAM (Bytes)	I/O	Interrupts	8-bit A/D (ch)	CCP (PWM)	SPI (Master)	I <sup>2</sup> C (Slave)	USART	Timers 8/16-bit
PIC16F73	4096	192	22	11	5	2	Yes	Yes	Yes	2/1
PIC16F74	4096	192	33	12	8	2	Yes	Yes	Yes	2/1
PIC16F76	8192	368	22	11	5	2	Yes	Yes	Yes	2/1
PIC16F77	8192	368	33	12	8	2	Yes	Yes	Yes	2/1

### **Pin Diagrams**



# Pin Diagrams (Continued)



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#### 1.0 DEVICE OVERVIEW

This document contains device specific information about the following devices:

- PIC16F73
- PIC16F74
- PIC16F76
- PIC16F77

PIC16F73/76 devices are available only in 28-pin packages, while PIC16F74/77 devices are available in 40-pin and 44-pin packages. All devices in the PIC16F7X family share common architecture, with the following differences:

- The PIC16F73 and PIC16F76 have one-half of the total on-chip memory of the PIC16F74 and PIC16F77
- The 28-pin devices have 3 I/O ports, while the 40/44-pin devices have 5
- The 28-pin devices have 11 interrupts, while the 40/44-pin devices have 12
- The 28-pin devices have 5 A/D input channels, while the 40/44-pin devices have 8
- The Parallel Slave Port is implemented only on the 40/44-pin devices

The available features are summarized in Table 1-1. Block diagrams of the PIC16F73/76 and PIC16F74/77 devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

Additional information may be found in the PICmicro™ Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

TABLE 1-1: PIC16F7X DEVICE FEATURES

Key Features	PIC16F73	PIC16F74	PIC16F76	PIC16F77
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
Interrupts	11	12	11	12
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	SSP, USART	SSP, USART	SSP, USART	SSP, USART
Parallel Communications	_	PSP	_	PSP
8-bit Analog-to-Digital Module	5 Input Channels	8 Input Channels	5 Input Channels	8 Input Channels
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packaging	28-pin DIP 28-pin SOIC 28-pin SSOP 28-pin MLF	40-pin PDIP 44-pin PLCC 44-pin TQFP	28-pin DIP 28-pin SOIC 28-pin SSOP 28-pin MLF	40-pin PDIP 44-pin PLCC 44-pin TQFP

PIC16F73 AND PIC16F76 BLOCK DIAGRAM FIGURE 1-1: 13 8 **PORTA** Data Bus Program Counter RA0/AN0 FLASH RA1/AN1 Program Memory RA2/AN2/ RAM 8 Level Stack RA3/AN3/VREF File RA4/T0CKI (13-bit) Registers RA5/AN4/SS Program RAM Addr<sup>(1)</sup> **∮** 9 Bus **PORTB** RB0/INT Addr MUX Instruction reg RB1 Indirect Addr RB2 Direct Addr 8 RB3/PGM RB4 FSR reg RB5 RB6/PGC RB7/PGD STATUS reg 8 PORTC RC0/T1OSO/T1CKI RC1/T1OSI/CCP2 3 MUX Power-up Timer RC2/CCP1 RC3/SCK/SCL RC4/SDI/SDA Oscillator Start-up Timer Instruction Decode & ALU RC5/SDO Control Power-on Reset RC6/TX/CK RC7/RX/DT Timing Generation Watchdog W reg OSC1/CLKIN Brown-out OSC2/CLKOUT Reset  $\boxtimes$  $\boxtimes$ MCLR VDD, VSS Timer0 Timer1 Timer2 8-bit A/D Synchronous USART CCP1 CCP2 Serial Port

Device	Program FLASH	Data Memory
PIC16F73	4K	192 Bytes
PIC16F76	8K	368 Bytes

Note 1: Higher order bits are from the STATUS register.

13 **PORTA** Data Bus Program Counter RA0/AN0 **FLASH** RA1/AN1 Program RA2/AN2 Memory RAM RA3/AN3/VREF 8 Level Stack File RA4/T0CKI (13-bit) Registers RA5/AN4/SS Program 14 RAM Addr<sup>(1)</sup>  $\Rightarrow$  9 PORTB Bus RB0/INT Addr MUX RB1 Instruction reg RB2 Indirect Addr RB3/PGM Direct Addr 8 RB4 RB5 FSR reg RB6/PGC RB7/PGD STATUS reg 8 PORTO RC0/T1OSO/T1CKI RC1/T1OSI/CCP2 MUX RC2/CCP1 Power-up Timer RC3/SCK/SCL RC4/SDI/SDA Instruction Oscillator RC5/SDO Start-up Time ALU RC6/TX/CK Control Power-on RC7/RX/DT Reset Timing Generation **PORTD** Watchdog W reg RD0/PSP0 RD1/PSP1 Timer OSC1/CLKIN Brown-out OSC2/CLKOUT RD2/PSP2 Reset RD3/PSP3 RD4/PSP4 RD5/PSP5 RD6/PSP6 X RD7/PSP7 MCLR VDD, Vss PORTE RE0/AN5/RD RE1/AN6/WR RE2/AN7/CS Timer0 Timer1 Timer2 8-bit A/D ĮĮ J[ ĮŢ Synchronous **USART** CCP1 CCP2 Parallel Slave Port Serial Port Program FLASH Device **Data Memory** PIC16F74 4K 192 Bytes PIC16F77 8K 368 Bytes Note 1: Higher order bits are from the STATUS register.

FIGURE 1-2: PIC16F74 AND PIC16F77 BLOCK DIAGRAM

TABLE 1-2: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI OSC1	9	6	I	ST/CMOS <sup>(3)</sup>	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
CLKI			I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO OSC2	10	7	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			0		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP MCLR	1	26	I	ST	Master Clear (input) or programming voltage (output).  Master Clear (Reset) input. This pin is an active low RESET to the device.
VPP			Р		Programming voltage input.
RA0/AN0 RA0	2	27	I/O	TTL	PORTA is a bi-directional I/O port.  Digital I/O.
AN0 RA1/AN1 RA1	3	28	I I/O	TTL	Analog input 0.  Digital I/O.
AN1			I		Analog input 1.
RA2/AN2 RA2 AN2	4	1	I/O I	TTL	Digital I/O. Analog input 2.
RA3/AN3/VREF RA3 AN3 VREF	5	2	I/O I	TTL	Digital I/O. Analog input 3. A/D reference voltage input.
RA4/T0CKI RA4 T0CKI	6	4	I/O I	ST	Digital I/O – Open drain when configured as output. Timer0 external clock input.
RA5/SS/AN4 RA5 SS AN4	7	5	I/O I I	TTL	Digital I/O. SPI slave select input. Analog input 4.

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

<sup>2:</sup> This buffer is a Schmitt Trigger input when used in Serial Programming mode.3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-2: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
					PORTB is a bi-directional I/O port. PORTB can be software
				(1)	programmed for internal weak pull-up on all inputs.
RB0/INT RB0	21	18	I/O	TTL/ST <sup>(1)</sup>	Digital I/O.
INT			ı, O		External interrupt.
RB1	22	19	I/O	TTL	Digital I/O.
RB2	23	20	I/O	TTL	Digital I/O.
RB3/PGM	24	21		TTL	
RB3			I/O		Digital I/O.
PGM	0.5	00	I/O		Low voltage ICSP programming enable pin.
RB4	25	22	1/0	TTL	Digital I/O.
RB5	26	23	I/O	TTL TTL/ST <sup>(2)</sup>	Digital I/O.
RB6/PGC RB6	27	24	I/O		Digital I/O.
PGC			I/O		In-Circuit Debugger and ICSP programming clock.
RB7/PGD	28	25		TTL/ST <sup>(2)</sup>	
RB7			I/O		Digital I/O.
PGD			I/O		In-Circuit Debugger and ICSP programming data.
D00/T1000/T10//	44	•		0.7	PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI RC0	11	8	I/O	ST	Digital I/O.
T1OSO			0		Timer1 oscillator output.
T1CKI			I		Timer1 external clock input.
RC1/T1OSI/CCP2	12	9		ST	
RC1			I/O		Digital I/O.
T1OSI CCP2			  /O		Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	13	10	., 0	ST	
RC2			I/O		Digital I/O.
CCP1			I/O		Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	11	1/0	ST	D: 1: 11/0
RC3 SCK			I/O I/O		Digital I/O. Synchronous serial clock input/output for SPI mode.
SCL			I/O		Synchronous serial clock input/output for I <sup>2</sup> C mode.
RC4/SDI/SDA	15	12		ST	,
RC4			I/O		Digital I/O.
SDI			I I/O		SPI data in.
SDA PC5/SDO	16	13	I/O	ęт	I <sup>2</sup> C data I/O.
RC5/SDO RC5	סו	13	I/O	ST	Digital I/O.
SDO			0		SPI data out.
RC6/TX/CK	17	14		ST	
RC6			I/O		Digital I/O.
TX CK			O I/O		USART asynchronous transmit. USART 1 synchronous clock.
RC7/RX/DT	18	15	., 0	ST	35, it i synonionous sissit.
RC7			I/O	.	Digital I/O.
RX			I		USART asynchronous receive.
DT			I/O		USART synchronous data.
Vss	8, 19	5, 16	Р	_	Ground reference for logic and I/O pins.
VDD	20	17 O – out	Р		Positive supply for logic and I/O pins.

Legend: I = input

O = output

I/O = input/output

P = power

— = Not used

TTL = TTL input

ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F74 AND PIC16F77 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	13	14	30		ST/CMOS <sup>(4)</sup>	Oscillator crystal or external clock input.
OSC1 CLKI				I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
OLN				'		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	14	15	31		_	Oscillator crystal or clock output.
OSC2				0		Oscillator crystal output.  Connects to crystal or resonator in Crystal Oscillator
						mode.
CLKO				0		In RC mode, OSC2 pin outputs CLKO, which has 1/4
						the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP	1	2	18		ST	Master Clear (input) or programming voltage (output).
MCLR				I		Master Clear (Reset) input. This pin is an active low RESET to the device.
VPP				Р		Programming voltage input.
				·		PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19		TTL	
RA0				I/O		Digital I/O.
AN0				I		Analog input 0.
RA1/AN1	3	4	20		TTL	
RA1				I/O		Digital I/O.
AN1	_	_	04	'	TT1	Analog input 1.
RA2/AN2 RA2	4	5	21	I/O	TTL	Digital I/O.
AN2				"		Analog input 2.
RA3/AN3/VREF	5	6	22		TTL	<del></del>
RA3				I/O		Digital I/O.
AN3				- 1		Analog input 3.
VREF				I		A/D reference voltage input.
RA4/T0CKI	6	7	23		ST	B: "- IVO - O - I - I
RA4 T0CKI				I/O		Digital I/O – Open drain when configured as output. Timer0 external clock input.
RA5/SS/AN4	7	8	24	'	TTL	Timoro external clock input.
RA5	′			I/O	'''	Digital I/O.
SS				I		SPI slave select input.
AN4				I		Analog input 4.

Legend:

I = input

atuo = O

O = output

I/O = input/output

P = power

— = Not used T

TTL = TTL input

ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

- 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
- 3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
- 4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F74 AND PIC16F77 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8		TTL/ST <sup>(1)</sup>	
RB0 INT				I/O I		Digital I/O. External interrupt.
RB1	34	37	9	I/O	TTL	Digital I/O.
RB2	35	38	10	I/O	TTL	Digital I/O.
RB3/PGM	36	39	11	., 0	TTL	Eightai # C.
RB3	00			I/O		Digital I/O.
PGM				I/O		Low voltage ICSP programming enable pin.
RB4	37	41	14	I/O	TTL	Digital I/O.
RB5	38	42	15	I/O	TTL	Digital I/O.
RB6/PGC	39	43	16		TTL/ST <sup>(2)</sup>	
RB6				I/O		Digital I/O.
PGC				I/O	(0)	In-Circuit Debugger and ICSP programming clock.
RB7/PGD	40	44	17	1/0	TTL/ST <sup>(2)</sup>	D: :: 11/0
RB7 PGD				I/O I/O		Digital I/O. In-Circuit Debugger and ICSP programming data.
FGD				1/0		PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32		ST	PONTO is a bi-directional I/O port.
RC0	15	10	32	I/O	31	Digital I/O.
T10S0				0		Timer1 oscillator output.
T1CKI				1		Timer1 external clock input.
RC1/T1OSI/CCP2	16	18	35		ST	
RC1				I/O		Digital I/O.
T1OSI				I I		Timer1 oscillator input.
CCP2	47	10	00	I/O	O.T.	Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1 RC2	17	19	36	I/O	ST	Digital I/O.
CCP1				I/O		Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	18	20	37		ST	
RC3				I/O		Digital I/O
SCK				I/O		Synchronous serial clock input/output for SPI mode.
SCL				I/O		Synchronous serial clock input/output for I <sup>2</sup> C mode.
RC4/SDI/SDA	23	25	42		ST	D. 1. 11/0
RC4 SDI				I/O		Digital I/O. SPI data in.
SDA				I/O		I <sup>2</sup> C data I/O.
RC5/SDO	24	26	43		ST	
RC5				I/O	J.	Digital I/O.
SDO				0		SPI data out.
RC6/TX/CK	25	27	44		ST	
RC6				I/O		Digital I/O.
TX				0		USART asynchronous transmit.
CK	00	00		I/O	O.T.	USART 1 synchronous clock.
RC7/RX/DT RC7	26	29	1	I/O	ST	Digital I/O.
RX				,,,,, 		USART asynchronous receive.
DT				I/O		USART synchronous data.
Legend: L = input		0 - 0	·		) – innut/outni	

Legend: I = input— = Not used O = output TTL = TTL input I/O = input/output ST = Schmitt Trigger input P = power

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

- 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
- 3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
- 4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F74 AND PIC16F77 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTD is a bi-directional I/O port or parallel slave port
						when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38		ST/TTL <sup>(3)</sup>	
RD0				I/O		Digital I/O.
PSP0				I/O	o= == (3)	Parallel Slave Port data.
RD1/PSP1	20	22	39	I I/O	ST/TTL <sup>(3)</sup>	Di-it-11/O
RD1 PSP1				I/O I/O		Digital I/O. Parallel Slave Port data.
RD2/PSP2	21	23	40	I/O	ST/TTL <sup>(3)</sup>	Farallel Slave Fort data.
RD2	21	23	40	I/O	51/11L\"/	Digital I/O.
PSP2				1/0		Parallel Slave Port data.
RD3/PSP3	22	24	41	., 0	ST/TTL <sup>(3)</sup>	r dranor oldvo r ort data.
RD3			7.	I/O	01/112	Digital I/O.
PSP3				I/O		Parallel Slave Port data.
RD4/PSP4	27	30	2		ST/TTL <sup>(3)</sup>	
RD4				I/O		Digital I/O.
PSP4				I/O		Parallel Slave Port data.
RD5/PSP5	28	31	3		ST/TTL <sup>(3)</sup>	
RD5				I/O		Digital I/O.
PSP5				I/O		Parallel Slave Port data.
RD6/PSP6	29	32	4		ST/TTL <sup>(3)</sup>	
RD6				I/O		Digital I/O.
PSP6				I/O	(2)	Parallel Slave Port data.
RD7/PSP7	30	33	5		ST/TTL <sup>(3)</sup>	D: :: 11/0
RD7 PSP7				I/O I/O		Digital I/O. Parallel Slave Port data.
P3P7				1/0		
DEO (DD (ANIE		•	0.5		OT (TT) (3)	PORTE is a bi-directional I/O port.
RE0/RD/AN5	8	9	25	I/O	ST/TTL <sup>(3)</sup>	District I/O
RE0 RD				I/O I		Digital I/O.  Read control for parallel slave port .
AN5				i		Analog input 5.
RE1/WR/AN6	9	10	26		ST/TTL <sup>(3)</sup>	, malog input of
RE1		10	20	I/O	01/112	Digital I/O.
WR				Ī		Write control for parallel slave port.
AN6				1		Analog input 6.
RE2/CS/AN7	10	11	27		ST/TTL <sup>(3)</sup>	
RE2				I/O		Digital I/O.
CS				1		Chip select control for parallel slave port.
AN7				I		Analog input 7.
Vss	12,31	13,34	6,29	Р		Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	Р		Positive supply for logic and I/O pins.
NC	-	1,17,2	12,13,		_	These pins are not internally connected. These pins should
		8, 40	33, 34			be left unconnected.

Legend: I = input O = output I/O = input/output P = power - = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

<sup>2:</sup> This buffer is a Schmitt Trigger input when used in Serial Programming mode.

<sup>3:</sup> This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

<sup>4:</sup> This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

#### 2.0 **MEMORY ORGANIZATION**

There are two memory blocks in each of these PICmicro® MCUs. The Program Memory and Data Memory have separate buses so that concurrent access can occur and is detailed in this section. The Program Memory can be read internally by user code (see Section 3.0).

Additional information on device memory may be found in the PICmicro™ Mid-Range Reference Manual (DS33023).

#### 2.1 **Program Memory Organization**

The PIC16F7X devices have a 13-bit program counter capable of addressing an 8K word x 14-bit program memory space. The PIC16F77/76 devices have 8K words of FLASH program memory and the PIC16F73/74 devices have 4K words. The program memory maps for PIC16F7X devices are shown in Figure 2-1. Accessing a location above the physically implemented address will cause a wraparound.

The RESET Vector is at 0000h and the Interrupt Vector is at 0004h.

#### 2.2 **Data Memory Organization**

The Data Memory is partitioned into multiple banks, which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (STATUS<6>) and RP0 (STATUS<5>) are the bank select bits:

RP1:RP0	Bank
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and guicker access.

#### GENERAL PURPOSE REGISTER 2.2.1

The register file (shown in Figure 2-2 and Figure 2-3) can be accessed either directly, or indirectly, through the File Select Register FSR.

PIC16F76/77 PIC16F73/74 PC<12:0> PC<12:0> 13 CALL, RETURN CALL, RETURN RETETE, RETLW RETETE, RETLW Stack Level 1 Stack Level 1 Stack Level 2 Stack Level 2 Stack Level 8 Stack Level 8 RESET Vector 0000h 0000h RESET Vector Interrupt Vector Interrupt Vector 0004h 0005h 0004h 0005h Page 0 Page 0 On-Chip 07FFh 07FFh Program 0800h 0800h Memory Page 1 Page 1 On-Chip 0FFFh 0FFFh Program 1000h 1000h Memory Page 2 Unimplemented 17FFh 1800h Read as '0' Page 3 1FFFh 1FFFh

FIGURE 2-1: PROGRAM MEMORY MAPS AND STACKS FOR PIC16F7X DEVICES

FIGURE 2-2: PIC16F77/76 REGISTER FILE MAP

A	File Address	A	File Address		File Address		File Addr
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181
PCL	02h	PCL	82h	PCL	102h	PCL	182
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183
FSR	04h	FSR	84h	FSR	104h	FSR	184
PORTA	05h	TRISA	85h		105h		185
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186
PORTC	07h	TRISC	87h		107h		187
PORTD <sup>(1)</sup>	08h	TRISD <sup>(1)</sup>	88h		108h		188
PORTE <sup>(1)</sup>	09h	TRISE <sup>(1)</sup>	89h		109h		189
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18/
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18E
PIR1	0Ch	PIE1	8Ch	PMDATA	10Ch	PMCON1	180
PIR2	0Dh	PIE2	8Dh	PMADR	10Dh		180
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh		18E
TMR1H	0Fh		8Fh	PMADRH	10Fh		18F
T1CON	10h		90h		110h		190
TMR2	11h		91h		111h		191
T2CON	12h	PR2	92h		112h		192
SSPBUF	13h	SSPADD	93h		113h		193
SSPCON	14h	SSPSTAT	94h		114h		194
CCPR1L	15h		95h		115h		195
CCPR1H	16h		96h		116h		196
CCP1CON	17h		97h	General	117h	General Purpose	197
RCSTA	18h	TXSTA	98h	Purpose Register	118h	Register	198
TXREG	19h	SPBRG	99h	16 Bytes	119h	16 Bytes	199
RCREG	1Ah		9Ah		11Ah		19/
CCPR2L	1Bh		9Bh		11Bh		19E
CCPR2H	1Ch		9Ch		11Ch		190
CCP2CON	1Dh		9Dh		11Dh		190
ADRES	1Eh		9Eh		11Eh		19E
ADCON0	1Fh	ADCON1	9Fh		11Fh		19F
	20h		A0h		120h		1A(
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes	EFh	General Purpose Register 80 Bytes	16Fh	General Purpose Register 80 Bytes	1EF
	7Fh	accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h 17Fh	accesses 70h - 7Fh	1F0
Bank 0		Bank 1		Bank 2		Bank 3	• •

Unimplemented data memory locations, read as '0'.

\* Not a physical register.

Note 1: These registers are not implemented on 28-pin devices.

PIC16F74/73 REGISTER FILE MAP FIGURE 2-3:

	File Address		File Address		File Address		File Addres
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD <sup>(1)</sup>	08h	TRISD <sup>(1)</sup>	88h		108h		188h
PORTE <sup>(1)</sup>	09h	TRISE <sup>(1)</sup>	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ał
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bl
PIR1	0Ch	PIE1	8Ch	PMDATA	10Ch	PMCON1	18C
PIR2	0Dh	PIE2	8Dh	PMADR	10Dh		18DI
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh		18El
TMR1H	0Fh		8Fh	PMADRH	10Fh		18Fl
T1CON	10h		90h		110h		190ł
TMR2	11h		91h				
T2CON	12h	PR2	92h				
SSPBUF	13h	SSPADD	93h				
SSPCON	14h	SSPSTAT	94h				
CCPR1L	15h		95h				
CCPR1H	16h		96h				
CCP1CON	17h		97h				
RCSTA	18h	TXSTA	98h				
TXREG	19h	SPBRG	99h				
RCREG	1Ah		9Ah				
CCPR2L	1Bh		9Bh				
CCPR2H	1Ch		9Ch				
CCP2CON	1Dh		9Dh				
ADRES	1Eh		9Eh				
ADCON0	1Fh	ADCON1	9Fh		1005		1A0ł
	20h		A0h		120h		IAUI
General Purpose Register		General Purpose Register		accesses 20h-7Fh		accesses A0h - FFh	
96 Bytes		96 Bytes			16Fh 170h		1EF 1F0
	7Fh		FFh		17Fh		1FF
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

\* Not a physical register.

Note 1: These registers are not implemented on 28-pin devices.

#### 2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1. The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 0											
00h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	nts of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
01h	TMR0	Timer0 Mo	dule Registe	er						xxxx xxxx	45, 96
02h <sup>(4)</sup>	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
03h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
04h <sup>(4)</sup>	FSR	Indirect Da	ata Memory /	Address Poir	nter	•		•		xxxx xxxx	27, 96
05h	PORTA	_	_	PORTA Dat	a Latch when	written: POF	RTA pins wh	en read		0x 0000	32, 96
06h	PORTB	PORTB D	DRTB Data Latch when written: PORTB pins when read								34, 96
07h	PORTC	PORTC D	DRTC Data Latch when written: PORTC pins when read								35, 96
08h <sup>(5)</sup>	PORTD	PORTD D	ORTD Data Latch when written: PORTD pins when read							xxxx xxxx	36, 96
09h <sup>(5)</sup>	PORTE	_	_	_	_	_	RE2	RE1	RE0	xxx	39, 96
0Ah <sup>(1,4)</sup>	PCLATH	_	-	_	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	26, 96
0Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	21, 96
0Ch	PIR1	PSPIF <sup>(3)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	23, 96
0Dh	PIR2	_	1	1	_	_	_	_	CCP2IF	0	24, 96
0Eh	TMR1L	Holding Re	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register							xxxx xxxx	50, 96
0Fh	TMR1H	Holding Re	egister for the	e Most Signi	ficant Byte of	the 16-bit TM	IR1 Registe	r		xxxx xxxx	50, 96
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	47, 96
11h	TMR2	Timer2 Mo	dule Registe	er						0000 0000	52, 96
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	52, 96
13h	SSPBUF	Synchrono	ous Serial Po	rt Receive B	uffer/Transmi	t Register				xxxx xxxx	64, 68, 96
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	61, 96
15h	CCPR1L	Capture/C	ompare/PWI	M Register1	(LSB)					xxxx xxxx	56, 96
16h	CCPR1H	Capture/C	ompare/PWI	M Register1	(MSB)					xxxx xxxx	56, 96
17h	CCP1CON	_	_	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	54, 96
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	70, 96
19h	TXREG	USART Tr	ansmit Data	Register						0000 0000	74, 96
1Ah	RCREG	USART R	eceive Data	Register						0000 0000	76, 96
1Bh	CCPR2L	Capture/C	ompare/PWI	M Register2	(LSB)					xxxx xxxx	58, 96
1Ch	CCPR2H	Capture/C	ompare/PWI	M Register2	(MSB)	<del>i</del>	<del>.</del>	<del> </del>	<del>i</del>	xxxx xxxx	58, 96
1Dh	CCP2CON	_	_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	54, 96
1Eh	ADRES	A/D Resul	A/D Result Register Byte							xxxx xxxx	88, 96
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/ DONE	_	ADON	0000 00-0	83, 96

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

- 2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset.
- 3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.
- 4: These registers can be addressed from any bank.
- 5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.
- 6: This bit always reads as a '1'.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 1											
80h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	nts of FSR to	address data	a memory (r	ot a physica	al register)	0000 0000	27, 96
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
82h <sup>(4)</sup>	PCL	Program C	Counter's (PC	C) Least Sign	ificant Byte					0000 0000	26, 96
83h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
84h <sup>(4)</sup>	FSR	Indirect da	ta memory a	ddress point	ter	•			•	xxxx xxxx	27, 96
85h	TRISA	_	_	PORTA Dat	a Direction R	egister				11 1111	32, 96
86h	TRISB	PORTB D	ata Direction	Register						1111 1111	34, 96
87h	TRISC	PORTC D	ata Direction	Register						1111 1111	35, 96
88h <sup>(5)</sup>	TRISD	PORTD D	ata Direction	Register						1111 1111	36, 96
89h <sup>(5)</sup>	TRISE	IBF	OBF	IBOV	BOV PSPMODE — PORTE Data Direction Bits						38, 96
8Ah <sup>(1,4)</sup>	PCLATH	_	1	1	Write Buffer	Vrite Buffer for the upper 5 bits of the Program Counter					21, 96
8Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
8Ch	PIE1	PSPIE <sup>(3)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	22, 96
8Dh	PIE2	_	1	1	_	_	_	1	CCP2IE	0	24, 97
8Eh	PCON	_	-	-	_	_	_	POR	BOR	qq	25, 97
8Fh	_	Unimplem	ented							_	_
90h	_	Unimplem	ented							_	_
91h	_	Unimplem	ented							_	_
92h	PR2	Timer2 Pe	riod Register	r						1111 1111	52, 97
93h	SSPADD	Synchrono	ous Serial Po	rt (I <sup>2</sup> C mode	) Address Re	gister				0000 0000	68, 97
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	60, 97
95h	_	Unimplem	ented							-	_
96h	_	Unimplem	ented							_	_
97h	_	Unimplem	ented							_	_
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	69, 97
99h	SPBRG	Baud Rate	Generator F	Register						0000 0000	71, 97
9Ah	_	Unimplem	ented							_	
9Bh	_	Unimplem	ented							_	
9Ch	_	Unimplem	ented							_	
9Dh	_	Unimplem	ented							_	
9Eh	_	Unimplem	ented							_	
9Fh	ADCON1	_	_	_	_	_	PCFG2	PCFG1	PCFG0	000	84, 97

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

- 2: Other (non power-up) RESETS include external RESET through MCLR and Watchdog Timer Reset.
- 3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.
- 4: These registers can be addressed from any bank.
- 5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.
- 6: This bit always reads as a '1'.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
101h	TMR0	Timer0 Mo	odule Registe	er						xxxx xxxx	45, 96
102h <sup>(4)</sup>	PCL	Program 0	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
103h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
104h <sup>(4)</sup>	FSR	Indirect Da	ata Memory /	Address Poir	nter					xxxx xxxx	27, 96
105h	_	Unimplem	ented							_	_
106h	PORTB	PORTB D	ata Latch wh	en written: F	ORTB pins w	hen read				xxxx xxxx	34, 96
107h	_	Unimplem	ented							_	_
108h	_	Unimplem	ented							_	_
109h	_	Unimplem	ented							_	_
10Ah <sup>(1,4)</sup>	PCLATH	_	— — Write Buffer for the upper 5 bits of the Program Counter							0 0000	21, 96
10Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
10Ch	PMDATA	Data Regi	Data Register Low Byte								29, 97
10Dh	PMADR	Address F	Register Low	Byte						xxxx xxxx	29, 97
10Eh	PMDATH	— — Data Register High Byte							xxxx xxxx	29, 97	
10Fh	PMADRH	— — Address Register High Byte							xxxx xxxx	29, 97	
Bank 3											
180h <sup>(4)</sup>	INDF	Addressin	g this locatio	n uses conte	ents of FSR to	address data	a memory (r	not a physica	al register)	0000 0000	27, 96
181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
182h <sup>(4)</sup>	PCL	Program (	Counter (PC)	Least Signif	icant Byte					0000 0000	26, 96
183h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	19, 96
184h <sup>(4)</sup>	FSR	Indirect Da	ata Memory /	Address Poir	nter					xxxx xxxx	27, 96
185h	_	Unimplem	ented							_	_
186h	TRISB	PORTB D	ata Direction	Register						1111 1111	34, 96
187h	_	Unimplem	ented							_	_
188h	_	Unimplem	ented							_	_
189h	_	Unimplem	ented							_	_
18Ah <sup>(1,4)</sup>	PCLATH	_	_	_	Write Buffer	for the upper	5 bits of the	Program C	ounter	0 0000	21, 96
18Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	23, 96
18Ch	PMCON1	(6)	_	_	_	_	_		RD	10	29, 97
18Dh	_	Unimplem	ented								
18Eh	_	Reserved maintain clear								0000 0000	
18Fh	_	Reserved	Reserved maintain clear 0000 0000								

Legend: x = unknown, u = unchanged, q = value depends on condition, -= unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

- $\begin{tabular}{ll} \bf 2: & Other \ (non\ power-up)\ RESETS\ include\ external\ RESET\ through\ \overline{MCLR}\ and\ Watchdog\ Timer\ Reset. \end{tabular}$
- 3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.
- 4: These registers can be addressed from any bank.
- 5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.
- 6: This bit always reads as a '1'.

#### 2.2.2.1 STATUS Register

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are not writable, therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note 1: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

### REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	DC	С
bit 7							bit 0

bit 7 IRP: Register Bank Select bit (used for indirect addressing)

1 = Bank 2, 3 (100h - 1FFh)

0 = Bank 0, 1 (00h - FFh)

bit 6-5 RP1:RP0: Register Bank Select bits (used for direct addressing)

11 = Bank 3 (180h - 1FFh)

10 = Bank 2 (100h - 17Fh)

01 = Bank 1 (80h - FFh)

00 = Bank 0 (00h - 7Fh)

Each bank is 128 bytes

bit 4 **TO**: Time-out bit

1 = After power-up, CLRWDT instruction, or SLEEP instruction

0 = A WDT time-out occurred

bit 3 **PD**: Power-down bit

1 = After power-up or by the CLRWDT instruction

0 = By execution of the SLEEP instruction

bit 2 z: Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1 DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)

1 = A carry-out from the 4th low order bit of the result occurred

0 = No carry-out from the 4th low order bit of the result

bit 0 C: Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)

1 = A carry-out from the Most Significant bit of the result occurred

0 = No carry-out from the Most Significant bit of the result occurred

**Note:** For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

#### 2.2.2.2 OPTION REG Register

The OPTION\_REG register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

**Note:** To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

#### REGISTER 2-2: OPTION REG REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 RBPU: PORTB Pull-up Enable bit

1 = PORTB pull-ups are disabled

0 = PORTB pull-ups are enabled by individual port latch values

bit 6 INTEDG: Interrupt Edge Select bit

1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin

bit 5 TOCS: TMR0 Clock Source Select bit

1 = Transition on RA4/T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4 T0SE: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on RA4/T0CKI pin

0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000 001 010 011 100 101 110	1:2 1:4 1:8 1:16 1:32 1:64 1:128	1:1 1:2 1:4 1:8 1:16 1:32 1:64
111	1:256	1:128

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

#### 2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

#### REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF
bit 7							bit 0

Note:

bit 7 GIE: Global Interrupt Enable bit

1 = Enables all unmasked interrupts

0 = Disables all interrupts

bit 6 **PEIE**: Peripheral Interrupt Enable bit

1 = Enables all unmasked peripheral interrupts

0 = Disables all peripheral interrupts

bit 5 TMR0IE: TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 interrupt

0 = Disables the TMR0 interrupt

bit 4 INTE: RB0/INT External Interrupt Enable bit

1 = Enables the RB0/INT external interrupt

0 = Disables the RB0/INT external interrupt

bit 3 RBIE: RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt

0 = Disables the RB port change interrupt

bit 2 TMR0IF: TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)

0 = TMR0 register did not overflow

bit 1 INTF: RB0/INT External Interrupt Flag bit

1 = The RB0/INT external interrupt occurred (must be cleared in software)

0 = The RB0/INT external interrupt did not occur

bit 0 RBIF: RB Port Change Interrupt Flag bit

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)

0 = None of the RB7:RB4 pins have changed state

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

#### 2.2.2.4 PIE1 Register

The PIE1 register contains the individual enable bits for the peripheral interrupts. **Note:** Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

#### REGISTER 2-4: PIE1 REGISTER (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

hit 7	PSPIE <sup>(1)</sup> : Parallel Slave Port Read/Write Interrupt Enable bit
nit /	<b>PSPIE</b> 17: Parallel Slave Port Bead/Write Interrupt Enable bit

1 = Enables the PSP read/write interrupt

0 = Disables the PSP read/write interrupt

bit 6 ADIE: A/D Converter Interrupt Enable bit

1 = Enables the A/D converter interrupt

0 = Disables the A/D converter interrupt

bit 5 RCIE: USART Receive Interrupt Enable bit

1 = Enables the USART receive interrupt

0 = Disables the USART receive interrupt

bit 4 TXIE: USART Transmit Interrupt Enable bit

1 = Enables the USART transmit interrupt

0 = Disables the USART transmit interrupt

bit 3 SSPIE: Synchronous Serial Port Interrupt Enable bit

1 = Enables the SSP interrupt

0 = Disables the SSP interrupt

bit 2 CCP1IE: CCP1 Interrupt Enable bit

1 = Enables the CCP1 interrupt

0 = Disables the CCP1 interrupt

bit 1 TMR2IE: TMR2 to PR2 Match Interrupt Enable bit

1 = Enables the TMR2 to PR2 match interrupt

0 = Disables the TMR2 to PR2 match interrupt

bit 0 TMR1IE: TMR1 Overflow Interrupt Enable bit

1 = Enables the TMR1 overflow interrupt

0 = Disables the TMR1 overflow interrupt

Note 1: PSPIE is reserved on 28-pin devices; always maintain this bit clear.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### 2.2.2.5 PIR1 Register

The PIR1 register contains the individual flag bits for the peripheral interrupts. Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt bits are clear prior to enabling an interrupt.

#### REGISTER 2-5: PIR1 REGISTER (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF

Note:

bit 7 bit 0

bit 7 **PSPIF**<sup>(1)</sup>: Parallel Slave Port Read/Write Interrupt Flag bit

1 = A read or a write operation has taken place (must be cleared in software)

0 = No read or write has occurred

bit 6 ADIF: A/D Converter Interrupt Flag bit

1 = An A/D conversion is completed (must be cleared in software)

0 = The A/D conversion is not complete

bit 5 RCIF: USART Receive Interrupt Flag bit

1 = The USART receive buffer is full

0 = The USART receive buffer is empty

bit 4 TXIF: USART Transmit Interrupt Flag bit

1 = The USART transmit buffer is empty

0 = The USART transmit buffer is full

bit 3 SSPIF: Synchronous Serial Port (SSP) Interrupt Flag

1 = The SSP interrupt condition has occurred, and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:

<u>SPI</u>

A transmission/reception has taken place.

I<sup>2</sup>C Slave

A transmission/reception has taken place.

I<sup>2</sup>C Master

A transmission/reception has taken place.

The initiated START condition was completed by the SSP module.

The initiated STOP condition was completed by the SSP module.

The initiated Restart condition was completed by the SSP module.

The initiated Acknowledge condition was completed by the SSP module.

A START condition occurred while the SSP module was IDLE (multi-master system).

A STOP condition occurred while the SSP module was IDLE (multi-master system).

0 = No SSP interrupt condition has occurred

bit 2 CCP1IF: CCP1 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

bit 1 TMR2IF: TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred

bit 0 TMR1IF: TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflowed (must be cleared in software)

0 = TMR1 register did not overflow

Note 1: PSPIF is reserved on 28-pin devices; always maintain this bit clear.

Legend:

 $R = Readable \ bit$   $W = Writable \ bit$   $U = Unimplemented \ bit$ , read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is

'0' = Bit is cleared x = Bit is unknown