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PIC16F785/HV785
Data Sheet

20-Pin Flash-Based, 8-Bit CMOS Microcontroller with Two-Phase Asynchronous Feedback PWM Dual High-Speed Comparators and Dual Operational Amplifiers

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PIC16F785/HV785

20-Pin Flash-Based 8-Bit CMOS Microcontroller

High-Performance RISC CPU:

- Only 35 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt Capability
- 8-Level Seep Hardware Stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%
  - Software selectable frequency range of 8 MHz to 32 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Power-Saving Sleep mode
- Wide Operating Voltage Range (2.0V-5.5V)
- Industrial and Extended Temperature Range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Software Control Option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip Oscillator (software selectable nominal 268 seconds with full prescaler) with Software Enable
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years

Low-Power Features:

- Standby Current:
  - 30 nA @ 2.0V, typical
- Operating Current:
  - 8.5 μA @ 32 kHz, 2.0V, typical
  - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical
- Timer1 Oscillator Current:
  - 2 μA @ 32 kHz, 2.0V, typical

Peripheral Features:

- High-Speed Comparator module with:
  - Two independent analog comparators
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - 1.2V band gap voltage reference
  - Comparator inputs and outputs externally accessible
  - < 40 ns propagation delay
  - 2 mv offset, typical
- Operational Amplifier module with 2 independent Op Amps:
  - 3 MHz GBWP, typical
  - All I/O pins externally accessible
- Two-Phase Asynchronous Feedback PWM module:
  - Complementary output with programmable dead band delay
  - Infinite resolution analog duty cycle
  - Sync Output/Input for multi-phase PWM
  - F_{OSC}/2 maximum PWM frequency
- A/D Converter:
  - 10-bit resolution and 14 channels (2 internal)
- 17 I/O pins and 1 Input-only Pin:
  - High-current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Capture, Compare, PWM module:
  - 16-bit Capture, max resolution 12.5 ns
  - Compare, max resolution 200 ns
  - 10-bit PWM with 1 output channel, max frequency 20 kHz
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Shunt Voltage Regulator (PIC16HV785 only):
  - 5 volt regulation
  - 4 mA to 50 mA shunt range

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Op Amps	Comparators	CCP	Two-Phase PWM	Timers 8/16-bit	Shunt Reg.
	Flash (words)	SRAM (bytes)	EEPROM (bytes)								
PIC16F785	2048	128	256	17+1	12+2	2	2	1	1	2/1	0
PIC16HV785	2048	128	256	17+1	12+2	2	2	1	1	2/1	1

Dual in Line Pin Diagram

20-pin PDIP, SOIC, SSOP

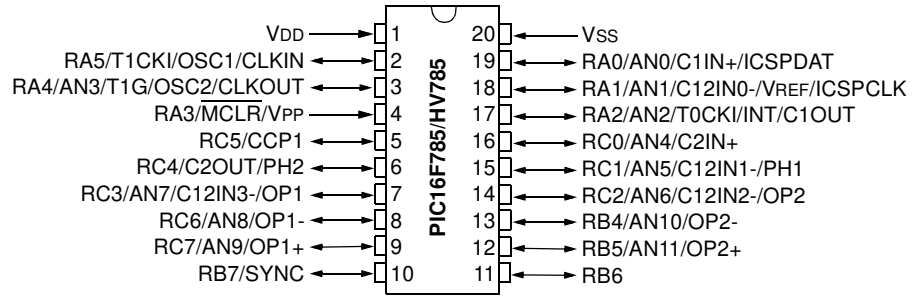

TABLE 1: DUAL IN LINE PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	19	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3(1)	4	—	—	—	—	—	—	IOC	Y	MCLR/VPP
RA4	3	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	2	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	13	AN10	—	OP2-	—	—	—	—	—	—
RB5	12	AN11	—	OP2+	—	—	—	—	—	—
RB6(2)	11	—	—	—	—	—	—	—	—	—
RB7	10	—	—	—	SYNC	—	—	—	—	—
RC0	16	AN4	C2IN+	—	—	—	—	—	—	—
RC1	15	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	14	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	7	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	6	—	C2OUT	—	PH2	—	—	—	—	—
RC5	5	—	—	—	—	—	CCP1	—	—	—
RC6	8	AN8	—	OP1-	—	—	—	—	—	—
RC7	9	AN9	—	OP1+	—	—	—	—	—	—
—	1	—	—	—	—	—	—	—	—	VDD
—	20	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Open drain.

QFN (4x4x0.9) Pin Diagram

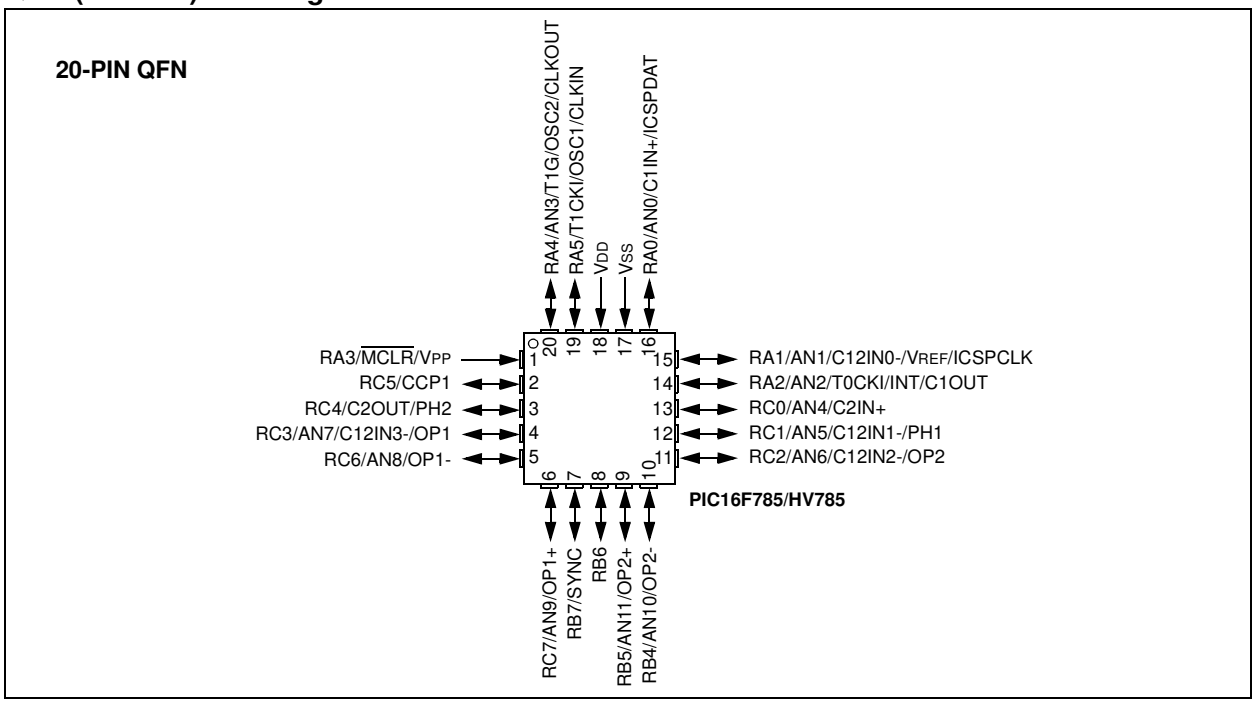

TABLE 2: QFN PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	16	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	15	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	14	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3(1)	1	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$/VPP
RA4	20	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	19	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	10	AN10	—	OP2-	—	—	—	—	—	—
RB5	9	AN11	—	OP2+	—	—	—	—	—	—
RB6(2)	8	—	—	—	—	—	—	—	—	—
RB7	7	—	—	—	SYNC	—	—	—	—	—
RC0	13	AN4	C2IN+	—	—	—	—	—	—	—
RC1	12	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	11	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	4	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	3	—	C2OUT	—	PH2	—	—	—	—	—
RC5	2	—	—	—	—	—	CCP1	—	—	—
RC6	5	AN8	—	OP1-	—	—	—	—	—	—
RC7	6	AN9	—	OP1+	—	—	—	—	—	—
—	18	—	—	—	—	—	—	—	—	VDD
—	17	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Open drain.

Table of Contents

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1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC16F785/HV785. It is available in 20-pin PDIP, SOIC, SSOP and QFN packages. Figure 1-1 shows a block diagram of the PIC16F785/HV785 device. Table 1-1 shows the pinout description.

FIGURE 1-1: PIC16F785/HV785 BLOCK DIAGRAM

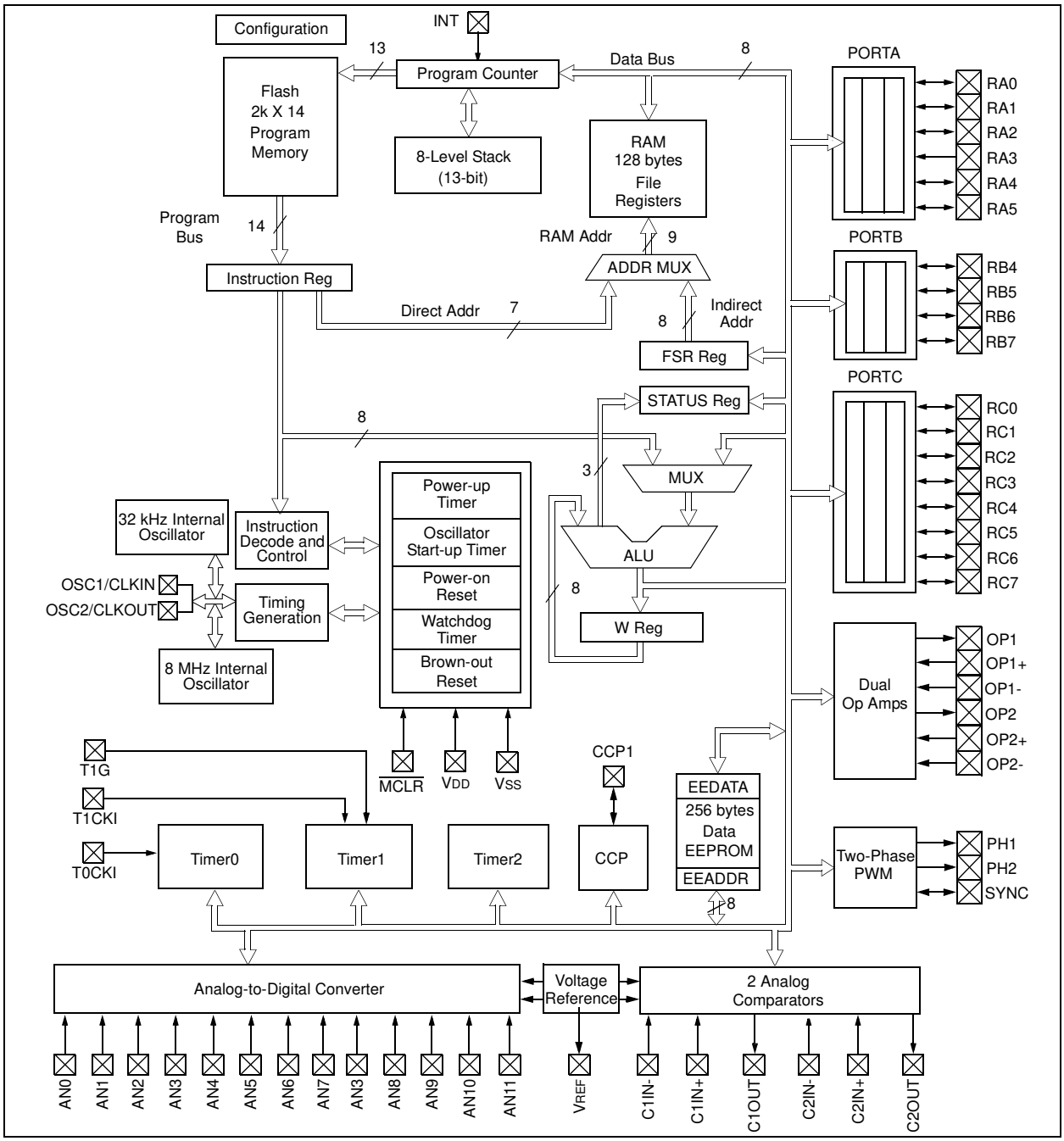


TABLE 1-1: PIC16F785/HV785 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT	RA0	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	C1IN+	AN	—	Comparator 1 non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
RA1/AN1/C12IN0-/VREF/ ICSPCLK	RA1	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	C12IN0-	AN	—	Comparator 1 and 2 inverting input
	VREF	AN	AN	External Voltage Reference for A/D, buffered reference output
	ICSPCLK	ST	—	Serial Programming Clock
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator 1 output
RA3/$\overline{\text{MCLR}}$/Vpp	RA3	TTL	—	PORTA input with prog. pull-up and interrupt-on-change
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
	VPP	HV	—	Programming voltage
RA4/AN3/T1G/OSC2/ CLKOUT	RA4	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	T1G	ST	—	Timer1 gate
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RB4/AN10/OP2-	RB4	TTL	CMOS	PORTB I/O
	AN10	AN	—	A/D Channel 10 input
	OP2-	—	AN	Op Amp 2 inverting input
RB5/AN11/OP2+	RB5	TTL	CMOS	PORTB I/O
	AN11	AN	—	A/D Channel 11 input
	OP2+	—	AN	Op Amp 2 non-inverting input
RB6	RB6	TTL	OD	PORTB I/O. Open drain output
RB7/SYNC	RB7	TTL	CMOS	PORTB I/O
	SYNC	ST	CMOS	Master PWM Sync output or slave PWM Sync input
RC0/AN4/C2IN+	RC0	TTL	CMOS	PORTC I/O
	AN4	AN	—	A/D Channel 4 input
	C2IN+	AN	—	Comparator 2 non-inverting input

Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, AN = Analog, OD = Open Drain output, HV = High Voltage

TABLE 1-1: PIC16F785/HV785 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC1/AN5/C12IN1-/PH1	RC1	TTL	CMOS	PORTC I/O
	AN5	AN	—	A/D Channel 5 input
	C12IN1-	AN	—	Comparator 1 and 2 inverting input
	PH1	—	CMOS	PWM phase 1 output
RC2/AN6/C12IN2-/OP2	RC2	TTL	CMOS	PORTC I/O
	AN6	AN	—	A/D Channel 6 input
	C12IN2-	AN	—	Comparator 1 and 2 inverting input
	OP2	—	AN	Op Amp 2 output
RC3/AN7/C12IN3-/OP1	RC3	TTL	CMOS	PORTC I/O
	AN7	AN	—	A/D Channel 7 input
	C12IN3-	AN	—	Comparator 1 and 2 inverting input
	OP1	—	AN	Op Amp 1 output
RC4/C2OUT/PH2	RC4	TTL	CMOS	PORTC I/O
	C2OUT	—	CMOS	Comparator 2 output
	PH2	—	CMOS	PWM phase 2 output
RC5/CCP1	RC5	TTL	CMOS	PORTC I/O
	CCP1	ST	CMOS	Capture input/Compare output
RC6/AN8/OP1-	RC6	TTL	CMOS	PORTC I/O
	AN8	AN	—	A/D Channel 8 input
	OP1-	AN	—	Op Amp 1 inverting input
RC7/AN9/OP1+	RC7		CMOS	PORTC I/O
	AN9	AN	—	A/D Channel 9 input
	OP1+	AN	—	Op Amp 1 non-inverting input
VSS	VSS	Power	—	Ground reference
VDD	VDD	Power	—	Positive supply

Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, AN = Analog, OD = Open Drain output, HV = High Voltage

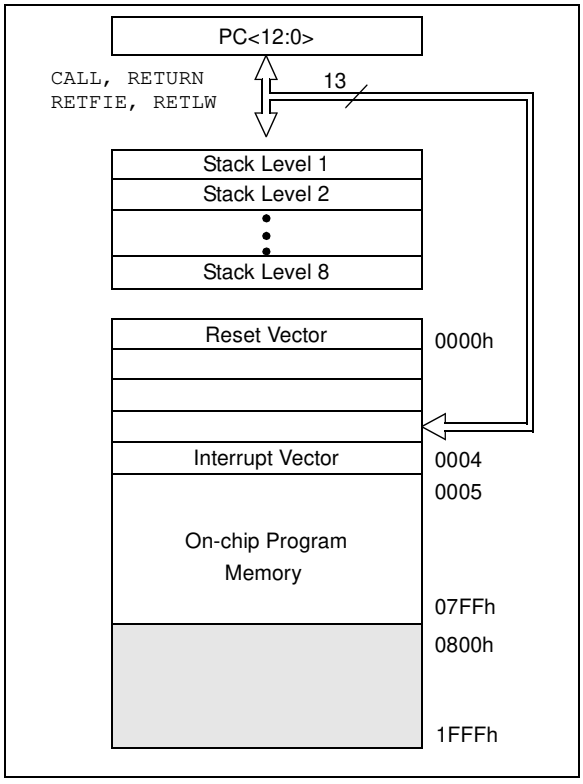
NOTES:

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F785/HV785 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2k x 14 (0000h-07FFh) for the PIC16F785/HV785 is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 2k x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F785/HV785



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into four banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. The last sixteen register locations in Bank 1 (F0h-FFh), Bank 2 (170h-17Fh), and Bank 3 (1F0h-1FFh) point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read.

Seven address bits are required to access any location in a data memory bank. Two additional bits are required to access the four banks. When data memory is accessed directly, the seven Least Significant address bits are contained within the opcode and the two Most Significant bits are contained in the STATUS register. RP0 and RP1 bits of the STATUS register are the two Most Significant data memory address bits and are also known as the bank select bits. Table 2-1 lists how to access the four banks of registers.

TABLE 2-1: BANK SELECTION

	RP1	RP0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file banks are organized as 128 x 8 in the PIC16F785/HV785. Each register is accessed, either directly, by seven address bits within the opcode, or indirectly, through the File Select Register (FSR). When the FSR is used to access data memory, the eight Least Significant data memory address bits are contained in the FSR and the ninth Most Significant address bit is contained in the IRP bit in the STATUS Register. (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-2). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2: DATA MEMORY MAP OF THE PIC16F785/HV785

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h	Indirect addr.(1)	100h	Indirect addr.(1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	PORTA	105h	TRISA	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	PORTC	107h	TRISC	187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch		10Ch	PIE1	18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	PWMCON1	110h		190h
TMR2	11h	ANSEL0	91h	PWMCON0	111h		191h
T2CON	12h	PR2	92h	PWMCLK	112h		192h
CCPR1L	13h	ANSEL1	93h	PWMPH1	113h		193h
CCPR1H	14h		94h	PWMPH2	114h		194h
CCP1CON	15h	WPUA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h		97h		117h		197h
WDTCON	18h	REFCON	98h		118h		198h
	19h	VRCON	99h	CM1CON0	119h		199h
	1Ah	EEDAT	9Ah	CM2CON0	11Ah		19Ah
	1Bh	EEADR	9Bh	CM2CON1	11Bh		19Bh
	1Ch	EECON1	9Ch	OPA1CON	11Ch		19Ch
	1Dh	EECON2(1)	9Dh	OPA2CON	11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h–6Fh	General Purpose Register 32 Bytes	A0h–BFh		120h–16Fh		1A0h–1EFh
	70h–7Fh	accesses Bank 0	F0h–FFh	accesses Bank 0	170h–17Fh	accesses Bank 0	1F0h–1FFh

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

TABLE 2-2: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
01h	TMR0	Timer0 Module's Register								xxxx xxxx	49,114
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	15,114
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
05h	PORTA(1)	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	35,114
06h	PORTB(1)	RB7	RB6	RB5	RB4	—	—	—	—	xx00 ----	42,114
07h	PORTC(1)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00xx 0000	45,114
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	19,114
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	52,114
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	52,114
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	53,114
11h	TMR2	Timer2 Module Register								0000 0000	55,114
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	55,114
13h	CCPR1L	Capture/Compare/PWM Register1 Low Byte								xxxx xxxx	58,114
14h	CCPR1H	Capture/Compare/PWM Register1 High Byte								xxxx xxxx	58,114
15h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	58,114
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	122,114
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	Most Significant 8 bits of the left justified A/D result or 2 bits of right justified result								xxxx xxxx	81,114
1Fh	ADCON0	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON	0000 0000	83,114

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
Note 1: Port pins with analog functions controlled by the ANSEL0 and ANSEL1 registers will read '0' immediately after a Reset even though the data latches are either undefined (POR) or unchanged (other Resets).

TABLE 2-3: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
81h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	17,114
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	15,114
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	35,114
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	42,114
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	45,114
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	17,114
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	18,114
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	SBOREN	—	—	$\overline{POR}$	$\overline{BOR}$	---1 --qq	20,114
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS(1)	HTS	LTS	SCS	-110 q000	33,114
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	28,114
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	82,114
92h	PR2	Timer2 Module Period Register								1111 1111	55,114
93h	ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	82,114
94h	—	Unimplemented								—	—
95h	WPUA	—	—	WPUA5	WPUA4	WPUA3(2)	WPUA2	WPUA1	WPUA0	--11 1111	36,114
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	37,114
97h	—	Unimplemented								—	—
98h	REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	--00 000-	73,114
99h	VRCON	C1VREN	C2VREN	VRR	—	VR3	VR2	VR1	VR0	000- 0000	72,114
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	103,114
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	103,114
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	104,114
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	104,114
9Eh	ADRESL	Least Significant 2 bits of the left justified A/D result or 8 bits of the right justified result								xxxx xxxx	81,114
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	84,114

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled, otherwise this bit resets to '1'.

2: RA3 pull-up is enabled when MCLRE is '1' in Configuration Word.

TABLE 2-4: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 2											
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
101h	TMR0	Timer0 Module's Register								xxxx xxxx	49,114
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	15,114
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
105h	PORTA(1)	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	35,114
106h	PORTB(1)	RB7	RB6	RB5	RB4	—	—	—	—	xx00 ----	42,114
107h	PORTC(1)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00xx 0000	45,114
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
10Ch	—	Unimplemented								—	—
10Dh	—	Unimplemented								—	—
10Eh	—	Unimplemented								—	—
10Fh	—	Unimplemented								—	—
110h	PWMCON1	—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0	-000 0000	101,114
111h	PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	93,114
112h	PWMCLK	PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0	0000 0000	94,114
113h	PWMPH1	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	95,114
114h	PWMPH2	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	96,114
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—
117h	—	Unimplemented								—	—
118h	—	Unimplemented								—	—
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	65,114
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	67,114
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	68,114
11Ch	OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	76,114
11Dh	OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	76,114
11Eh	—	Unimplemented								—	—
11Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
Note 1: Port pins with analog functions controlled by the ANSEL0 and ANSEL1 registers will read '0' immediately after a Reset even though the data latches are either undefined (POR) or unchanged (other Resets).

TABLE 2-5: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 3

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 3											
180h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
181h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	17,114
182h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
183h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	15,114
184h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
185h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	36,114
186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	42,114
187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	45,114
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
18Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
18Ch	—	Unimplemented								—	—
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	—	Unimplemented								—	—
192h	—	Unimplemented								—	—
193h	—	Unimplemented								—	—
194h	—	Unimplemented								—	—
195h	—	Unimplemented								—	—
196h	—	Unimplemented								—	—
197h	—	Unimplemented								—	—
198h	—	Unimplemented								—	—
199h	—	Unimplemented								—	—
19Ah	—	Unimplemented								—	—
19Bh	—	Unimplemented								—	—
19Ch	—	Unimplemented								—	—
19Dh	—	Unimplemented								—	—
19Eh	—	Unimplemented								—	—
19Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

2.2.2.1 STATUS Register

The STATUS register contains arithmetic status of the ALU, the Reset status and the bank select bits for data memory (SRAM).

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 17.0 "Instruction Set Summary"**.

Note:	The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS: STATUS REGISTER

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** Register Bank Select bit (used for Indirect addressing)
`1` = Bank 2,3 (100h-1FFh)
`0` = Bank 0,1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for Direct addressing)
`11` = Bank 3 (180h-1FFh)
`10` = Bank 2 (100h-17Fh)
`01` = Bank 1 (80h-FFh)
`00` = Bank 0 (00h-7Fh)

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

2.2.2.2 OPTION_REG Register

The Option register is a readable and writable register, which contains various control bits to configure the TMR0/WDT prescaler, the external RA2/INT interrupt, the TMR0 and the weak pull-ups on PORTA.

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to '1' in the OPTION Register. See **Section 5.4 "Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{RAPU}}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual port latch values in WPUA register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/AN2/T0CKI/INT/C1OUT pin
0 = Interrupt on falling edge of RA2/AN2/T0CKI/INT/C1OUT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA2/AN2/T0CKI/INT/C1OUT pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/AN2/T0CKI/INT/C1OUT pin
0 = Increment on low-to-high transition on RA2/AN2/T0CKI/INT/C1OUT pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate(1)
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available for the PIC16F785/HV785. See **Section 15.5 "Watchdog Timer (WDT)"** for more information.

2.2.2.3 INTCON Register

The Interrupt Control register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE bit of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RAIE(1)	T0IF(2)	INTF	RAIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RA2/AN2/T0CKI/INT/C1OUT External Interrupt Enable bit
1 = Enables the RA2/AN2/T0CKI/INT/C1OUT external interrupt
0 = Disables the RA2/AN2/T0CKI/INT/C1OUT external interrupt

bit 3 **RAIE:** PORTA Change Interrupt Enable bit(1)
1 = Enables the PORTA change interrupt
0 = Disables the PORTA change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit(2)
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RA2/AN2/T0CKI/INT/C1OUT External Interrupt Flag bit
1 = The RA2/AN2/T0CKI/INT/C1OUT external interrupt occurred (must be cleared in software)
0 = The RA2/AN2/T0CKI/INT/C1OUT external interrupt did not occur

bit 0 **RAIF:** PORTA Change Interrupt Flag bit
1 = When at least one of the PORTA <5:0> pins changed state (must be cleared in software)
0 = None of the PORTA <5:0> pins have changed state

Note 1: IOCA register must also be enabled.

2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

2.2.2.4 PIE1 Register

The Peripheral Interrupt Enable Register 1 contains the interrupt enable bits, as shown in Register 2-4.

Note:	Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 6 **ADIE:** A/D Converter Interrupt Enable bit
1 = Enables the A/D converter interrupt
0 = Disables the A/D converter interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 4 **C2IE:** Comparator 2 Interrupt Enable bit
1 = Enables the Comparator 2 interrupt
0 = Disables the Comparator 2 interrupt

bit 3 **C1IE:** Comparator 1 Interrupt Enable bit
1 = Enables the Comparator 1 interrupt
0 = Disables the Comparator 1 interrupt

bit 2 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the Oscillator Fail interrupt
0 = Disables the Oscillator Fail interrupt

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

2.2.2.5 PIR1 Register

The Peripheral Interrupt Register 1 contains the interrupt flag bits.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE, in the INTCON Register). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started

bit 6 **ADIF:** A/D Interrupt Flag bit
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 4 **C2IF:** Comparator 2 Interrupt Flag bit
1 = Comparator 2 output has changed (must be cleared in software)
0 = Comparator 2 output has not changed

bit 3 **C1IF:** Comparator 1 Interrupt Flag bit
1 = Comparator 1 output has changed (must be cleared in software)
0 = Comparator 1 output has not changed

bit 2 **OSFIF:** Oscillator Fail Interrupt Flag bit
1 = System oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = System clock operating

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed

2.2.2.6 PCON Register

The Power Control register contains flag bits to allow differentiation between a Power-on Reset ($\overline{POR}$), a Brown-out Reset ($\overline{BOR}$), a Watchdog Timer (WDT) Reset (WDT) and an external $\overline{MCLR}$ Reset.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	R/W-1	U-0	U-0	R/W-0	R/W-x
	—	—	—	SBOREN(1)	—	—	$\overline{POR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SBOREN:** Software BOR Enable bit(1)
- 1 = BOR enabled
- 0 = BOR disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
- 1 = No Brown-out Reset occurred
- 0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: BOREN<1:0> = 01 in Configuration Word for this bit to control the $\overline{BOR}$.

2.3 PCL and PCLATH

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The program counter is 13 bits wide. The low byte is called the PCL register. The PCL register is readable and writable. The high byte of the PC Register is called the PCH register. This register contains PC<12:8> bits which are not directly readable or writable. All updates to the PCH register goes through the PCLATH register.

On any Reset, the PC is cleared. Figure 2-3 shows the two situations for loading the PC. The upper example of Figure 2-3 shows how the PC is loaded on a write to PCL in the PCLATH Register→ PCH. The lower example of Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction in the PCLATH Register→ PCH).

2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

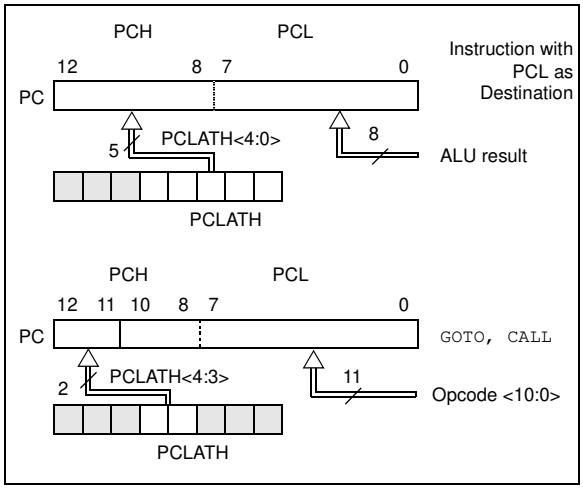
A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 PROGRAM MEMORY PAGING

The CALL and GOTO instructions provide 11 bits of address to allow branching within any 2K program memory page. When using a CALL or GOTO instruction, the Most Significant bits of the address are provided by PCLATH<4:3> (page select bits). When using a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired destination program memory page is addressed. When the CALL instruction (or interrupt) is executed, the entire 13-bit PC return address is PUSHed onto the stack. Therefore, manipulation of the PCLATH<4:3> bits are not required for the RETURN or RETFIE instructions (which POPs the address from the stack).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.3 STACK

The PIC16F785/HV785 family has an 8-level deep x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth PUSH overwrites the value that was stored from the first PUSH. The tenth PUSH overwrites the second PUSH (and so on).

Note 1:	There are no Status bits to indicate stack overflow or stack underflow conditions.
2:	There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

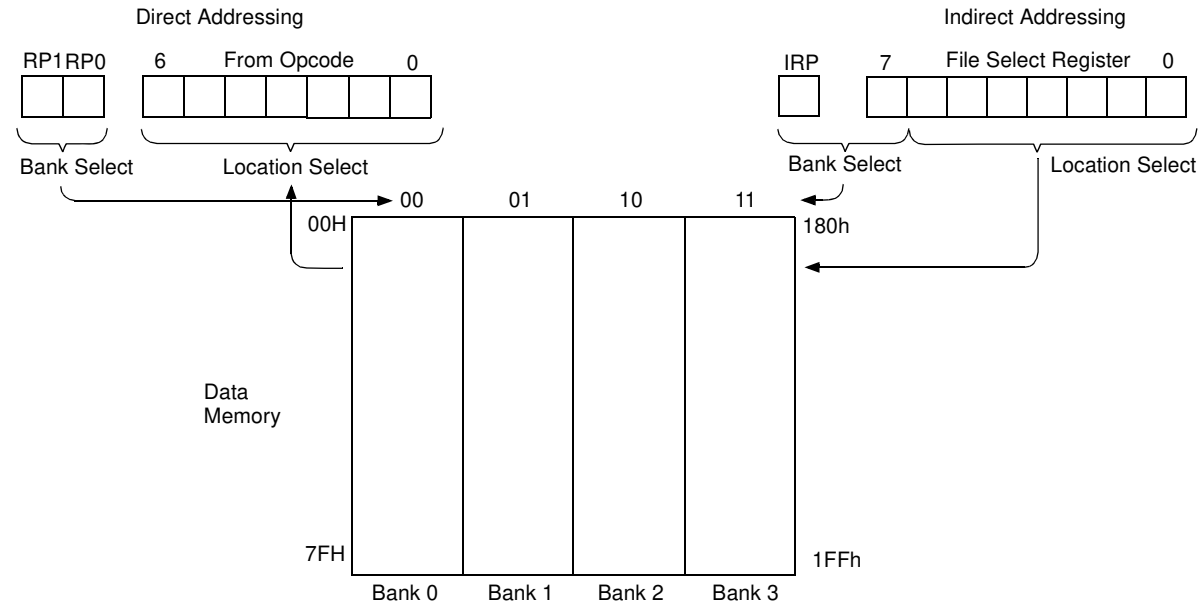
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit in the STATUS Register, as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
      MOVLW  0x20   ;initialize pointer
      MOVWF  FSR    ;to RAM
NEXT  CLRF   INDF   ;clear INDF register
      INCF   FSR    ;increment pointer
      BTFSS  FSR,4  ;all done?
      GOTO   NEXT   ;no clear next
CONTINUE            ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F785/HV785



Note: For memory map detail see Figure 2-2.

3.0 CLOCK SOURCES

3.1 Overview

The PIC16F785/HV785 has a wide variety of clock sources and selection features to allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the PIC16F785/HV785 clock sources.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal via software.
- Two-Speed Clock Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch to the internal oscillator.

The PIC16F785/HV785 can be configured in one of eight clock modes.

1. EC – External clock with I/O on RA4.
2. LP – 32.768 kHz Watch Crystal or Ceramic Resonator Oscillator mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with FOSC/4 output on RA4
6. RCIO – External Resistor-Capacitor with I/O on RA4.
7. INTOSC – Internal Oscillator with FOSC/4 output on RA4 and I/O on RA5.
8. INTOSCIO – Internal Oscillator with I/O on RA4 and RA5.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word (see **Section 15.0 "Special Features of the CPU"**). Once the PIC16F785/HV785 is programmed and the Clock Source mode configured, it cannot be changed in the software.

FIGURE 3-1: PIC16F785/HV785 CLOCK SOURCE BLOCK DIAGRAM