Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC16(L)F1516/7/8/9

28/40/44-Pin Flash Microcontrollers with XLP Technology

Devices Included In This Data Sheet

- PIC16F1516
- PIC16F1517
- PIC16F1518
- PIC16F1519
- PIC16LF1516
- PIC16LF1517
- PIC16LF1518
- PIC16LF1519

High-Performance RISC CPU

- C Compiler Optimized Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 20 MHz clock input @ 2.5V
  - DC – 16 MHz clock input @ 1.8V
  - DC – 200 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Memory

- Up to 28 Kbytes Linear Program Memory Addressing
- Up to 1024 Bytes Linear Data Memory Addressing
- High Endurance Flash Data Memory (HEF):
  - 128B of nonvolatile data storage
- 100K Erase/Write Cycles

Flexible Oscillator Structure

- 16 MHz Internal Oscillator Block:
  - Software selectable frequency range from 16 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Four crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

Analog Features

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 28 channels
  - Auto acquisition capability
  - Conversion available during Sleep
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
- Temperature Indicator

eXtreme Low-Power (XLP) Management PIC16LF1516/7/8/9 with XLP

- Sleep mode: 20 nA @ 1.8V, typical
- Watchdog Timer: 300 nA @ 1.8V, typical
- Secondary Oscillator: 600 nA @ 32 kHz
- Operating Current: 30 μA/MHz @ 1.8V, typical

Special Microcontroller Features

- Operating Voltage Range:
  - 2.3V-5.5V (PIC16F1516/7/8/9)
  - 1.8V-3.6V (PIC16LF1516/7/8/9)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-out Reset (LPBOR)
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Programmable Code Protection
- Low-Power Sleep mode

Peripheral Highlights

- Up to 35 I/O Pins and 1 Input-Only Pin:
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-change (IOC) pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Low-power 32 kHz secondary oscillator driver
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture/Compare (CCP) modules

- Master Synchronous Serial Port (MSSP) with SPI and I^2C with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module:
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start

PIC16(L)F151X/152X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High Endurance Flash (bytes)	I/O's(2)	ADC		Timers (8/16-bit)	EUSART	MSSP (I^2C/SPI)	CCP	Debug(1)	XLP
						10-bit (ch)	Advanced Control						
PIC16(L)F1512	(1)	2048	128	128	25	17	Y	2/1	1	1	2	I	Y
PIC16(L)F1513	(1)	4096	256	128	25	17	Y	2/1	1	1	2	I	Y
PIC16(L)F1516	(2)	8192	512	128	25	17	N	2/1	1	1	2	I	Y
PIC16(L)F1517	(2)	8192	512	128	36	28	N	2/1	1	1	2	I	Y
PIC16(L)F1518	(2)	16384	1024	128	25	17	N	2/1	1	1	2	I	Y
PIC16(L)F1519	(2)	16384	1024	128	36	28	N	2/1	1	1	2	I	Y
PIC16(L)F1526	(3)	8192	768	128	54	30	N	6/3	2	2	10	I	Y
PIC16(L)F1527	(3)	16384	1536	128	54	30	N	6/3	2	2	10	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS40001624 PIC16(L)F1512/13 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.

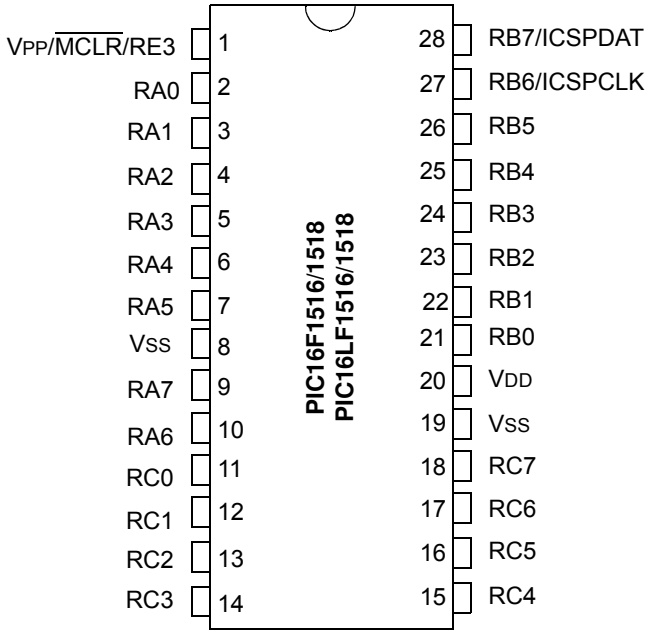
2: DS40001452 PIC16(L)F1516/7/8/9 Data Sheet, 28/40/44-Pin Flash, 8-bit MCUs.

3: DS40001458 PIC16(L)F1526/27 Data Sheet, 64-Pin Flash, 8-bit MCUs.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP PACKAGE DIAGRAM FOR PIC16(L)F1516/1518

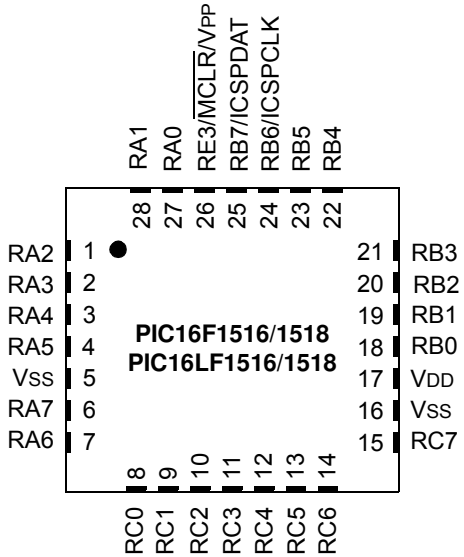
28-Pin SPDIP, SOIC, SSOP



Note: See Table 1 for location of all peripheral functions.

FIGURE 2: 28-PIN UQFN (4X4) PACKAGE DIAGRAM FOR PIC16(L)F1516/1518

28-Pin UQFN

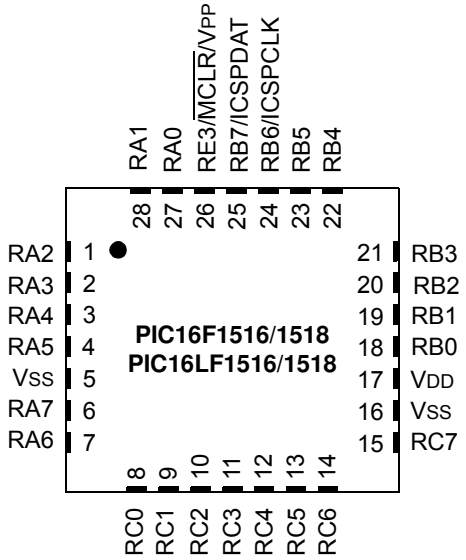


Note 1: See Table 1 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS.

FIGURE 3: 28-PIN QFN (6X6) PACKAGE DIAGRAM FOR PIC16(L)F1516/1518

28-Pin QFN

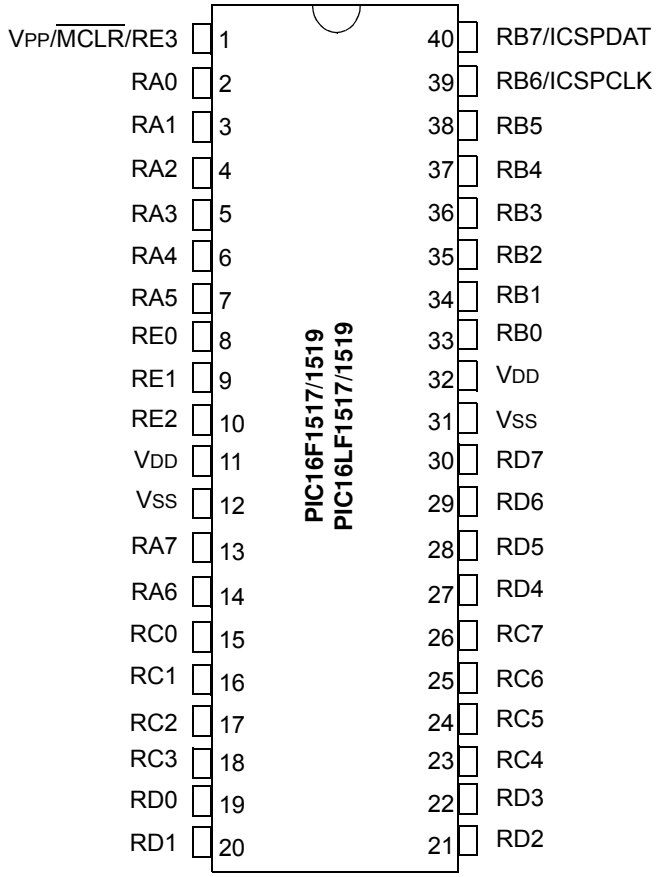


Note 1: See Table 1 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS.

FIGURE 4: 40-PIN PDIP PACKAGE DIAGRAM FOR PIC16(L)F1517/1519

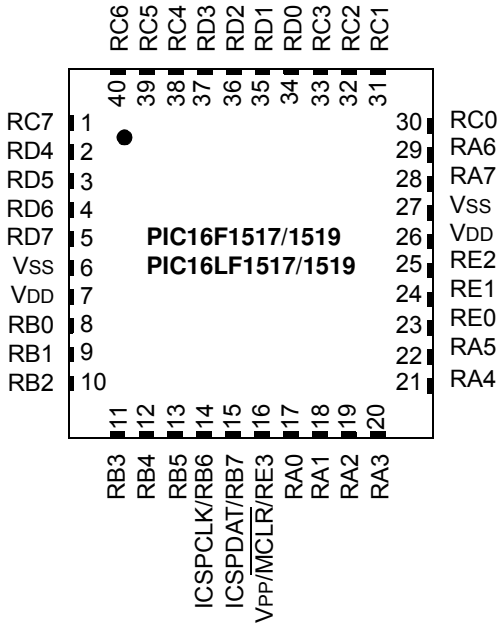
40-Pin PDIP



Note 1: See Table 1 for location of all peripheral functions.

FIGURE 5: 40-PIN UQFN (5X5) PACKAGE DIAGRAM FOR PIC16(L)F1517/1519

40-Pin UQFN

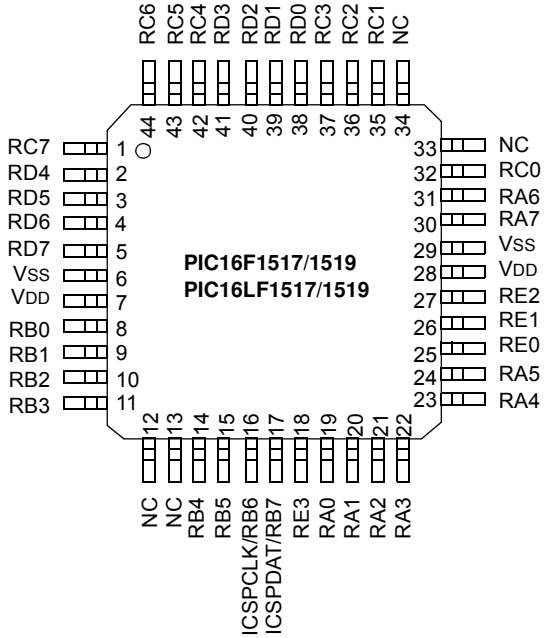


Note 1: See Table 1 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS.

FIGURE 6: 44-PIN TQFP PACKAGE DIAGRAM FOR PIC16(L)F1517/1519

44-Pin TQFP



Note: See Table 1 for location of all peripheral functions.

TABLE 1: 28/40/44-PIN ALLOCATION TABLE

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN, UQFN	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	ADC	Timers	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	2	17	19	AN0	—	—	—	$\overline{SS}$(2)	—	—	—
RA1	3	28	3	18	20	AN1	—	—	—	—	—	—	—
RA2	4	1	4	19	21	AN2	—	—	—	—	—	—	—
RA3	5	2	5	20	22	AN3/VREF+	—	—	—	—	—	—	—
RA4	6	3	6	21	23	—	T0CKI	—	—	—	—	—	—
RA5	7	4	7	22	24	AN4	—	—	—	$\overline{SS}$(1)	—	—	VCAP
RA6	10	7	14	29	31	—	—	—	—	—	—	—	OSC2/CLKOUT
RA7	9	6	13	28	30	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	21	18	33	8	8	AN12	—	—	—	—	INT/IOC	Y	—
RB1	22	19	34	9	9	AN10	—	—	—	—	IOC	Y	—
RB2	23	20	35	10	10	AN8	—	—	—	—	IOC	Y	—
RB3	24	21	36	11	11	AN9	—	CCP2(2)	—	—	IOC	Y	—
RB4	25	22	37	12	14	AN11	—	—	—	—	IOC	Y	—
RB5	26	23	38	13	15	AN13	T1G	—	—	—	IOC	Y	—
RB6	27	24	39	14	16	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	28	25	40	15	17	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	11	8	15	30	32	—	SOSCO/T1CKI	—	—	—	—	—	—
RC1	12	9	16	31	35	—	SOSCI	CCP2(1)	—	—	—	—	—
RC2	13	10	17	32	36	AN14	—	CCP1	—	—	—	—	—
RC3	14	11	18	33	37	AN15	—	—	—	SCK/SCL	—	—	—
RC4	15	12	23	38	42	AN16	—	—	—	SDI/SDA	—	—	—
RC5	16	13	24	39	43	AN17	—	—	—	SDO	—	—	—
RC6	17	14	25	40	44	AN18	—	—	TX/CK	—	—	—	—
RC7	18	15	26	1	1	AN19	—	—	RX/DT	—	—	—	—
RD0(3)	—	—	19	34	38	AN20	—	—	—	—	—	—	—
RD1(3)	—	—	20	35	39	AN21	—	—	—	—	—	—	—
RD2(3)	—	—	21	36	40	AN22	—	—	—	—	—	—	—
RD3(3)	—	—	22	37	41	AN23	—	—	—	—	—	—	—
RD4(3)	—	—	27	2	2	AN24	—	—	—	—	—	—	—
RD5(3)	—	—	28	3	3	AN25	—	—	—	—	—	—	—
RD6(3)	—	—	29	4	4	AN26	—	—	—	—	—	—	—
RD7(3)	—	—	30	5	5	AN27	—	—	—	—	—	—	—
RE0(3)	—	—	8	23	25	AN5	—	—	—	—	—	—	—
RE1(3)	—	—	9	24	26	AN6	—	—	—	—	—	—	—
RE2(3)	—	—	10	25	27	AN7	—	—	—	—	—	—	—
RE3	1	26	1	16	18	—	—	—	—	—	—	Y	$\overline{MCLR}$/VPP
VDD	20	17	11, 32	7, 26	7, 28	—	—	—	—	—	—	—	—
VSS	8, 19	5, 16	12, 31	6, 27	6, 29	—	—	—	—	—	—	—	—
NC	—	—	—	—	12, 13, 33, 34	—	—	—	—	—	—	—	—

Note 1: Peripheral pin location selected using APFCON register. Default location.

2: Peripheral pin location selected using APFCON register. Alternate location.

3: PIC16(L)F1517/9 only.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Website at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Website; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our website at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

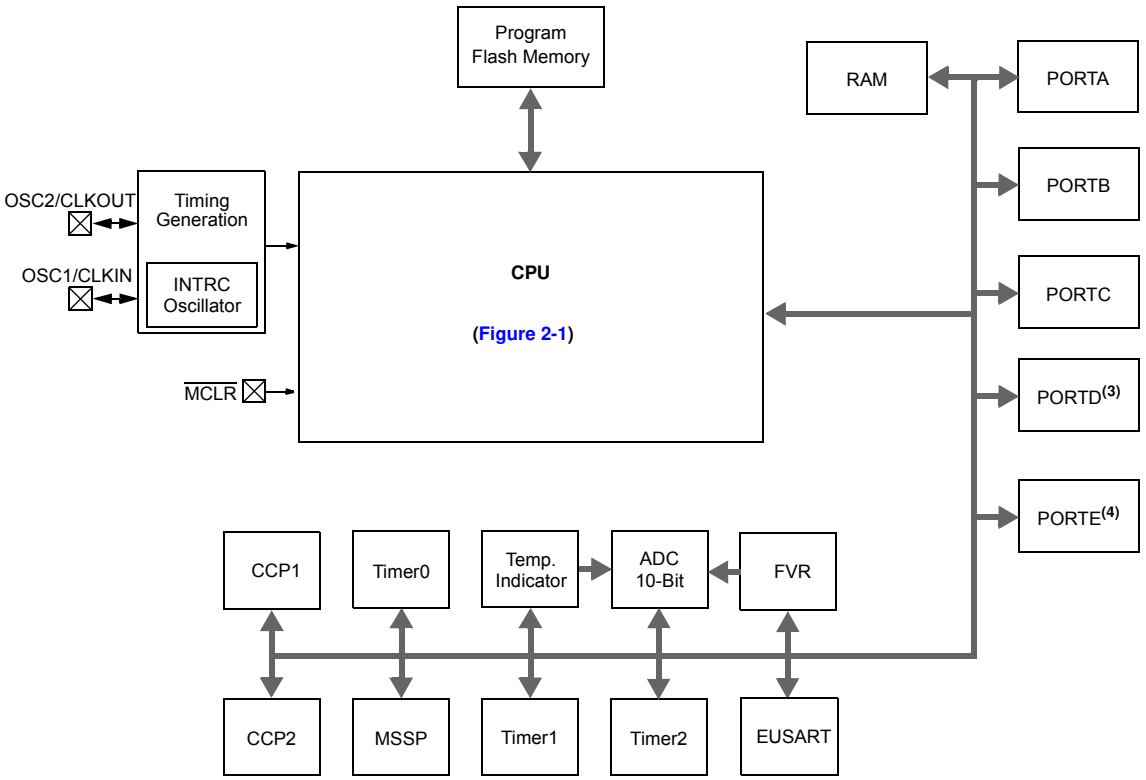
The PIC16(L)F1516/7/8/9 are described within this data sheet. Figure 1-1 shows a block diagram of the PIC16(L)F1516/7/8/9 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1516	PIC16(L)F1517	PIC16(L)F1518	PIC16(L)F1519
Analog-to-Digital Converter (ADC)		●	●	●	●
Fixed Voltage Reference (FVR)		●	●	●	●
Temperature Indicator		●	●	●	●
Capture/Compare/PWM Modules					
	CCP1	●	●	●	●
	CCP2	●	●	●	●
EUSARTs					
	EUSART	●	●	●	●
Master Synchronous Serial Ports					
	MSSP	●	●	●	●
Timers					
	Timer0	●	●	●	●
	Timer1	●	●	●	●
	Timer2	●	●	●	●

FIGURE 1-1: PIC16(L)F1516/7/8/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.
2: See Table 1-1 for peripherals available on specific devices.
3: PIC16(L)F1517/9 only.
4: RE<2:0>, PIC16(L)F1517/9 only.

TABLE 1-2: PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/$\overline{SS}$(2)	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	$\overline{SS}$	ST	—	Slave Select input.
RA1/AN1	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
RA2/AN2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
RA3/AN3/VREF+	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC Positive Voltage Reference input.
RA4/T0CKI	RA4	TTL	CMOS	General purpose I/O.
	T0CKI	ST	—	Timer0 clock input.
RA5/AN4/$\overline{SS}$(1)/VCAP	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	$\overline{SS}$	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1516/7/8/9 only).
RA6/OSC2/CLKOUT	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA7/OSC1/CLKIN	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External clock input (EC mode).
RB0/AN12/INT	RB0	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN12	AN	—	ADC Channel 12 input.
	INT	ST	—	External interrupt.
RB1/AN10	RB1	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN10	AN	—	ADC Channel 10 input.
RB2/AN8	RB2	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN8	AN	—	ADC Channel 8 input.
RB3/AN9/CCP2(2)	RB3	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN9	AN	—	ADC Channel 9 input.
	CCP2	ST	CMOS	Capture/Compare/PWM 2.
RB4/AN11	RB4	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN11	AN	—	ADC Channel 11 input.
RB5/AN13/T1G	RB5	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN13	AN	—	ADC Channel 13 input.
	T1G	ST	—	Timer1 Gate input.
RB6/ICSPCLK	RB6	TTL	CMOS	General purpose I/O with IOC and WPU.
	ICSPCLK	ST	CMOS	In-Circuit Data I/O.
RB7/ICSPDAT	RB7	TTL	CMOS	General purpose I/O with IOC and WPU.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Peripheral pin location selected using APFCON register (Register 12-1). Default location.
2: Peripheral pin location selected using APFCON register (Register 12-1). Alternate location.
3: PORTD and RE<2:0> available on PIC16(L)F1517/9 only.

TABLE 1-2: PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC0/SOSCO/T1CKI	RC0	ST	CMOS	General purpose I/O.
	SOSCO	—	XTAL	Secondary oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
RC1/SOSCI/CCP2(1)	RC1	ST	CMOS	General purpose I/O.
	SOSCI	—	XTAL	Secondary oscillator connection.
	CCP2	ST	CMOS	Capture/Compare/PWM 2.
RC2/AN14/CCP1	RC2	ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	CCP1	ST	CMOS	Capture/Compare/PWM 1.
RC3/AN15/SCK/SCL	RC3	ST	CMOS	General purpose I/O.
	AN15	AN	—	ADC Channel 15 input.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C clock.
RC4/AN16/SDI/SDA	RC4	ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C data input/output.
RC5/AN17/SDO	RC5	ST	CMOS	General purpose I/O.
	AN17	AN	—	ADC Channel 17 input.
	SDO	—	CMOS	SPI data output.
RC6/AN18/TX/CK	RC6	ST	CMOS	General purpose I/O.
	AN18	AN	—	ADC Channel 18 input.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
RC7/AN19/RX/DT	RC7	ST	CMOS	General purpose I/O.
	AN19	AN	—	ADC Channel 19 input.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
RD0(3)/AN20	RD0	ST	CMOS	General purpose I/O.
	AN20	AN	—	ADC Channel 20 input.
RD1(3)/AN21	RD1	ST	CMOS	General purpose I/O.
	AN21	AN	—	ADC Channel 21 input.
RD2(3)/AN22	RD2	ST	CMOS	General purpose I/O.
	AN22	AN	—	ADC Channel 22 input.
RD3(3)/AN23	RD3	ST	CMOS	General purpose I/O.
	AN23	AN	—	ADC Channel 23 input.
RD4(3)/AN24	RD4	ST	CMOS	General purpose I/O.
	AN24	AN	—	ADC Channel 24 input.
RD5(3)/AN25	RD5	ST	CMOS	General purpose I/O.
	AN25	AN	—	ADC Channel 25 input.
RD6(3)/AN26	RD6	ST	CMOS	General purpose I/O.
	AN26	AN	—	ADC Channel 26 input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Peripheral pin location selected using APFCON register (Register 12-1). Default location.
2: Peripheral pin location selected using APFCON register (Register 12-1). Alternate location.
3: PORTD and RE<2:0> available on PIC16(L)F1517/9 only.

TABLE 1-2: PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD7(3)/AN27	RD7	ST	CMOS	General purpose I/O.
	AN27	AN	—	ADC Channel 27 input.
RE0(3)/AN5	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
RE1(3)/AN6	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
RE2(3)/AN7	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
RE3/$\overline{MCLR}$/VPP	RE3	ST	—	General purpose input with WPU.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

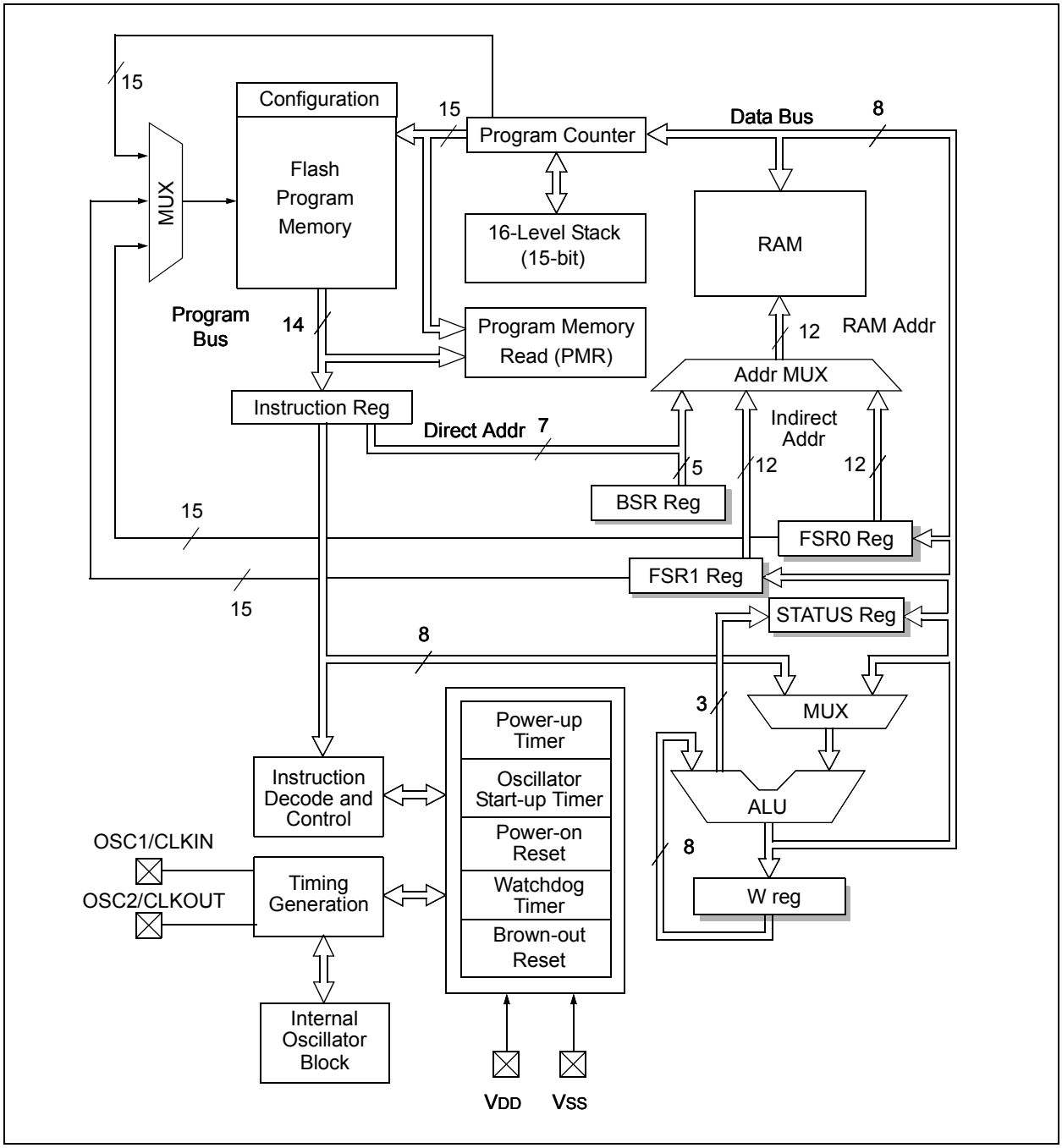
Note 1: Peripheral pin location selected using APFCON register (Register 12-1). Default location.
2: Peripheral pin location selected using APFCON register (Register 12-1). Alternate location.
3: PORTD and RE<2:0> available on PIC16(L)F1517/9 only.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See **Section 3.6 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.7 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 24.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for these devices. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1 and Figure 3-2).

3.2 High-Endurance Flash

This device has a 128-byte section of high-endurance Program Flash Memory (PFM) in lieu of data EEPROM. This area is especially well suited for nonvolatile data storage that is expected to be updated frequently over the life of the end product. See **Section 11.2 "Flash Program Memory Overview"** for more information on writing data to PFM. See **Section 3.2.1.2 "Indirect Read with FSR"** for more information about using the FSR registers to read byte data stored in PFM.

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range (1)
PIC16F1516 PIC16LF1516	8,192	1FFFh	1F80h-1FFFh
PIC16F1827 PIC16LF1517			
PIC16F1939 PIC16LF1518	16,384	3FFFh	3F80h-3FFFh
PIC16LF1933 PIC16LF1519			

Note 1: High-endurance Flash applies to the low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1516/7

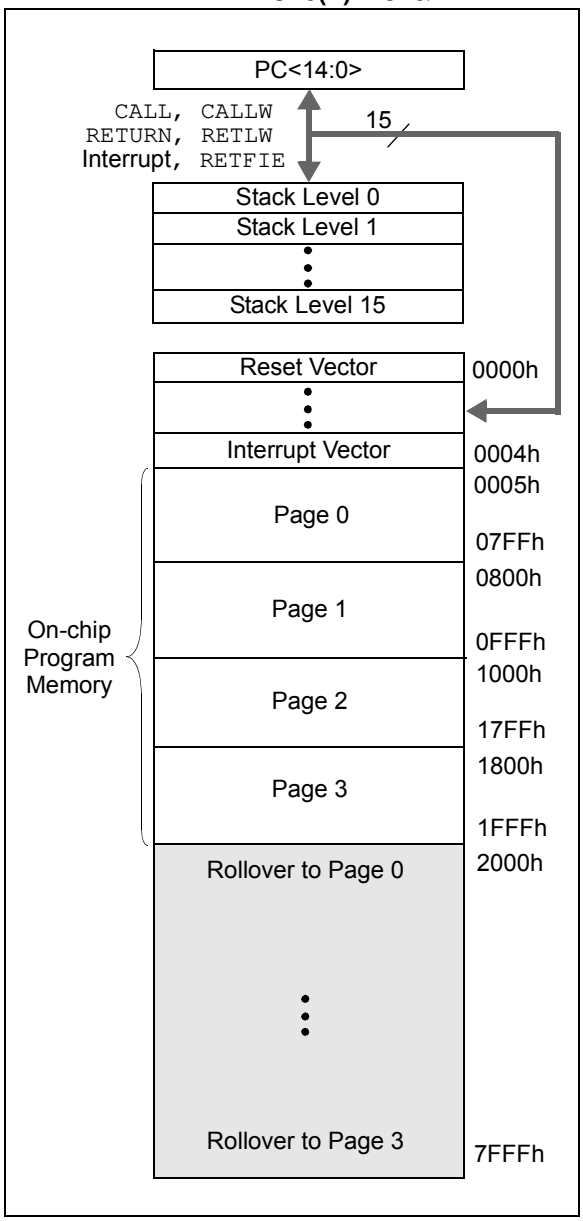
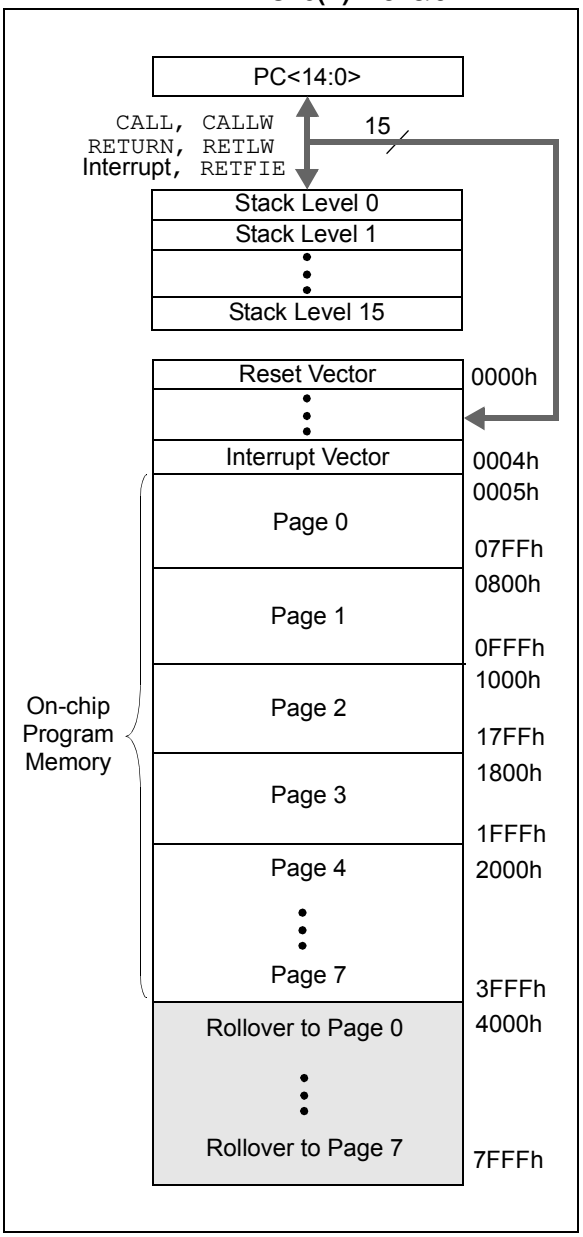


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1518/9



3.2.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.2.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    CALL constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If the code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.2.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    DW DATA0        ;First constsnt
    DW DATA1        ;Second constant
    DW DATA2        ;
    DW DATA3        ;
my_function
    ;… LOTS OF CODE…
    MOVLW   DATA_INDEX
    MOVWF   LOW constants
    MOVWF   FSR1H
    MOVLW   HIGH constants ;MSB is set
                           ;automatically
    MOVWF   FSR1H
    BTFSC   STATUS,C    ;carry from ADDLW?
    INCF    FSR1H,f     ;yes
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.3 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.7 "Indirect Addressing"** for more information.

Data Memory uses a 12-bit address. The upper five bits of the address define the Bank address, and the lower seven bits select the individual SFR, GPR and common RAM locations in that bank.

3.3.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-7.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.3.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 24.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

3.4 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

3.4.1 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.4.2 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

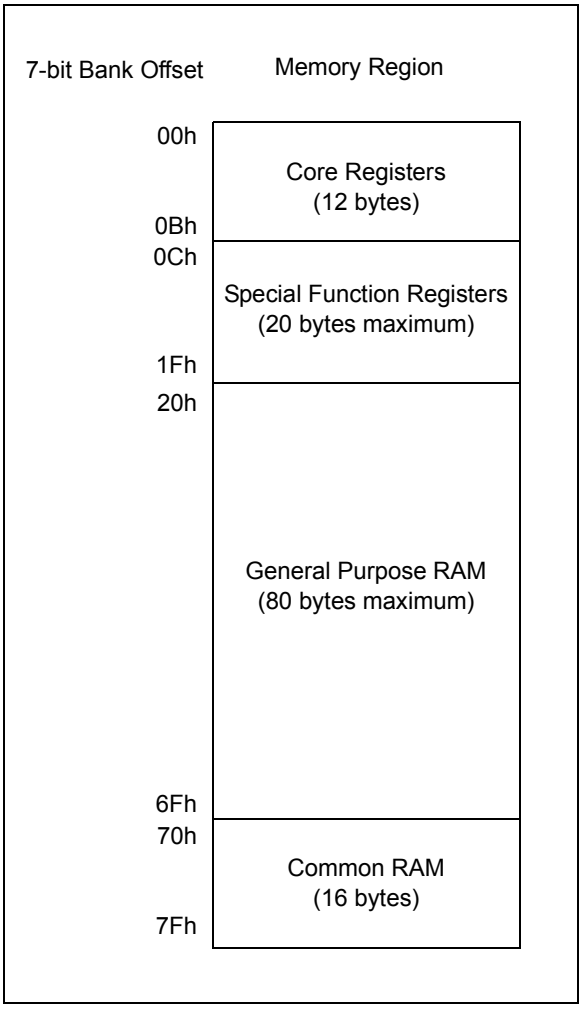
3.4.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.7.2 "Linear Data Memory"** for more information.

3.4.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.4.4 DEVICE MEMORY MAPS

The memory maps for PIC16(L)F1516/7 and PIC16(L)F1518/9 are as shown in Table 3-3 and Table 3-4, respectively.

TABLE 3-3: PIC16(L)F1516/7 MEMORY MAP

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	—	28Ch	—	30Ch	—	38Ch	—
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	PORTD(1)	08Fh	TRISD(1)	10Fh	LATD(1)	18Fh	ANSELD(1)	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	LATE(1)	190h	ANSELE(1)	210h	WPUE	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	—	191h	PMADRL	211h	SSPBUF	291h	CCPR1L	311h	—	391h	—
012h	PIR2	092h	PIE2	112h	—	192h	PMADRH	212h	SSPADD	292h	CCPR1H	312h	—	392h	—
013h	—	093h	—	113h	—	193h	PMDATL	213h	SSPMSK	293h	CCP1CON	313h	—	393h	—
014h	—	094h	—	114h	—	194h	PMDATH	214h	SSPSTAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	—	195h	PMCON1	215h	SSPCON1	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSPCON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON(2)	217h	SSPCON3	297h	—	317h	—	397h	—
018h	T1CON	098h	—	118h	—	198h	—	218h	—	298h	CCPR2L	318h	—	398h	—
019h	T1GCON	099h	OSCCON	119h	—	199h	RCREG	219h	—	299h	CCPR2H	319h	—	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TXREG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	—	19Bh	SPBRG	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SPBRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON	19Dh	RCSTA	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1	11Eh	—	19Eh	TXSTA	21Eh	—	29Eh	—	31Eh	—	39Eh	—
01Fh	—	09Fh	—	11Fh	—	19Fh	BAUDCON	21Fh	—	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 16 Bytes	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		32Fh		3EFh	
070h	Common RAM	0F0h	Common RAM (Accesses 70h – 7Fh)	170h	Common RAM (Accesses 70h – 7Fh)	1F0h	Common RAM (Accesses 70h – 7Fh)	270h	Common RAM (Accesses 70h – 7Fh)	2F0h	Common RAM (Accesses 70h – 7Fh)	330h	Unimplemented Read as '0'	3F0h	Common RAM (Accesses 70h – 7Fh)
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		36Fh		3FFh	
												370h	Common RAM (Accesses 70h – 7Fh)		
												37Fh			

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16F/LF1516/7/8/9 only.

2: PIC16F1516/7 only.

TABLE 3-3: PIC16(L)F1516/7 MEMORY MAP (CONTINUED)

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	Unimplemented Read as '0'	48Ch	Unimplemented Read as '0'	50Ch	Unimplemented Read as '0'	58Ch	Unimplemented Read as '0'	60Ch	Unimplemented Read as '0'	68Ch	Unimplemented Read as '0'	70Ch	Unimplemented Read as '0'	78Ch	Unimplemented Read as '0'
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
470h	Common RAM (Accesses 70h – 7Fh)	4F0h	Common RAM (Accesses 70h – 7Fh)	570h	Common RAM (Accesses 70h – 7Fh)	5F0h	Common RAM (Accesses 70h – 7Fh)	670h	Common RAM (Accesses 70h – 7Fh)	6F0h	Common RAM (Accesses 70h – 7Fh)	770h	Common RAM (Accesses 70h – 7Fh)	7F0h	Common RAM (Accesses 70h – 7Fh)
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	Unimplemented Read as '0'	88Ch	Unimplemented Read as '0'	90Ch	Unimplemented Read as '0'	98Ch	Unimplemented Read as '0'	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Common RAM (Accesses 70h – 7Fh)	8F0h	Common RAM (Accesses 70h – 7Fh)	970h	Common RAM (Accesses 70h – 7Fh)	9F0h	Common RAM (Accesses 70h – 7Fh)	A70h	Common RAM (Accesses 70h – 7Fh)	AF0h	Common RAM (Accesses 70h – 7Fh)	B70h	Common RAM (Accesses 70h – 7Fh)	BF0h	Common RAM (Accesses 70h – 7Fh)
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh	
C0Ch	Unimplemented Read as '0'	C8Ch	Unimplemented Read as '0'	D0Ch	Unimplemented Read as '0'	D8Ch	Unimplemented Read as '0'	E0Ch	Unimplemented Read as '0'	E8Ch	Unimplemented Read as '0'	F0Ch	Unimplemented Read as '0'
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh	
C70h	Common RAM (Accesses 70h – 7Fh)	CF0h	Common RAM (Accesses 70h – 7Fh)	D70h	Common RAM (Accesses 70h – 7Fh)	DF0h	Common RAM (Accesses 70h – 7Fh)	E70h	Common RAM (Accesses 70h – 7Fh)	EF0h	Common RAM (Accesses 70h – 7Fh)	F70h	Common RAM (Accesses 70h – 7Fh)
C7Fh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-3: PIC16(L)F1516/7 MEMORY MAP (CONTINUED)

	Bank 31
F80h F8Bh	Core Registers (Table 3-2)
F8Ch FE3h	Unimplemented Read as '0'
FE4h	STATUS_SHAD
FE5h	WREG_SHAD
FE6h	BSR_SHAD
FE7h	PCLATH_SHAD
FE8h	FSR0L_SHAD
FE9h	FSR0H_SHAD
FEAh	FSR1L_SHAD
FEBh	FSR1H_SHAD
FECh	—
FEDh	STKPTR
FEEh	TOSL
FEFh	TOSH
FF0h FFFh	Common RAM (Accesses 70h – 7Fh)

= Unimplemented data memory locations, read as '0',