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PIC16(L)F1526/7

64-Pin Flash Microcontrollers with XLP Technology

High-Performance RISC CPU

- C Compiler Optimized Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 20 MHz clock input @ 2.5V
  - DC – 16 MHz clock input @ 1.8V
  - DC – 200 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Memory

- Up to 28 Kbytes Linear Program Memory Addressing
- Up to 1536 Bytes Linear Data Memory Addressing
- High-Endurance Flash Data Memory (HEF)
  - 128B of nonvolatile data storage
  - 100K erase/write cycles

Flexible Oscillator Structure

- 16 MHz Internal Oscillator Block:
  - Software selectable frequency range from 16 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Four crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor
  - Allows safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

Special Microcontroller Features

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1526/7)
  - 2.3V to 5.5V (PIC16F1526/7)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Programmable Low-Power Brown-Out Reset (LPBOR)
- Extended Watch-Dog Timer (WDT):
  - Programmable period from 1 ms to 256s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Power-Saving Sleep mode

Extreme Low-Power Management PIC16LF1526/7 with XLP

- Sleep mode: 20 nA @ 1.8V, typical
- Watchdog Timer: 300 nA @ 1.8V, typical
- Secondary Oscillator: 600 nA @ 32 kHz, 1.8V, typical

Analog Features

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - 30 external channels
  - Two internal channels
    - Fixed Voltage Reference (FVR) channel
    - Temperature Indicator channel
  - Auto acquisition capability
  - Conversion available during Sleep
  - Dedicated ADC RC oscillator
  - Fixed Voltage Reference (FVR) as ADC positive reference
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - Low-Power Sleep mode
  - Low-Power BOR (LPBOR)

Peripheral Features

- 53 I/O Pins and One Input-only Pin:
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-change (IOC) pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1, 3, 5:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Low-power 32 kHz secondary oscillator driver
- Timer2, 4, 6, 8, 10: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Ten Capture/Compare/PWM (CCP) modules:
  - 16-bit Capture, 200 ns (max. resolution)
  - 16-bit Compare, 200 ns (max. resolution)
  - 10-bit PWM, 20 kHz @ 10 bits (max. frequency)
- Two Master Synchronous Serial Ports (MSSPs) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
  - Auto-wake-up on start
- Two Enhanced Universal Synchronous Asynchronous Receiver Transmitters (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect

PIC16(L)F151X/152X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash (bytes)	I/O's(2)	ADC		Timers (8/16-bit)	EUSART	MSSP (I^2C/SPI)	CCP	Debug(1)	XLP
						10-bit (ch)	Advanced Control						
PIC16(L)F1512	(1)	2048	128	128	25	17	Y	2/1	1	1	2	I	Y
PIC16(L)F1513	(1)	4096	256	128	25	17	Y	2/1	1	1	2	I	Y
PIC16(L)F1516	(2)	8192	512	128	25	17	N	2/1	1	1	2	I	Y
PIC16(L)F1517	(2)	8192	512	128	36	28	N	2/1	1	1	2	I	Y
PIC16(L)F1518	(2)	16384	1024	128	25	17	N	2/1	1	1	2	I	Y
PIC16(L)F1519	(2)	16384	1024	128	36	28	N	2/1	1	1	2	I	Y
PIC16(L)F1526	(3)	8192	768	128	54	30	N	6/3	2	2	10	I	Y
PIC16(L)F1527	(3)	16384	1536	128	54	30	N	6/3	2	2	10	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

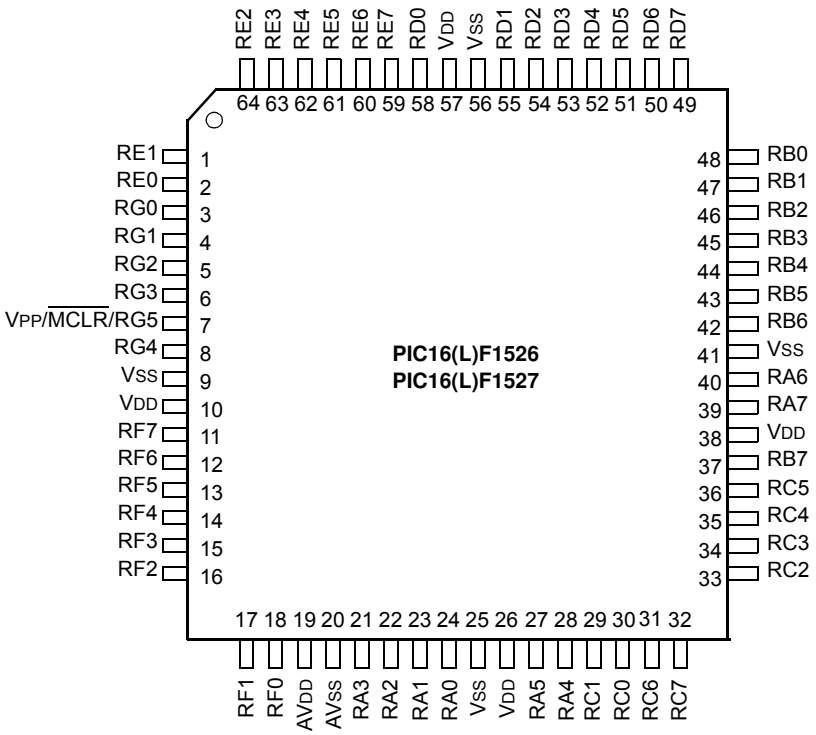
1: DS41624 PIC16(L)F1512/13 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.

2: DS41452 PIC16(L)F1516/7/8/9 Data Sheet, 28/40/44-Pin Flash, 8-bit MCUs.

3: DS41458 PIC16(L)F1526/7 Data Sheet, 64-Pin Flash, 8-bit MCUs.

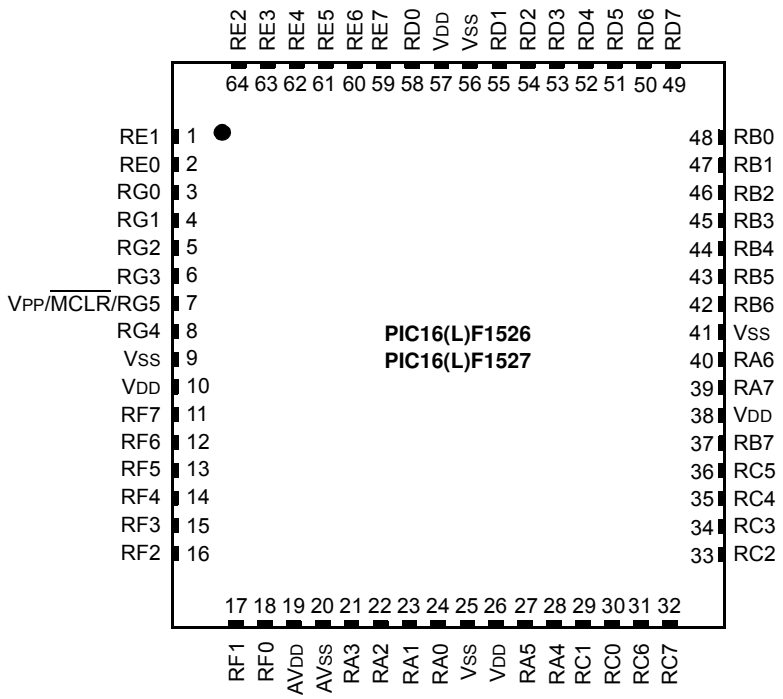
Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

FIGURE 1: 64-PIN TQFP (10MM X 10MM) PACKAGE DIAGRAM FOR PIC16(L)F1526/7



Note 1: See Table 1 for list of pin peripheral function.

FIGURE 2: 64-PIN QFN (9MM X 9MM) PACKAGE DIAGRAM FOR PIC16(L)F1526/7



Note 1: See Table 1 for list of pin peripheral function.

TABLE 1: 64-PIN DEVICE ALLOCATION TABLE (PIC16(L)F1526/7)

I/O	64-Pin TQFP, QFN	ADC	Timers	CCP	USART	SSP	Interrupt	Pull-up	Basic
RA0	24	AN0	—	—	—	—	—	—	—
RA1	23	AN1	—	—	—	—	—	—	—
RA2	22	AN2	—	—	—	—	—	—	—
RA3	21	AN3	—	—	—	—	—	—	VREF+
RA4	28	—	T0CKI	—	—	—	—	—	—
RA5	27	AN4	T3G	—	—	—	—	—	—
RA6	40	—	—	—	—	—	—	—	OSC2/CLKOUT
RA7	39	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	48	AN17	—	—	—	—	INT/ IOC	Y	—
RB1	47	AN18	—	—	—	—	IOC	Y	—
RB2	46	AN19	—	—	—	—	IOC	Y	—
RB3	45	AN20	—	—	—	—	IOC	Y	—
RB4	44	AN21	T3CKI(1)	—	—	—	IOC	Y	—
RB5	43	AN22	T1G/T3CKI	—	—	—	IOC	Y	—
RB6	42	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	37	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	30	—	SOSCO/T1CKI	—	—	—	—	—	—
RC1	29	—	SOSCI	CCP2	—	—	—	—	—
RC2	33	—	—	CCP1	—	—	—	—	—
RC3	34	—	—	—	—	SCK1/SCL1	—	—	—
RC4	35	—	—	—	—	SDI1/SDA1	—	—	—
RC5	36	—	—	—	—	SDO1	—	—	—
RC6	31	—	—	—	TX1/CK1	—	—	—	—
RC7	32	—	—	—	RX1/DT1	—	—	—	—
RD0	58	AN23	—	—	—	—	—	Y	—
RD1	55	AN24	T5CKI	—	—	—	—	Y	—
RD2	54	AN25	—	—	—	—	—	Y	—
RD3	53	AN26	—	—	—	—	—	Y	—
RD4	52	—	—	—	—	SDO2	—	Y	—
RD5	51	—	—	—	—	SDI2, SDA2	—	Y	—
RD6	50	—	—	—	—	SCK2, SCL2	—	Y	—
RD7	49	—	—	—	—	$\overline{SS2}$	—	Y	—
RE0	2	AN27	—	—	—		—	Y	—
RE1	1	AN28	—	—	—	—	—	Y	—
RE2	64	AN29	—	CCP10	—	—	—	Y	—
RE3	63	—	—	CCP9	—	—	—	Y	—
RE4	62	—	—	CCP8	—	—	—	Y	—
RE5	61	—	—	CCP7	—	—	—	Y	—
RE6	60	—	—	CCP6	—	—	—	Y	—

Note 1: Alternate pin function selected with the APFCON (Register 12-1) register.
2: Weak pull-up is always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

TABLE 1: 64-PIN DEVICE ALLOCATION TABLE (PIC16(L)F1526/7) (CONTINUED)

I/O	64-Pin TQFP, QFN	ADC	Timers	CCP	USART	SSP	Interrupt	Pull-up	Basic
RE7	59	—	—	CCP2(1)	—	—	—	Y	—
RF0	18	AN16	—	—	—	—	—	—	VCAP
RF1	17	AN6	—	—	—	—	—	—	—
RF2	16	AN7	—	—	—	—	—	—	—
RF3	15	AN8	—	—	—	—	—	—	—
RF4	14	AN9	—	—	—	—	—	—	—
RF5	13	AN10	—	—	—	—	—	—	—
RF6	12	AN11	—	—	—	—	—	—	—
RF7	11	AN5	—	—	—	$\overline{SS1}$	—	—	—
RG0	3	—	—	CCP3	—	—	—	—	—
RG1	4	AN15	—	—	TX2/CK2	—	—	—	—
RG2	5	AN14	—	—	RX2/DT2	—	—	—	—
RG3	6	AN13	—	CCP4	—	—	—	—	—
RG4	8	AN12	T5G	CCP5	—	—	—	—	—
RG5	7	—	—	—	—	—	—	Y(2)	$\overline{MCLR}$/VPP
VDD	10, 26, 38, 57	—	—	—	—	—	—	—	VDD
VSS	9, 25, 41, 56	—	—	—	—	—	—	—	VSS
AVDD	19	—	—	—	—	—	—	—	AVDD
AVSS	20	—	—	—	—	—	—	—	AVSS

Note 1: Alternate pin function selected with the APFCON (Register 12-1) register.

2: Weak pull-up is always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

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1.0 DEVICE OVERVIEW

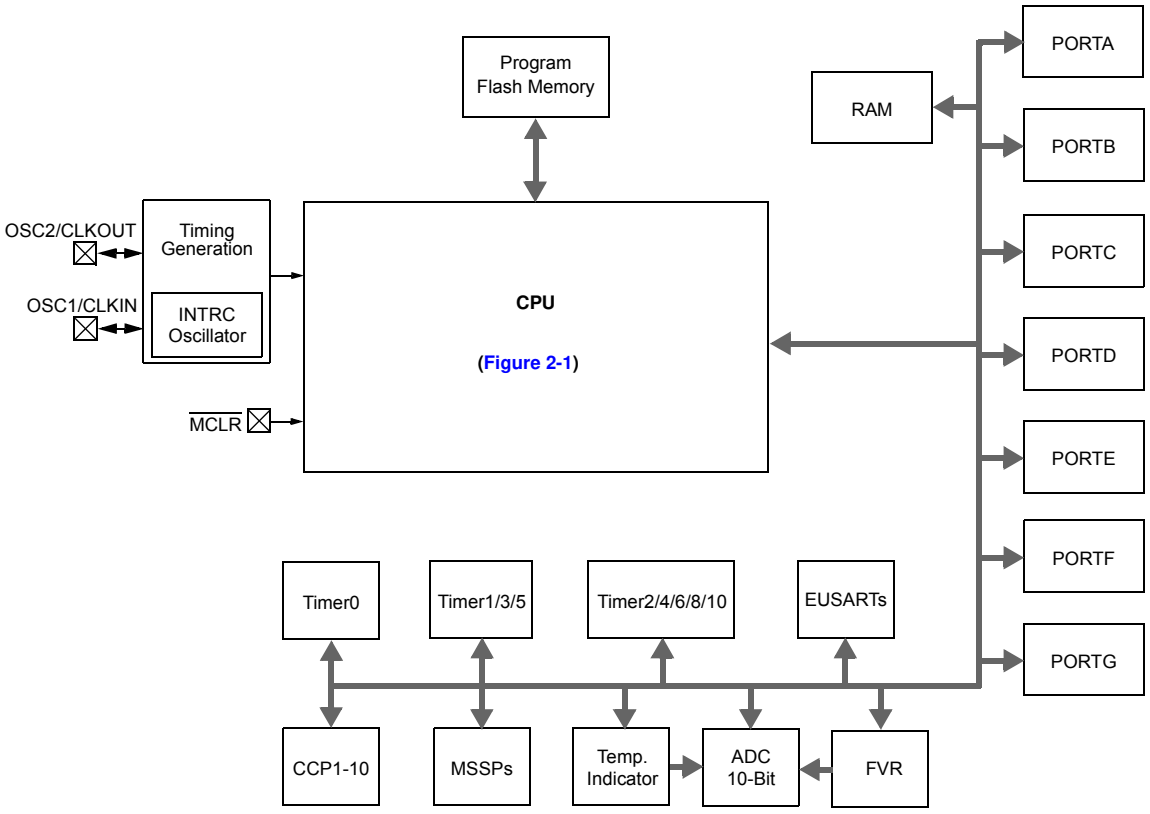
The PIC16(L)F1526/7 are described within this data sheet. They are available in 64-pin packages. Figure 1-1 shows a block diagram of the PIC16(L)F1526/7 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16F1526 PIC16LF1526	PIC16F1527 PIC16LF1527
ADC		•	•
EUSART		•	•
Fixed Voltage Reference (FVR)		•	•
Temperature Indicator		•	•
Capture/Compare/PWM Modules			
	CCP1	•	•
	CCP2	•	•
	CCP3	•	•
	CCP4	•	•
	CCP5	•	•
	CCP6	•	•
	CCP7	•	•
	CCP8	•	•
	CCP9	•	•
	CCP10	•	•
EUSARTs			
	EUSART1	•	•
	EUSART2	•	•
Master Synchronous Serial Ports			
	MSSP1	•	•
	MSSP2	•	•
Timers			
	Timer0	•	•
	Timer1/3/5	•	•
	Timer2/4/6/8/10	•	•

FIGURE 1-1: PIC16(L)F1526/7 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.
2: See Table 1-1 for peripherals available on specific devices.

TABLE 1-2: PIC16(L)F1526/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
RA1/AN1	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
RA2/AN2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
RA3/AN3/VREF+	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC Positive Voltage Reference input.
RA4/T0CKI	RA4	TTL	CMOS	General purpose I/O.
	T0CKI	ST	—	Timer0 clock input.
RA5/AN4/T3G	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	T3G	ST	—	Timer3 gate input.
RA6/OSC2/CLKOUT	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA7/OSC1/CLKIN	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External clock input (EC mode).
RB0/AN17/INT	RB0	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN17	AN	—	ADC Channel 17 input.
	INT	ST	—	External interrupt.
RB1/AN18	RB1	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN18	AN	—	ADC Channel 18 input.
RB2/AN19	RB2	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN19	AN	—	ADC Channel 19 input.
RB3/AN20	RB3	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN20	AN	—	ADC Channel 20 input.
RB4/AN21/T3CKI(1)	RB4	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN21	AN	—	ADC Channel 21 input.
	T3CKI	ST	—	Timer3 clock input.
RB5/AN22/T1G/T3CKI	RB5	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN22	AN	—	ADC Channel 22 input.
	T1G	ST	—	Timer1 gate input.
	T3CKI	ST	—	Timer3 clock input.
RB6/ICSPCLK/ICDCLK	RB6	TTL	CMOS	General purpose I/O with IOC and WPU.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RB7/ICSPDAT/ICDDAT	RB7	TTL	CMOS	General purpose I/O with IOC and WPU.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 12-1) register.
2: RC3, RC4, RD5 and RD6 read the I^2C ST input when I^2C mode is enabled.

TABLE 1-2: PIC16(L)F1526/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC0/SOSCO/T1CKI	RC0	ST	CMOS	General purpose I/O.
	SOSCO	XTAL	XTAL	Timer1/3/5 oscillator connection.
	T1CKI	ST	—	Timer1/3/5 clock input.
RC1/SOSCI/CCP2	RC1	ST	CMOS	General purpose I/O.
	SOSCI	XTAL	XTAL	Timer1/3/5 oscillator connection.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/CCP1	RC2	ST	CMOS	General purpose I/O.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/SCK1/SCL1(2)	RC3	ST	CMOS	General purpose I/O.
	SCK1	ST	CMOS	SPI clock.
	SCL1	I^2C	OD	I^2C clock.
RC4/SDI1/SDA1(2)	RC4	ST	CMOS	General purpose I/O.
	SDI1	ST	—	SPI data input.
	SDA1	I^2C	OD	I^2C data input/output.
RC5/SDO1	RC5	ST	CMOS	General purpose I/O.
	SDO1	—	CMOS	SPI data output.
RC6/TX1/CK1	RC6	ST	CMOS	General purpose I/O.
	TX1	—	CMOS	USART1 asynchronous transmit.
	CK1	ST	CMOS	USART1 synchronous clock.
RC7/RX1/DT1	RC7	ST	CMOS	General purpose I/O.
	RX1	ST	—	USART1 asynchronous input.
	DT1	ST	CMOS	USART1 synchronous data.
RDO/AN23	RD0	ST	CMOS	General purpose I/O with WPU.
	AN23	AN	—	ADC Channel 23 input.
RD1/AN24/T5CKI	RD1	ST	CMOS	General purpose I/O with WPU.
	AN24	AN	—	ADC Channel 24 input.
	T5CKI	ST	—	Timer5 clock input.
RD2/AN25	RD2	ST	CMOS	General purpose I/O with WPU.
	AN25	AN	—	ADC Channel 25 input.
RD3/AN26	RD3	ST	CMOS	General purpose I/O with WPU.
	AN26	AN	—	ADC Channel 26 input.
RD4/SDO2	RD4	ST	CMOS	General purpose I/O with WPU.
	SDO2	—	CMOS	SPI data output.
RD5/SDI2/SDA2(2)	RD5	ST	CMOS	General purpose I/O with WPU.
	SDI2	ST	—	SPI data input.
	SDA2	I^2C	OD	I^2C data input/output.
RD6/SCK2/SCL2(2)	RD6	ST	CMOS	General purpose I/O with WPU.
	SCK2	ST	CMOS	SPI clock.
	SCL2	I^2C	OD	I^2C clock.
RD7/$\overline{SS2}$	RD7	ST	CMOS	General purpose I/O with WPU.
	$\overline{SS2}$	ST	—	Slave Select input.
RE0/AN27	RE0	ST	CMOS	General purpose I/O with WPU.
	AN27	AN	—	ADC Channel 27 input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 12-1) register.
2: RC3, RC4, RD5 and RD6 read the I^2C ST input when I^2C mode is enabled.

TABLE 1-2: PIC16(L)F1526/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RE1/AN28	RE1	ST	CMOS	General purpose I/O with WPU.
	AN28	AN	—	ADC Channel 28 input.
RE2/AN29/CCP10	RE2	ST	CMOS	General purpose I/O with WPU.
	AN29	AN	—	ADC Channel 29 input.
	CCP10	ST	CMOS	Capture/Compare/PWM10.
RE3/CCP9	RE3	ST	CMOS	General purpose I/O with WPU.
	CCP9	ST	CMOS	Capture/Compare/PWM9.
RE4/CCP8	RE4	ST	CMOS	General purpose I/O with WPU.
	CCP8	ST	CMOS	Capture/Compare/PWM8.
RE5/CCP7	RE5	ST	CMOS	General purpose I/O with WPU.
	CCP7	ST	CMOS	Capture/Compare/PWM7.
RE6/CCP6	RE6	ST	CMOS	General purpose I/O with WPU.
	CCP6	ST	CMOS	Capture/Compare/PWM6.
RE7/CCP2(1)	RE7	ST	CMOS	General purpose I/O with WPU.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RF0/AN16/VCAP	RF0	ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator.
RF1/AN6	RF1	ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
RF2/AN7	RF2	ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
RF3/AN8	RF3	ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
RF4/AN9	RF4	ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
RF5/AN10	RF5	ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
RF6/AN11	RF6	ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
RF7/AN5/$\overline{SS1}$	RF7	ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
	$\overline{SS1}$	ST	—	Slave Select input.
RG0/CCP3	RG0	ST	CMOS	General purpose I/O.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
RG1/AN15/TX2/CK2	RG1	ST	CMOS	General purpose I/O.
	AN15	AN	—	ADC Channel 15 input.
	TX2	—	CMOS	USART2 asynchronous transmit.
	CK2	ST	CMOS	USART2 synchronous clock.
RG2/AN14/RX2/DT2	RG2	ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	RX2	ST	—	USART2 asynchronous input.
	DT2	ST	CMOS	USART2 synchronous data.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 12-1) register.
2: RC3, RC4, RD5 and RD6 read the I^2C ST input when I^2C mode is enabled.

TABLE 1-2: PIC16(L)F1526/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RG3/AN13/CCP4	RG3	ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
RG4/AN12/T5G/CCP5	RG4	ST	—	General purpose input.
	AN12	AN	—	ADC Channel 12 input.
	T5G	ST	—	Timer5 gate input.
	CCP5	ST	CMOS	Capture/Compare/PWM5.
RG5/$\overline{MCLR}$/V_{PP}	RG5	ST	—	General purpose input with WPU.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	V_{PP}	HV	—	Programming voltage.
AV_{DD}	AV_{DD}	Power	—	Analog positive supply.
AV_{SS}	AV_{SS}	Power	—	Analog ground reference.
V_{DD}	V_{DD}	Power	—	Positive supply.
V_{SS}	V_{SS}	Power	—	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

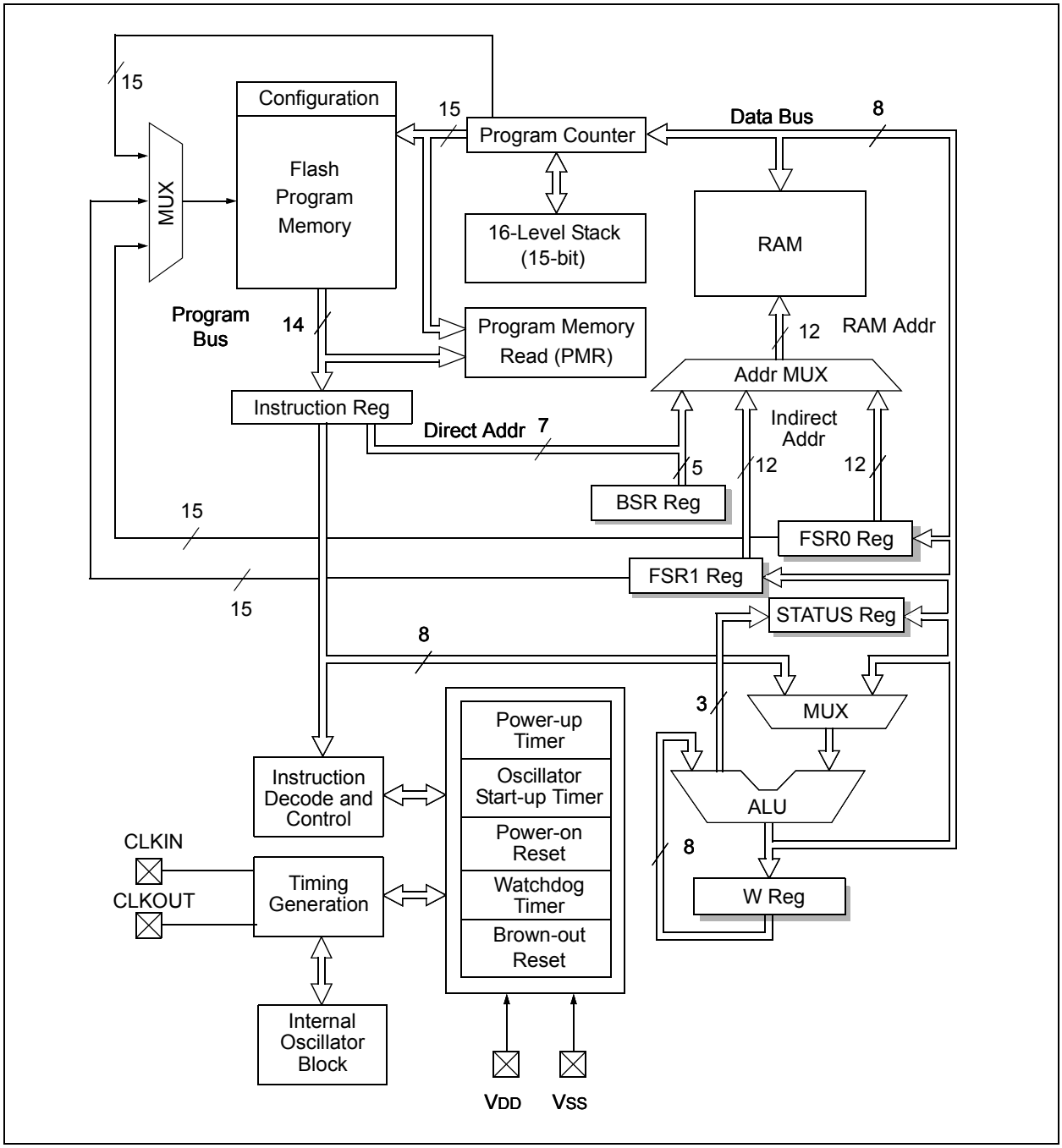
Note 1: Alternate pin function selected with the APFCON (Register 12-1) register.
2: RC3, RC4, RD5 and RD6 read the I^2C ST input when I^2C mode is enabled.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See **Section 3.7 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.8 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 24.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1526/7 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1 and Figure 3-2).

3.2 High Endurance Flash

This device has a 128-byte section of high-endurance Program Flash Memory (PFM) in lieu of data EEPROM. This area is especially well suited for nonvolatile data storage that is expected to be updated frequently over the life of the end product. See **Section 11.2 "Flash Program Memory Overview"** for more information on writing data to PFM. Refer to section **Section 3.2.1.2 "Indirect Read with FSR"** for more information about using the FSR registers to read byte data stored in PFM.

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range (1)
PIC16F1526 PIC16LF1526	8,192	1FFFh	1F80h-1FFFh
PIC16F1527 PIC16LF1527	16,384	3FFFh	3F80h-3FFFh

Note 1: High-endurance Flash applies to the low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1526

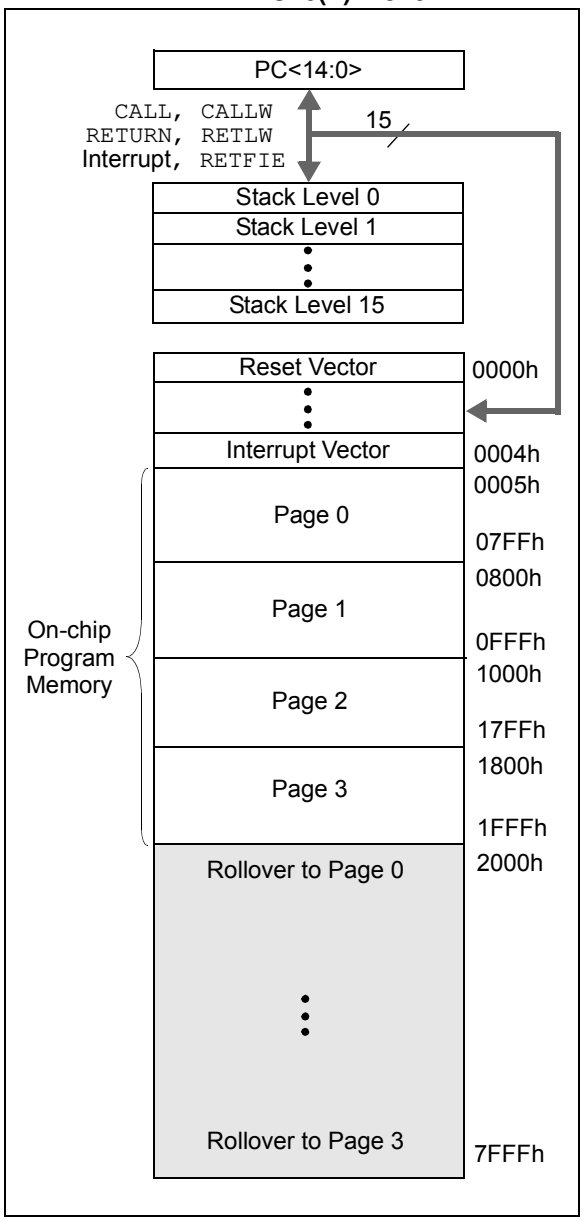
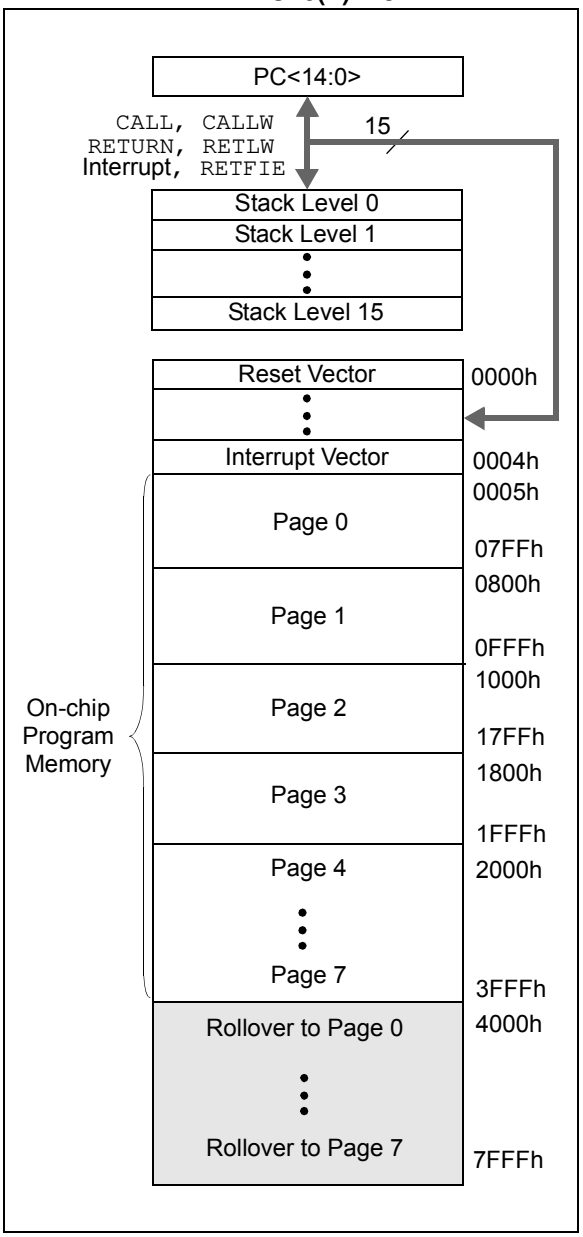


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1527



3.2.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.2.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    CALL constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.2.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The high directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    DW DATA0            ;First constant
    DW DATA1            ;Second constant
    DW DATA2
    DW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   DATA_INDEX
    ADDLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants ;Msb is set
                            automatically
    MOVWF   FSR1H
    BTFSC   STATUS,C        ;carry from
                             ADDLW?
    INCF    FSR1H,f         ;yes
    MOVIW 0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.3 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.8 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper seven bits of the address define the Bank address and the lower five bits select the registers/RAM in that bank.

3.3.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-4.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.3.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 24.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

3.4 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

3.5 Special Function Register

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.5.1 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

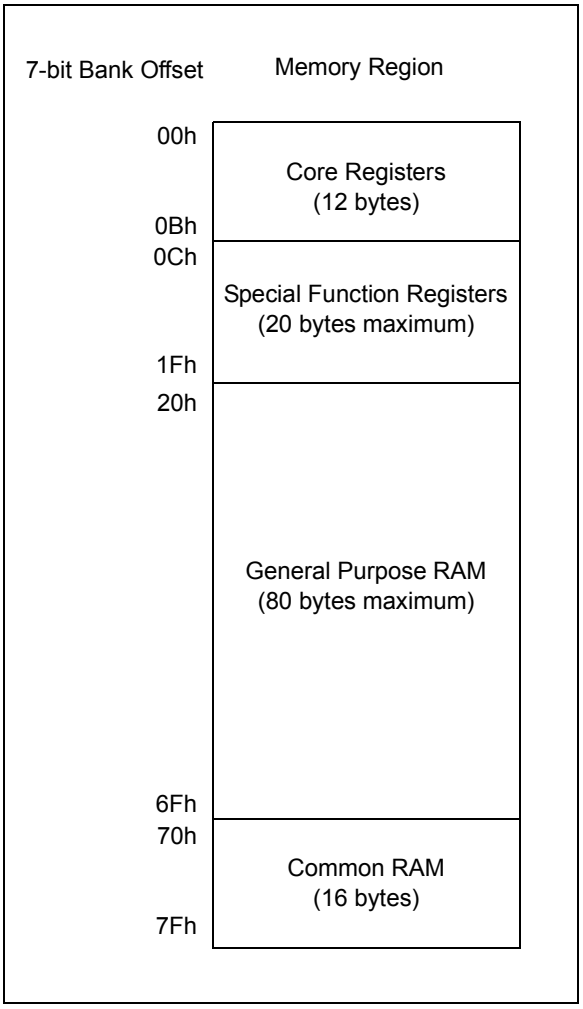
3.5.1.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.8.2 "Linear Data Memory"** for more information.

3.5.2 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.5.3 DEVICE MEMORY MAPS

The memory maps for PIC16(L)F1526/7 are shown in Table 3-3.

TABLE 3-3: PIC16(L)F1526/7 MEMORY MAP

BANK 0	BANK 1	BANK 2	BANK 3	BANK 4	BANK 5	BANK 6	BANK 7
000h Core Registers (Table 3-2) 00Bh	080h Core Registers (Table 3-2) 08Bh	100h Core Registers (Table 3-2) 10Bh	180h Core Registers (Table 3-2) 18Bh	200h Core Registers (Table 3-2) 20Bh	280h Core Registers (Table 3-2) 28Bh	300h Core Registers (Table 3-2) 30Bh	380h Core Registers (Table 3-2) 38Bh
00Ch PORTA	08Ch TRISA	10Ch LATA	18Ch ANSELA	20Ch —	28Ch PORTF	30Ch TRISF	38Ch LATF
00Dh PORTB	08Dh TRISB	10Dh LATB	18Dh ANSELB	20Dh WPUB	28Dh PORTG	30Dh TRISG	38Dh LATG
00Eh PORTC	08Eh TRISC	10Eh LATC	18Eh —	20Eh —	28Eh —	30Eh —	38Eh —
00Fh PORTD	08Fh TRISD	10Fh LATD	18Fh ANSELD	20Fh WPUD	28Fh —	30Fh —	38Fh —
010h PORTE	090h TRISE	110h LATE	190h ANSELE	210h WPUE	290h —	310h —	390h —
011h PIR1	091h PIE1	111h —	191h PMADRL	211h SSP1BUF	291h CCPR1L	311h CCPR3L	391h —
012h PIR2	092h PIE2	112h —	192h PMADRH	212h SSP1ADD	292h CCPR1H	312h CCPR3H	392h —
013h PIR3	093h PIE3	113h —	193h PMDATL	213h SSP1MSK	293h CCP1CON	313h CCP3CON	393h —
014h PIR4	094h PIE4	114h —	194h PMDATH	214h SSP1STAT	294h —	314h —	394h IOCBP
015h TMR0	095h OPTION_REG	115h —	195h PMCON1	215h SSP1CON1	295h —	315h —	395h IOCBN
016h TMR1L	096h PCON	116h BORCON	196h PMCON2	216h SSP1CON2	296h —	316h —	396h IOCBF
017h TMR1H	097h WDTCON	117h FVRCON	197h VREGCON(1)	217h SSP1CON3	297h —	317h —	397h —
018h T1CON	098h —	118h —	198h —	218h —	298h CCPR2L	318h CCPR4L	398h —
019h T1GCON	099h OSCCON	119h —	199h RC1REG	219h SSP2BUF	299h CCPR2H	319h CCPR4H	399h —
01Ah TMR2	09Ah OSCSTAT	11Ah —	19Ah TX1REG	21Ah SSP2ADD	29Ah CCP2CON	31Ah CCP4CON	39Ah —
01Bh PR2	09Bh ADRESL	11Bh —	19Bh SP1BRG	21Bh SSP2MSK	29Bh —	31Bh —	39Bh —
01Ch T2CON	09Ch ADRESH	11Ch —	19Ch SP1BRGH	21Ch SSP2STAT	29Ch —	31Ch CCPR5L	39Ch —
01Dh —	09Dh ADCON0	11Dh APFCON	19Dh RC1STA	21Dh SSP2CON1	29Dh CCPTMRS0	31Dh CCPR5H	39Dh —
01Eh —	09Eh ADCON1	11Eh —	19Eh TX1STA	21Eh SSP2CON2	29Eh CCPTMRS1	31Eh CCP5CON	39Eh —
01Fh —	09Fh —	11Fh —	19Fh BAUD1CON	21Fh SSP2CON3	29Fh CCPTMRS2	31Fh —	39Fh —
020h General Purpose Register 80 Bytes 06Fh	0A0h General Purpose Register 80 Bytes 0EFh	120h General Purpose Register 80 Bytes 16Fh	1A0h General Purpose Register 80 Bytes 1EFh	220h General Purpose Register 80 Bytes 26Fh	2A0h General Purpose Register 80 Bytes 2EFh	320h General Purpose Register 80 Bytes 36Fh	3A0h General Purpose Register 80 Bytes 3EFh
070h Common RAM 07Fh	0F0h Common RAM (Accesses 70h – 7Fh) 0FFh	170h Common RAM (Accesses 70h – 7Fh) 17Fh	1F0h Common RAM (Accesses 70h – 7Fh) 1FFh	270h Common RAM (Accesses 70h – 7Fh) 27Fh	2F0h Common RAM (Accesses 70h – 7Fh) 2FFh	370h Common RAM (Accesses 70h – 7Fh) 37Fh	3F0h Common RAM (Accesses 70h – 7Fh) 3FFh

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16F1526/7 only.

TABLE 3-3: PIC16(L)F1526/7 MEMORY MAP (CONTINUED)

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	ANSELF	48Ch	—	50Ch	Unimplemented Read as '0'	58Ch	—	60Ch	—	68Ch	Unimplemented Read as '0'	70Ch	Unimplemented Read as '0'	78Ch	Unimplemented Read as '0'
40Dh	ANSELG	48Dh	WPUG			58Dh	—	60Dh	—						
40Eh	—	48Eh	—			58Eh	—	60Eh	—						
40Fh	—	48Fh	—			58Fh	—	60Fh	—						
410h	—	490h	—			590h	—	610h	—						
411h	TMR3L	491h	RC2REG			591h	—	611h	CCPR6L						
412h	TMR3H	492h	TX2REG			592h	—	612h	CCPR6H						
413h	T3CON	493h	SP2BRG			593h	—	613h	CCP6CON						
414h	T3GCON	494h	SP2BRGH			594h	—	614h	CCPR7L						
415h	TMR4	495h	RC2STA			595h	TMR8	615h	CCPR7H						
416h	PR4	496h	TX2STA			596h	PR8	616h	CCP7CON						
417h	T4CON	497h	BAUD2CON			597h	T8CON	617h	CCPR8L						
418h	TMR5H	498h	—			598h	—	618h	CCPR8H						
419h	TMR5H	499h	—			599h	—	619h	CCP8CON						
41Ah	T5CON	49Ah	—			59Ah	—	61Ah	CCPR9L						
41Bh	T5GCON	49Bh	—			59Bh	—	61Bh	CCPR9H						
41Ch	TMR6	49Ch	—			59Ch	TMR10	61Ch	CCP9CON						
41Dh	PR6	49Dh	—			59Dh	PR10	61Dh	CCPR10L						
41Eh	T6CON	49Eh	—			59Eh	T10CON	61Eh	CCPR10H						
41Fh	—	49Fh	—	51Fh		59Fh	—	61Fh	CCP10CON	69Fh		71Fh		79Fh	
420h	General Purpose Register 80 Bytes	4A0h	General Purpose Register 32 Bytes	520h	General Purpose Register 80 Bytes(1)	5A0h	General Purpose Register 80 Bytes(1)	620h	General Purpose Register 80 Bytes(1)	6A0h	General Purpose Register 80 Bytes(1)	720h	General Purpose Register 80 Bytes(1)	7A0h	General Purpose Register 80 Bytes(1)
46Fh		4BFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
		4C0h	General Purpose Register 48 Bytes(1)												
470h	Common RAM (Accesses 70h – 7Fh)	4F0h	Common RAM (Accesses 70h – 7Fh)	570h	Common RAM (Accesses 70h – 7Fh)	5F0h	Common RAM (Accesses 70h – 7Fh)	670h	Common RAM (Accesses 70h – 7Fh)	6F0h	Common RAM (Accesses 70h – 7Fh)	770h	Common RAM (Accesses 70h – 7Fh)	7F0h	Common RAM (Accesses 70h – 7Fh)
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16(L)F1527 only.

TABLE 3-3: PIC16(L)F1526/7 MEMORY MAP (CONTINUED)

BANK 16	BANK 17	BANK 18	BANK 19	BANK 20	BANK 21	BANK 22	BANK 23
800h Core Registers (Table 3-2) 80Bh	880h Core Registers (Table 3-2) 88Bh	900h Core Registers (Table 3-2) 90Bh	980h Core Registers (Table 3-2) 98Bh	A00h Core Registers (Table 3-2) A0Bh	A80h Core Registers (Table 3-2) A8Bh	B00h Core Registers (Table 3-2) B0Bh	B80h Core Registers (Table 3-2) B8Bh
80Ch Unimplemented Read as '0' 81Fh	88Ch Unimplemented Read as '0' 89Fh	90Ch Unimplemented Read as '0' 91Fh	98Ch Unimplemented Read as '0' 9EFh	A0Ch Unimplemented Read as '0' A6Fh	A8Ch Unimplemented Read as '0' AEFh	B0Ch Unimplemented Read as '0' B6Fh	B8Ch Unimplemented Read as '0' BEFh
820h General Purpose Register 80 Bytes(1) 86Fh	8A0h General Purpose Register 80 Bytes(1) 8EFh	920h General Purpose Register 80 Bytes(1) 96Fh					
870h Common RAM (Accesses 70h – 7Fh) 87Fh	8F0h Common RAM (Accesses 70h – 7Fh) 8FFh	970h Common RAM (Accesses 70h – 7Fh) 97Fh	9F0h Common RAM (Accesses 70h – 7Fh) 9FFh	A70h Common RAM (Accesses 70h – 7Fh) A7Fh	AF0h Common RAM (Accesses 70h – 7Fh) AFFh	B70h Common RAM (Accesses 70h – 7Fh) B7Fh	BF0h Common RAM (Accesses 70h – 7Fh) BFFh

BANK 24	BANK 25	BANK 26	BANK 27	BANK 28	BANK 29	BANK 30
C00h Core Registers (Table 3-2) C0Bh	C80h Core Registers (Table 3-2) C8Bh	D00h Core Registers (Table 3-2) D0Bh	D80h Core Registers (Table 3-2) D8Bh	E00h Core Registers (Table 3-2) E0Bh	E80h Core Registers (Table 3-2) E8Bh	F00h Core Registers (Table 3-2) F0Bh
C0Ch Unimplemented Read as '0' C6Fh	C8Ch Unimplemented Read as '0' CEFh	D0Ch Unimplemented Read as '0' D6Fh	D8Ch Unimplemented Read as '0' DEFh	E0Ch Unimplemented Read as '0' E6Fh	E8Ch Unimplemented Read as '0' EEFh	F0Ch Unimplemented Read as '0' F6Fh
C70h Common RAM (Accesses 70h – 7Fh) C7Fh	CF0h Common RAM (Accesses 70h – 7Fh) CFFh	D70h Common RAM (Accesses 70h – 7Fh) D7Fh	DF0h Common RAM (Accesses 70h – 7Fh) DFFh	E70h Common RAM (Accesses 70h – 7Fh) E7Fh	EF0h Common RAM (Accesses 70h – 7Fh) EFFh	F70h Common RAM (Accesses 70h – 7Fh) F7Fh

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16(L)F1527 only.