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PIC16(L)F15354/55

Full-Featured 28-Pin Microcontrollers

Description

PIC16(L)F15354/55 microcontrollers feature Analog, Core Independent Peripherals and Communication Peripherals, combined with eXtreme Low-Power (XLP) technology for a wide range of general purpose and low-power applications.

The devices feature multiple PWMs, multiple communication, temperature sensor, and memory features like Memory Access Partition (MAP) to support customers in data protection and bootloader applications, and Device Information Area (DIA) which stores factory calibration values to help improve temperature sensor accuracy.

Core Features

- C Compiler Optimized RISC Architecture
- Only 48 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - 8-bit Timer2 with Hardware Limit Timer (HLT)
  - 16-bit Timer0/1
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software
- Programmable Code Protection

Memory

- Up to 14 KB Flash Program Memory
- Up to 1 KB Data SRAM
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Write protect
  - Customizable Partition
- Device Information Area (DIA)
- Device Configuration Information (DCI)

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF15354/55)
  - 2.3V to 5.5V (PIC16F15354/55)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- DOZE mode: Ability to Run the CPU Core Slower than the System Clock
- IDLE mode: Ability to halt CPU Core while Internal Peripherals Continue Operating
- SLEEP mode: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to disable hardware module to minimize active power consumption of unused peripherals

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 μA @ 32 kHz, 1.8V, typical
  - 32 μA/MHz @ 1.8V, typical

Digital Peripherals

- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Two Capture/Compare/PWM (CCP) module:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Four 10-Bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0 Hz < F_{NCO} < 32 MHz
  - Resolution: $F_{NCO}/2^{20}$
- Communication:
  - Up to two EUSART, RS-232, RS-485, LIN compatible
  - Up to two SPI
  - Two I^2C, SMBus, PMBus™ compatible

Digital Peripherals (Cont.)

- I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals

- Analog-to-Digital Converter (ADC):
  - 10-bit with up to 43 external channels
  - Operates in Sleep
- Two Comparators:
  - FVR, DAC and external input pin available on inverting and noninverting input
  - Software selectable hysteresis
  - Outputs available internally to other modules, or externally through PPS
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detect module
  - AC high voltage zero-crossing detection for simplifying TRIAC control
  - Synchronized switching control and timing

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Software selectable frequency range up to 32 MHz, ±1% typical
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 32 MHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if primary clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator resources

TABLE 1: PIC16(L)F153XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (KW)	Program Flash Memory (KB)	Storage Area Flash (B)	Data SRAM (bytes)	I/OPins	10-bit ADC	5-bit DAC	Comparator	8-bit/ (with HLT) Timer	16-bit Timer	Window Watchdog Timer	CCP/10-bit PWM	CWG	NCO	CLC	Zero-Cross Detect	Temperature Sensor	Memory Access Partition	Device Information Area	EUSART/ I2C-SPI	Peripheral Pin Select	Peripheral Module Disable	Debug (1)
PIC16(L)F15313	(C)	2	3.5	224	256	6	5	1	1	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16(L)F15323	(C)	2	3.5	224	256	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16(L)F15324	(D)	4	7	224	512	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15325	(B)	8	14	224	1024	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15344	(D)	4	7	224	512	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15345	(B)	8	14	224	1024	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15354	(A)	4	7	224	512	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15355	(A)	8	14	224	1024	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15356	(E)	16	28	224	2048	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15375	(E)	8	14	224	1024	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15376	(E)	16	28	224	2048	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15385	(E)	8	14	224	1024	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15386	(E)	16	28	224	2048	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I

Note 1: I - Debugging integrated on chip.

Data Sheet Index:

- **A: DS40001853B** PIC16(L)F15354/5 Data Sheet, 28-Pin
- **B:** Future Release PIC16(L)F15325/45 Data Sheet, 14/20-Pin
- **C:** Future Release PIC16(L)F15313/23 Data Sheet, 8/14-Pin
- **D:** Future Release PIC16(L)F15324/44 Data Sheet, 14/20-Pin
- **E:** Future Release PIC16(L)F15356/75/76/85/86 Data Sheet, 28/40/48-Pin

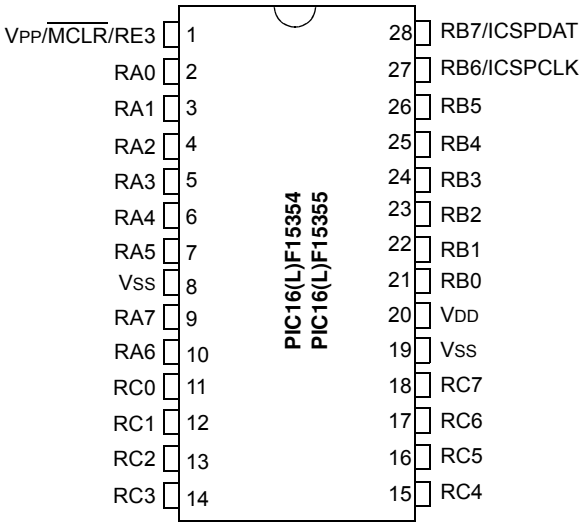
Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

TABLE 2: PACKAGES

Device	(S)PDIP	SOIC	SSOP	UQFN (4x4)	UQFN (6x6)
PIC16(L)F15354	•	•	•	•	•
PIC16(L)F15355	•	•	•	•	•

PIN DIAGRAMS

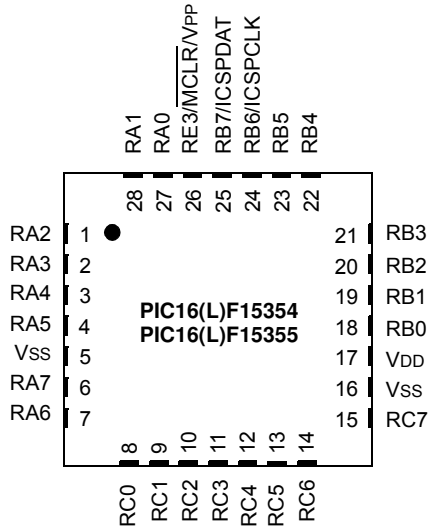
28-PIN PDIP, SOIC, SSOP



Note 1: See Table 2 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level.

28-PIN UQFN (4x4), UQFN (6x6)



Note 1: See Table 3 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

3: The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

PIN ALLOCATION TABLES

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F15354, PIC16(L)F15355)

I/O(2)	28-Pin PDIP/SOIC/SSOP	28-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	CLCIN0(1)	—	IOCA0	Y	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	CLCIN1(1)	—	IOCA1	Y	—
RA2	4	1	ANA2	—	C1IN0+ C2IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	—	IOCA2	Y	—
RA3	5	2	ANA3	VREF+	C1IN1+	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA3	Y	—
RA4	6	3	ANA4	—	—	—	—	T0CKI	—	—	—	—	—	—	—	—	IOCA4	Y	—
RA5	7	4	ANA5	—	—	—	—	—	—	—	—	$\overline{SS1}$(1)	—	—	—	—	IOCA5	Y	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	Y	CLKOUT OSC2
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	Y	CLKIN OSC1
RB0	21	18	ANB0	—	C2IN1+	—	—	—	—	—	CWG1IN(1)	$\overline{SS2}$(1)	ZCD1	—	—	—	INT(1) IOCB0	Y	—
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SCK2, SCL2(1,4)	—	—	—	—	IOCB1	Y	—
RB2	23	20	ANB2	—	—	—	—	—	—	—	—	SDA2, SDI2(1,4)	—	—	—	—	IOCB2	Y	—
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	IOCB3	Y	—
RB4	25	22	ANB4 ADACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCB4	Y	—
RB5	26	23	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	—	IOCB5	Y	—
RB6	27	24	ANB6	—	—	—	—	—	—	—	—	—	—	TX2 CK2(1)	CLCIN2(1)	—	IOCB6	Y	ICSPCLK
RB7	28	25	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	—	RX2 DT2(1)	CLCIN3(1)	—	IOCB7	Y	ICSPDAT

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F15354, PIC16(L)F15355) (CONTINUED)

I/O(2)	28-Pin PDIP/SOIC/SSOP	28-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC0	11	8	ANC0	—	—	—	—	SOSCO T1CKI	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	12	9	ANC1	—	—	—	—	SOSCI	CCP2(1)	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	13	10	ANC2	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	14	11	ANC3	—	—	—	—	T2IN(1)	—	—	—	SCL1, SCK1(1,4)	—	—	—	—	IOCC3	Y	—
RC4	15	12	ANC4	—	—	—	—	—	—	—	—	SDA1, SDI1(1,4)	—	—	—	—	IOCC4	Y	—
RC5	16	13	ANC5	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC5	Y	—
RC6	17	14	ANC6	—	—	—	—	—	—	—	—	—	—	TX1 CK1(1)	—	—	IOCC6	Y	—
RC7	18	15	ANC7	—	—	—	—	—	—	—	—	—	—	RX1 DT1(1)	—	—	IOCC7	Y	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	Y	$\overline{MCLR}$ V_{PP}
V_{DD}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{SS}	19	5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
VSEL0	19	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3	CWG1A CWG2A	SDO1/2	—	DT	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	CCP2	PWM4	CWG1B CWG2B	SCK1/2	—	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	PWM5	CWG1C CWG2C	SCL1/2(3,4)	—	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	PWM6	CWG1D CWG2D	SDA1/2(3,4)	—	—	CLC4OUT	—	—	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

Table of Contents

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1.0 DEVICE OVERVIEW

The PIC16(L)F15354/55 are described within this data sheet. The PIC16(L)F15354/55 devices are available in 28-pin SPDIP, SSOP, SOIC, and UQFN packages. Figure 1-1 shows a block diagram of the PIC16(L)F15354/55 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F15354/55
Analog-to-Digital Converter		•
Digital-to-Analog Converter (DAC1)		•
Fixed Voltage Reference (FVR)		•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1 and EUSART2)		•
Numerically Controlled Oscillator (NCO1)		•
Temperature Indicator Module (TIM)		•
Zero-Cross Detect (ZCD1)		•
Capture/Compare/PWM Modules (CCP)		
	CCP1	•
	CCP2	•
Comparator Module (Cx)		
	C1	•
	C2	•
Configurable Logic Cell (CLC)		
	CLC1	•
	CLC2	•
	CLC3	•
	CLC4	•
Complementary Waveform Generator (CWG)		
	CWG1	•
Master Synchronous Serial Ports (MSSP)		
	MSSP1	•
	MSSP2	•
Pulse-Width Modulator (PWM)		
	PWM3	•
	PWM4	•
	PWM5	•
	PWM6	•
Timers		
	Timer0	•
	Timer1	•
	Timer2	•

1.1 Register and Bit Naming Conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

Example 2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt, and Mirror Bits

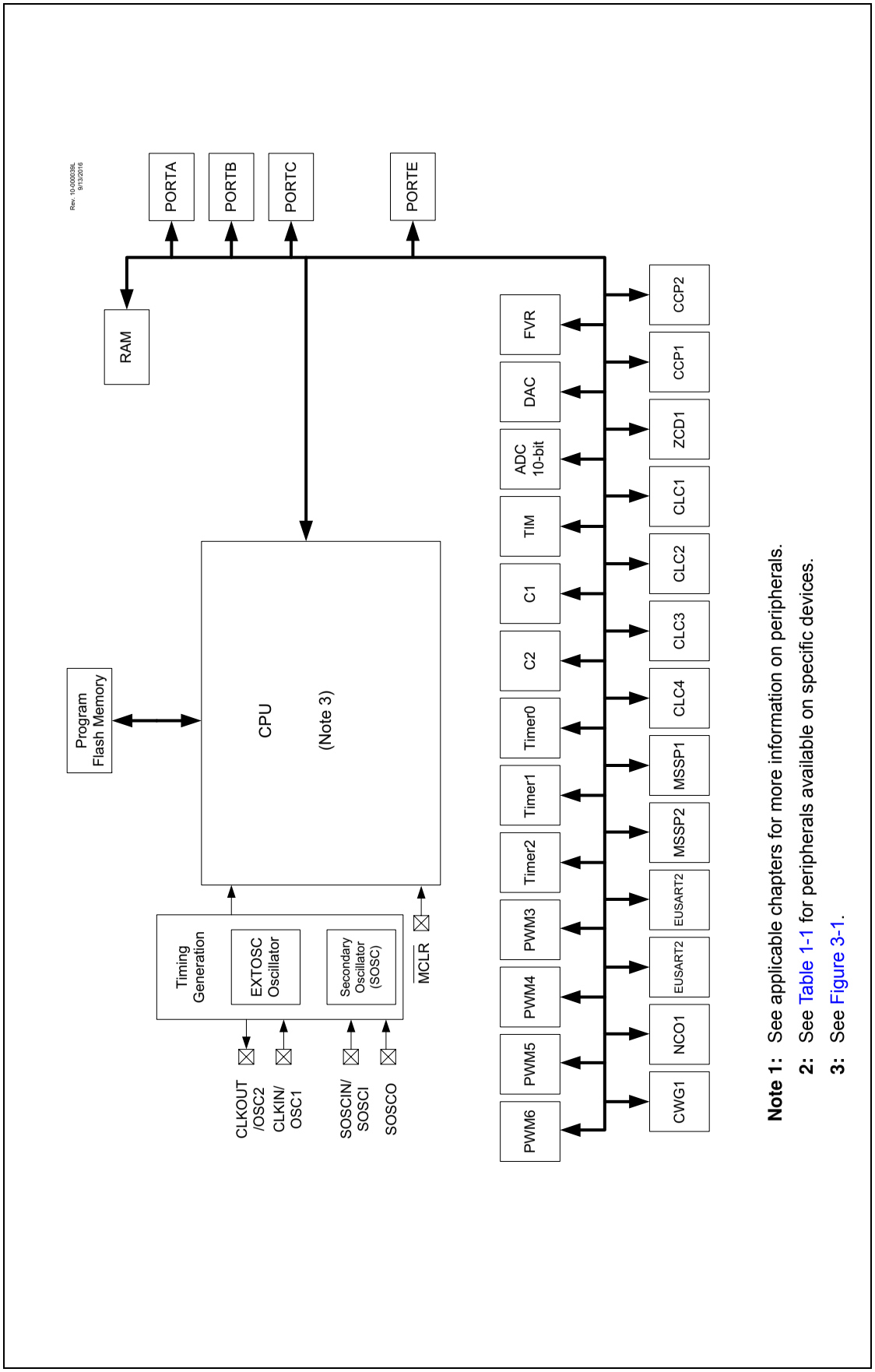
Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

- EUSART
- MSSP

FIGURE 1-1: PIC16(L)F15354/55 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

2: See Table 1-1 for peripherals available on specific devices.

3: See Figure 3-1.

TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0-/C2IN0-/CLCIN0(1)/IOCA0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0-	AN	—	Comparator 1 negative input.
	C2IN0-	AN	—	Comparator 2 negative input.
	CLCIN0(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
RA1/ANA1/C1IN1-/C2IN1-/CLCIN1(1)/IOCA1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	CLCIN1(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
RA2/ANA2/C1IN0+/C2IN0+/VREF-/DAC1OUT1/IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	C1IN0+	AN	—	Comparator 2 positive input.
	C2IN0+	AN	—	Comparator 2 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
RA3/ANA3/C1IN1+/VREF+/IOCA3/DAC1REF+	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	ANA3	AN	—	ADC Channel A3 input.
	C1IN1+	AN	—	Comparator 1 positive input.
	VREF+	AN	—	External ADC and/or DAC positive reference input.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
	DAC1REF+	TTL/ST	AN	DAC positive reference.
RA4/ANA4/T0CKI(1)/IOCA4	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T0CKI(1)	TTL/ST	—	Timer0 clock input.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
RA5/ANA5/SS1(1)/IOCA5	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	SS1(1)	TTL/ST	—	MSSP1 SPI slave select input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA6/ANA6/OSC2/CLKOUT/IOCA6	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN	—	ADC Channel A6 input.
	OSC2	—	XTAL	External Crystal/Resonator (LP, XT, HS modes) driver output.
	CLKOUT	—	CMOS/OD	FOSC/4 digital output (in non-crystal/resonator modes).
	IOCA6	TTL/ST	—	Interrupt-on-change input.
RA7/ANA7/OSC1/CLKIN/IOCA7	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN	—	ADC Channel A7 input.
	OSC1	XTAL	—	External Crystal/Resonator (LP, XT, HS modes) driver input.
	CLKIN	TTL/ST	—	External digital clock input.
	IOCA7	TTL/ST	—	Interrupt-on-change input.
RB0/ANB0/C2IN1+/ZCD1/SS2(1)/CWG1IN(1)/INT(1)/IOCB0	RB0	TTL/ST	CMOS/OD	General purpose I/O.
	ANB0	AN	—	ADC Channel B0 input.
	C2IN1+	AN	—	Comparator 2 positive input.
	ZCD1	AN	AN	Zero-cross detect input pin (with constant current sink/source).
	SS2(1)	TTL/ST	—	MSSP2 SPI slave select input.
	CWG1IN(1)	TTL/ST	—	Complementary Waveform Generator 1 input.
	INT(1)	TTL/ST	—	External interrupt request input.
	IOCB0	TTL/ST	—	Interrupt-on-change input.
RB1/ANB1/C1IN3-/C2IN3-/SCL2(3,4)/SCK2(1)/IOCB1	RB1	TTL/ST	CMOS/OD	General purpose I/O.
	ANB1	AN	—	ADC Channel B1 input.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	SCL2(3,4)	I^2C	OD	MSSP2 I^2C clock input/output.
	SCK2(1)	TTL/ST	CMOS/OD	MSSP2 SPI serial clock (default input location, SCK2 is a PPS remappable input and output).
	IOCB1	TTL/ST	—	Interrupt-on-change input.
RB2/ANB2/SDA2(3,4)/SDI2(1)/IOCB2	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	ANB2	AN	—	ADC Channel B2 input.
	SDA2(3,4)	I^2C	OD	MSSP2 I^2C serial data input/output.
	SDI2(1)	TTL/ST	—	MSSP2 SPI serial data input.
	IOCB2	TTL/ST	—	Interrupt-on-change input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
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TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3/ANB3/C1IN2-/C2IN2-/IOCB3	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	ANB3	AN	—	ADC Channel B3 input.
	C1IN2-	AN	—	Comparator 1 negative input.
	C2IN2-	AN	—	Comparator 2 negative input.
	IOCB3	TTL/ST	—	Interrupt-on-change input.
RB4/ANB4/ADACT(1)/IOCB4	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	ANB4	AN	—	ADC Channel B4 input.
	ADACT(1)	TTL/ST	—	ADC Auto-Conversion Trigger input.
	IOCB4	TTL/ST	—	Interrupt-on-change input.
RB5/ANB5/T1G(1)/IOCB5	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	ANB5	AN	—	ADC Channel B5 input.
	T1G(1)	ST	—	Timer1 Gate input.
	IOCB5	TTL/ST	—	Interrupt-on-change input.
RB6/ANB6/CLCIN2(1)/IOCB6/TX2/CK2(3)/ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	ANB6	AN	—	ADC Channel B6 input.
	CLCIN2(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCB6	TTL/ST	—	Interrupt-on-change input.
	TX2	—	CMOS	EUSART2 asynchronous.
	CK2(3)	TTL/ST	CMOS/OD	EUSART2 synchronous mode clock input/output.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.
RB7/ANB7/RX2/DT2/CLCIN3(1)/IOCB7/DAC1OUT2/ICSPDAT	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	ANB7	AN	—	ADC Channel B7 input.
	CLCIN3(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCB7	TTL/ST	—	Interrupt-on-change input.
	RX2(1)	TTL/ST	—	EUSART2 Asynchronous mode receiver data input.
	DT2(3)	TTL/ST	CMOS/OD	EUSART2 Synchronous mode data input/output.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ and debugging data input/output.
RC0/ANC0/T1CKI(1)/IOCC0/SOSCO	RC0	TTL/ST	CMOS/OD	General purpose I/O.
	ANC0	AN	—	ADC Channel C0 input.
	T1CKI(1)	TTL/ST	—	Timer1 external digital clock input.
	IOCC0	TTL/ST	—	Interrupt-on-change input.
	SOSCO	—	AN	32.768 kHz secondary oscillator crystal driver output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-2 for details on which PORT pins may be used for this signal.

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4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC1/ANC1/CCP2(1)/IOCC1/SOSCI	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	ANC1	AN	—	ADC Channel C1 input.
	CCP2(1)	TTL/ST	CMOS/OD	CCP2 Capture Input.
	IOCC1	TTL/ST	—	Interrupt-on-change input.
	SOSCI	AN	—	32.768 kHz secondary oscillator crystal driver input.
RC2/ANC2/CCP1(1)/IOCC2	RC2	TTL/ST	CMOS/OD	General purpose I/O.
	ANC2	AN	—	ADC Channel C2 input.
	CCP1(1)	TTL/ST	CMOS/OD	CCP1 Capture Input.
	IOCC2	TTL/ST	—	Interrupt-on-change input.
RC3/ANC3/SCL1(3,4)/SCK1(1)/T2IN(1)/IOCC3	RC3	TTL/ST	CMOS/OD	General purpose I/O.
	ANC3	AN	—	ADC Channel C3 input.
	SCL1(3,4)	I^2C	OD	MSSP1 I^2C input/output.
	SCK1(1)	TTL/ST	CMOS/OD	MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output).
	T2IN(1)	TTL/ST	—	Timer2 external input.
	IOCC3	TTL/ST	—	Interrupt-on-change input.
RC4/ANC4/SDA1(3,4)/SDI1(1)/IOCC4	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
	SDA1(3,4)	I^2C	OD	MSSP1 I^2C serial data input/output.
	SDI1(1)	TTL/ST	—	MSSP1 SPI serial data input.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
RC5/ANC5/IOCC5	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	IOCC5	TTL/ST	—	Interrupt-on-change input.
RC6/ANC6/TX1/CK1(1)/IOCC6	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	ANC6	AN	—	ADC Channel C6 input.
	TX1	—	CMOS	EUSART1 asynchronous transmit.
	CK1(1)	TTL/ST	CMOS/OD	EUSART 1 synchronous mode clock input/output.
	IOCC6	TTL/ST	—	Interrupt-on-change input.
RC7/ANC7/RX1/DT1(3)/IOCC7	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	ANC7	AN	—	ADC Channel C7 input.
	RX1	TTL/ST	—	EUSART1 Asynchronous mode receiver data input.
	DT1(3)	TTL/ST	CMOS/OD	EUSART1 Synchronous mode data input/output.
	IOCC7	TTL/ST	—	Interrupt-on-change input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

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4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RE3/ANE3/IOCE3/$\overline{MCLR}$/V_{PP}	RE3	TTL/ST	—	General purpose input only (when $\overline{MCLR}$ is disabled by the Configuration bit).
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	$\overline{MCLR}$	ST	—	Master clear input with internal weak pull up resistor.
	V_{PP}	HV	—	ICSP™ High-Voltage Programming mode entry input.
V_{DD}	V_{DD}	Power	—	Positive supply voltage input.
V_{SS}		Power	—	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

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2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

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4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1OUT	—	CMOS/OD	Comparator 1 output.
	C2OUT	—	CMOS/OD	Comparator 2 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	SDO2	—	CMOS/OD	MSSP2 SPI serial data output.
	SCK2	—	CMOS/OD	MSSP2 SPI serial clock output.
	TX1	—	CMOS/OD	EUSART1 Asynchronous mode transmitter data output.
	CK1(3)	—	CMOS/OD	EUSART1 Synchronous mode clock output.
	TX2	—	CMOS/OD	EUSART2 Asynchronous mode transmitter data output.
	CK2(3)	—	CMOS/OD	EUSART2 Synchronous mode clock output.
	DT(3)	—	CMOS/OD	EUSART Synchronous mode data output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	CCP2 output (compare/PWM functions).
	CCP2	—	CMOS/OD	CCP2 output (compare/PWM functions).
	PWM3OUT	—	CMOS/OD	PWM3 output.
	PWM4OUT	—	CMOS/OD	PWM4 output.
	PWM5OUT	—	CMOS/OD	PWM5 output.
	PWM6OUT	—	CMOS/OD	PWM6 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
	CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.
	NCO1	—	CMOS/OD	Numerically Controller Oscillator output.
	CLKR	—	CMOS/OD	Clock Reference module output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
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2.0 GUIDELINES FOR GETTING STARTED WITH PIC16(L)F15354/55 MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC16(L)F15354/55 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Power Supply Pins"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)

These pins must also be connected if they are being used in the end application:

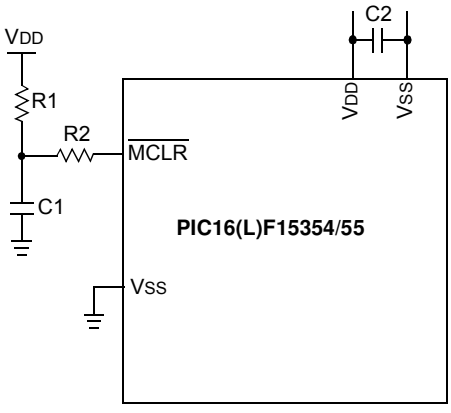
- PGC/PGD pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.4 "ICSP™ Pins"**)
- OSCI and OSCO pins when an external oscillator source is used (see **Section 2.5 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 and C2: 0.1 µF, 20V ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins (VDD and VSS) is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 µF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 µF in parallel with 0.001 µF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

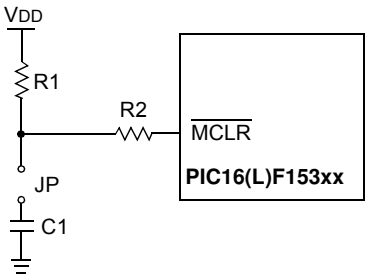
2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS



Note 1: R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

2: R2 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C1, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

2.4 ICSP™ Pins

The PGC and PGD pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGC and PGD pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., PGCx/PGDx pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 39.0 "Development Support"**.

2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-3. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

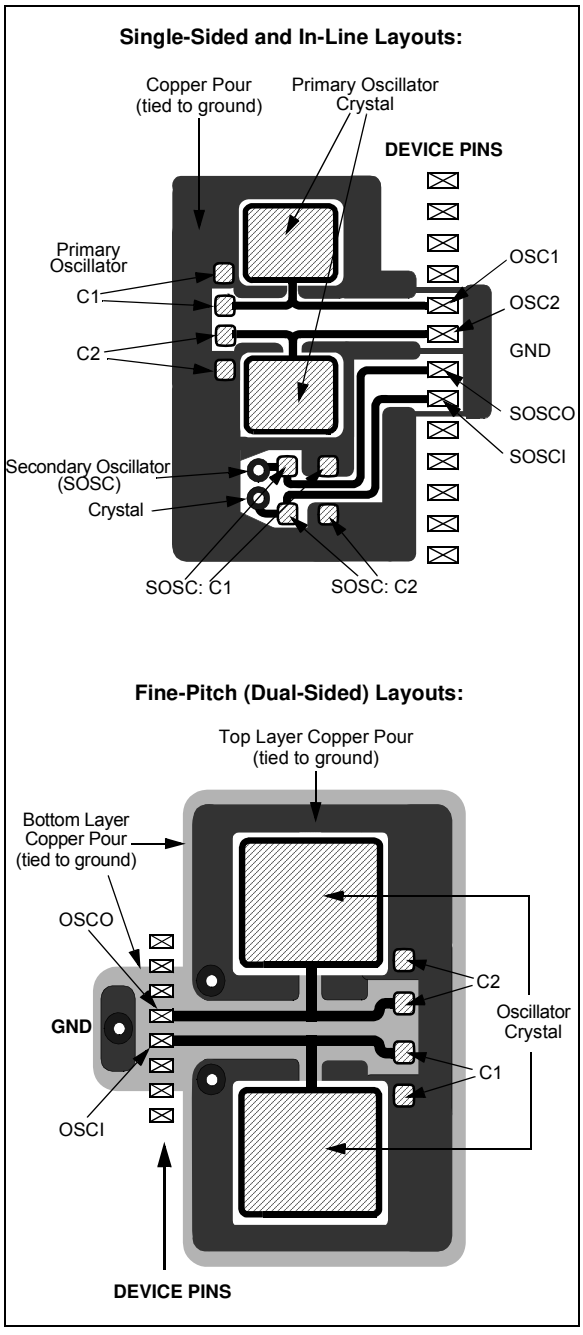
For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- *AN849, "Basic PICmicro® Oscillator Design"*
- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output to logic low.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

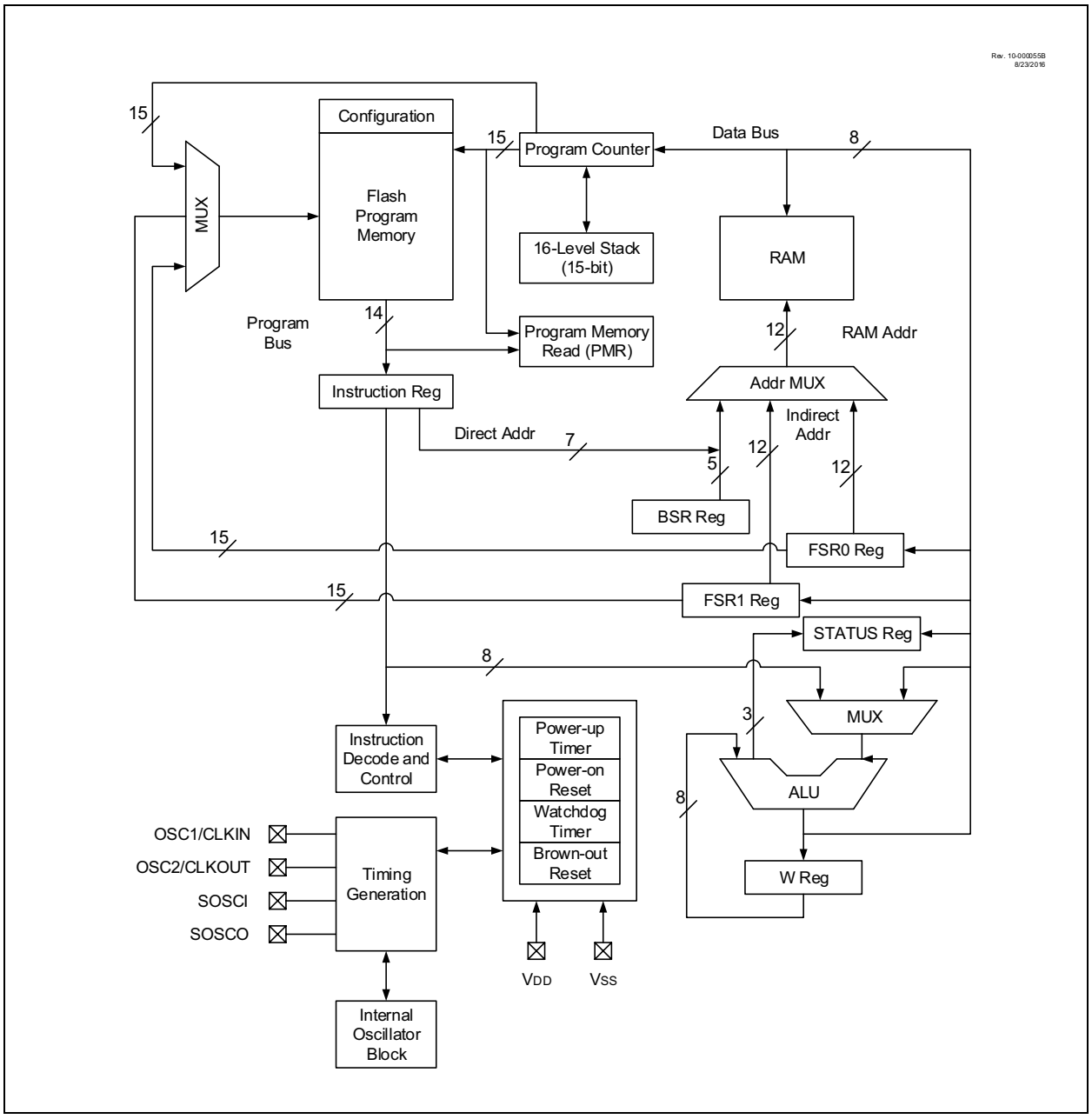


3.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 48 instructions. Interrupt capability includes automatic context saving.

The hardware stack is 16-levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

FIGURE 3-1: CORE DATA PATH DIAGRAM



3.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 10.5 "Automatic Context Saving"** for more information.

3.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 4.5 "Stack"** for more details.

3.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. See **Section 4.6 "Indirect Addressing"** for more details.

3.4 Instruction Set

There are 48 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 36.0 "Instruction Set Summary"** for more details.

4.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Program Flash Memory
  - Device Information Area (DIA)
  - Device Configuration Information (DCI)
  - Revision ID
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing
- NVMREG access

4.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing 32K x 14 program memory space. Table 4-1 shows the memory sizes implemented. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 4-1).

TABLE 4-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Size (Words)	Last Program Memory Address
PIC16(L)F15354	4096	0FFFh
PIC16(L)F15355	8192	1FFFh

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F15354

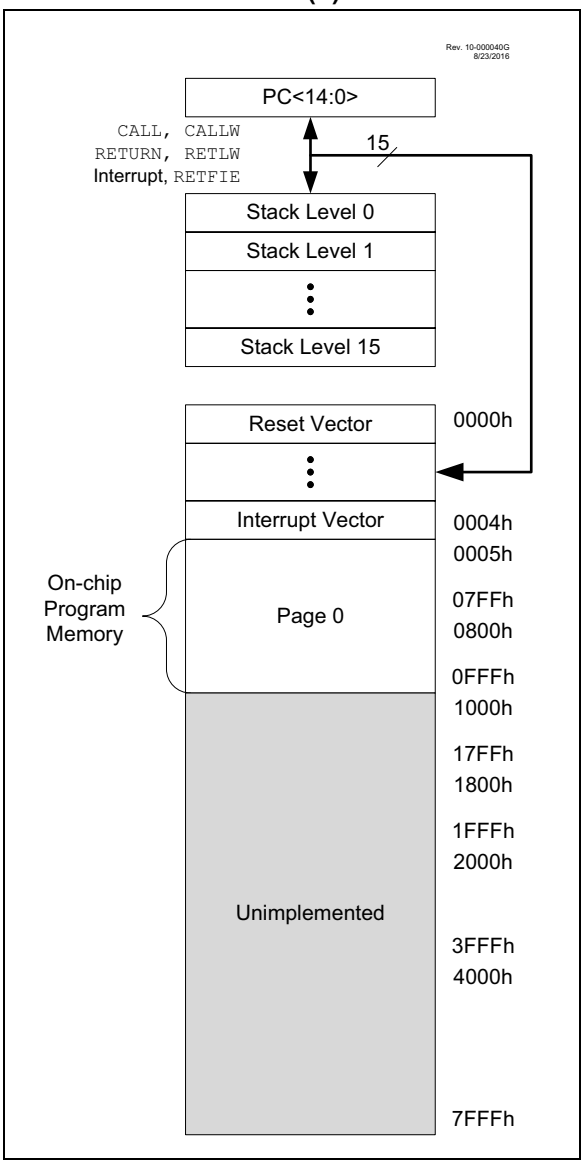


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F15355