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PIC16LF1554/1559

20-Pin Flash, 8-Bit Microcontrollers with XLP Technology

Description

The PIC16LF1554/1559 microcontrollers with Microchip enhanced mid-range core deliver unique on-chip features for the design of mTouch® solutions and general purpose applications in 14/20-pin count packages. Two 10-bit high-speed ADCs with automated hardware CVD modules connect to up to 17 analog channels to achieve a total sampling rate of 600k samples per second. Combined with two PWMs and multiple communication peripherals, this microcontroller family is an excellent solution to implement low-power and noise-robust capacitive sensing and other front-end sampling applications with minimal software overhead.

High-Performance RISC CPU

- Only 49 Instructions to Learn
- Operating Speed:
  - DC – 32 MHz clock input
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Special Microcontroller Features

- Precision 16 MHz Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 4x Phase-Locked Loop (PLL)
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- BOR with Selectable Trip Point
- Low-Power Brown-Out Reset (LPBOR)
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
  - 1.8V to 3.6V
- Programmable Code Protection
- Self-Programmable under Software Control

eXtreme Low Power (XLP) Features

- Sleep Current:
  - 30 nA @ 1.8V, typical
- Operating Current:
  - 75 μA @ 1 MHz, 1.8V, typical
- Low-Power Watchdog Timer Current:
  - 500 nA @ 1.8V, typical

Peripheral Features

- Up to 17 I/O Pins and One Input-only Pin:
  - High current sink/source for LED drivers
  - Individually programmable interrupt-on-change pins
  - Individually programmable weak pull-ups
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
- Timer2 modules: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two PWM modules
- Two Analog-to-Digital Converters (ADC):
  - 10-bit resolution
  - Up to 17 channels
  - Simultaneous sampling on two ADCs
  - Connect multiple channels together for sampling
  - External conversion trigger
  - Flexible analog channel selection
  - Conversion during Sleep
  - Fixed Voltage Reference as channel
  - External pin as ADC positive reference
  - Temp sensor channel input
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V and 2.048V output levels
- Hardware Capacitive Voltage Divider (CVD):
  - Double-sample conversions
  - Two sets of result registers
  - Inverted acquisition
  - 7-bit precharge timer
  - 7-bit acquisition timer
  - Two guard ring output drives
  - 30 pF adjustable sample and hold capacitor array

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- Master Synchronous Serial Port (MSSP) with SPI and I^2C with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start

PIC16LF1554/1559 Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	SRAM (bytes)	I/Os(1)	10-bit ADC (ch)(2)	Timers 8/16-Bit	EUSART	MSSP	PWM	Cap Touch Channels	Debug(3)
PIC16LF1554	**(A)**	4096	0	256	12	11	2/1	1	1	2	11	I
PIC16LF1559	**(A)**	8192	0	512	18	17	2/1	1	1	2	17	I

Note 1: RA3 is input only.

2: 11/17 analog channels are connected to two ADC modules.

3: Debugging Methods: (I) – Integrated on Chip; (H) – available using Debug Header

Data Sheet Index: (Unshaded devices are described in this document)

A. DS40001761 PIC16LF1554/1559 Data Sheet, 14/20-Pin, 8-Bit Flash Microcontrollers.

Note:	For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

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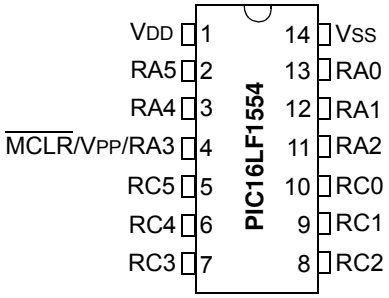
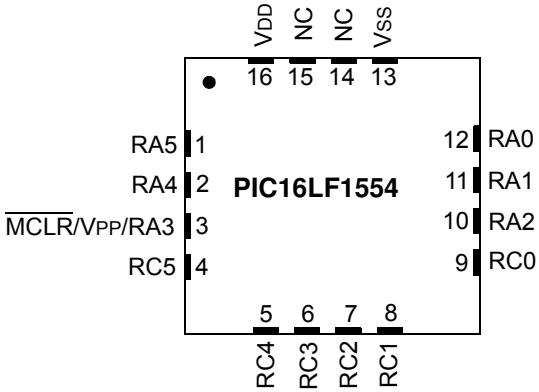
Pin Diagrams

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP



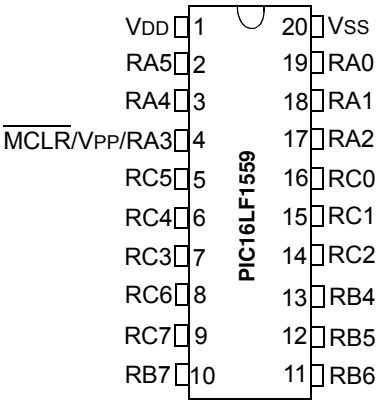
Note: See Table 1 for location of all peripheral functions.

FIGURE 2: 16-PIN QFN



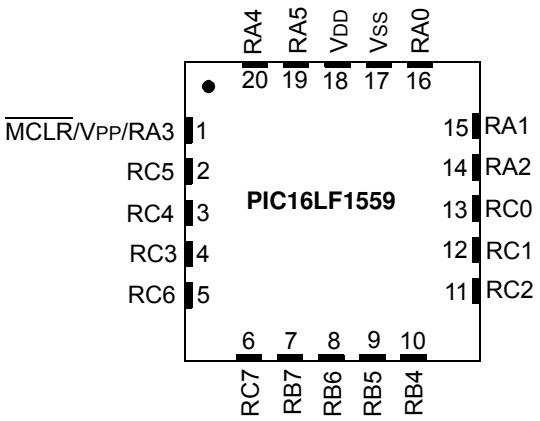
Note: See Table 1 for location of all peripheral functions.

FIGURE 3: 20-PIN PDIP, SSOP



Note: See Table 2 for location of all peripheral functions.

FIGURE 4: 20-PIN QFN,UQFN (4x4)



Note: See Table 2 for location of all peripheral functions.

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Pin Allocation Tables

TABLE 1: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16LF1554)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	ADC	Reference	Timers	PWM	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	13	12	AN0	—	—	—	—	—	IOC	Y	ICSPDAT/ ICDDAT
RA1	12	11	AN1	VREF+	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RA2	11	10	AN2	—	T0CKI	—	—	—	INT/ IOC	Y	—
RA3	4	3	—	—	—	—	—	$\overline{SS}$(1) SDA(1) SDI(1)	IOC	Y	$\overline{MCLR}$ VPP
RA4	3	2	AN10 ADTRIG	—	T1G	—	RX(1) DT(1)	SDO(1)	IOC	Y	CLKOUT
RA5	2	1	AN20	—	T1CKI	—	—	—	IOC	Y	CLKIN
RC0	10	9	AN13	—	—	—	—	SCL SCK	—	Y	—
RC1	9	8	AN23	—	—	—	—	SDA(1) SDI(1)	—	Y	—
RC2	8	7	AN12 AD1GRDB AD2GRDB(1)	—	—	PWM1	—	SDO(1)	—	Y	—
RC3	7	6	AN22 AD1GRDB(1) AD2GRDB	—	—	PWM2	TX(1) CK(1)	$\overline{SS}$(1)	—	Y	—
RC4	6	5	AN11 AD1GRDA AD2GRDA(1)	—	—	—	TX(1) CK(1)	—	—	Y	—
RC5	5	4	AN21 AD1GRDA(1) AD2GRDA	—	—	—	RX(1) DT(1)	—	—	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	VSS

Note 1: Pin functions can be assigned to one of two pin locations via software.

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16LF1559)

I/O	20-Pin PDIP/SSOP	20-Pin QFN/UQFN	ADC	Reference	Timers	PWM	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	19	16	AN0	—	—	—	—	—	IOC	Y	ICSPDAT/ ICDDAT
RA1	18	15	AN1	VREF+	—	—	—	—	IOC	Y	ICSPCLK/ ICDCLK
RA2	17	14	AN2	—	T0CKI	—	—	—	INT/ IOC	Y	—
RA3	4	1	—	—	—	—	—	SDA(1) SDI(1) $\overline{SS}$(1)	IOC	Y	$\overline{MCLR}$ VPP
RA4	3	20	AN10 ADTRIG	—	T1G	—	—	—	IOC	Y	CLKOUT
RA5	2	19	AN20	—	T1CKI	—	—	—	IOC	Y	CLKIN
RB4	13	10	AN26	—	—	—	—	SDA(1) SDI(1)	IOC	Y	—
RB5	12	9	AN16	—	—	—	RX DT	—	IOC	Y	—
RB6	11	8	AN25	—	—	—	—	SCL SCK	IOC	Y	—
RB7	10	7	AN15	—	—	—	TX CK	—	IOC	Y	—
RC0	16	13	AN13	—	—	—	—	—	—	Y	—
RC1	15	12	AN23	—	—	—	—	—	—	Y	—
RC2	14	11	AN12 AD1GRDB AD2GRDB(1)	—	—	PWM1	—	—	—	Y	—
RC3	7	4	AN22 AD1GRDB(1) AD2GRDB	—	—	PWM2	—	—	—	Y	—
RC4	6	3	AN11 AD1GRDA AD2GRDA(1)	—	—	—	—	—	—	Y	—
RC5	5	2	AN21 AD1GRDA(1) AD2GRDA	—	—	—	—	—	—	Y	—
RC6	8	5	AN14	—	—	—	—	$\overline{SS}$(1)	—	Y	—
RC7	9	6	AN24	—	—	—	—	SDO	—	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	VSS

Note 1: Pin functions can be assigned to one of two pin locations via software.

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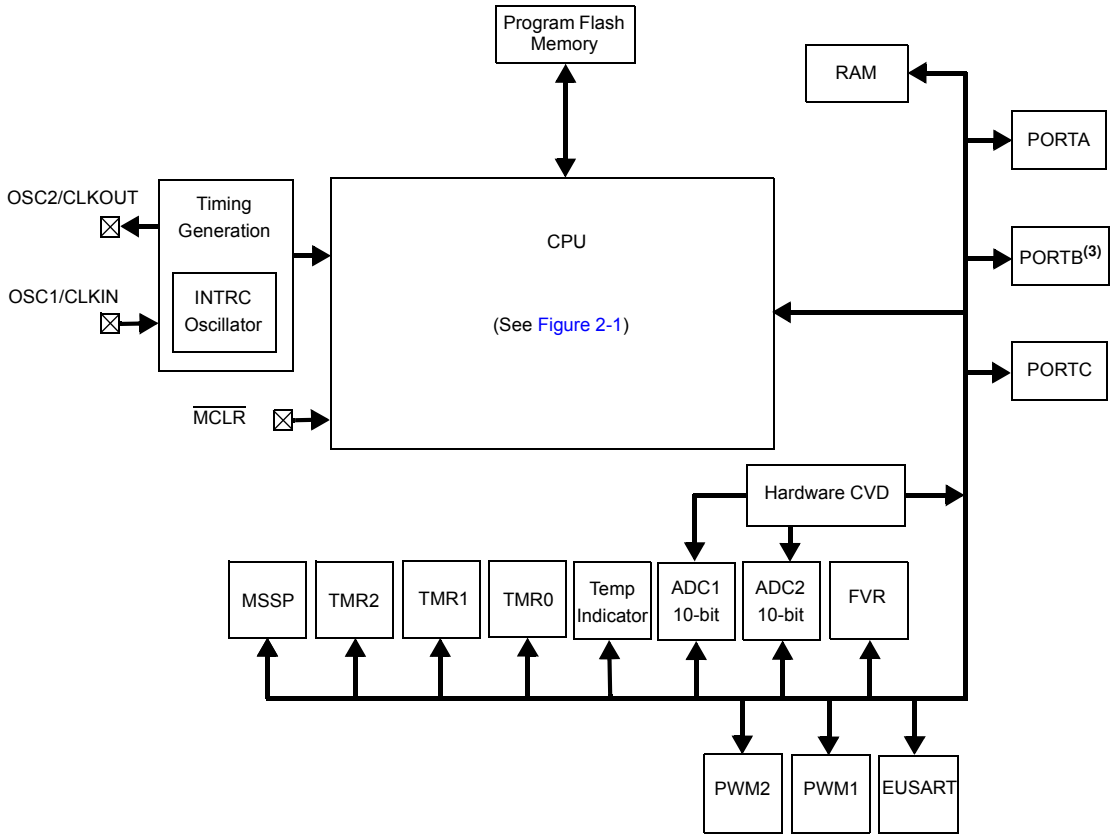
1.0 DEVICE OVERVIEW

The PIC16LF1554/1559 devices are described within this data sheet. The block diagram of these devices is shown in Figure 1-1, the available peripherals are shown in Table 1-1 and the pinout descriptions are shown in Table 1-2 and Table 1-3.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16LF1554	PIC16LF1559
Analog-to-Digital Converter (ADC)			
	ADC1	●	●
	ADC2	●	●
Hardware Capacitive Voltage Divider (CVD)		●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)		●	●
Fixed Voltage Reference (FVR)		●	●
Temperature Indicator		●	●
Master Synchronous Serial Ports			
	MSSP	●	●
PWM Modules			
	PWM1	●	●
	PWM2	●	●
Timers			
	Timer0	●	●
	Timer1	●	●
	Timer2	●	●

FIGURE 1-1: PIC16LF1554/1559 BLOCK DIAGRAM(1,2)



Note 1: See applicable chapters for more information on peripherals.
2: See Table 1-1 for peripherals available on specific devices.
3: PIC16LF1559 only.

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TABLE 1-2: PIC16LF1554 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/ISCPDAT/ICDDAT	RA0	TTL	CMOS	General Purpose I/O
	AN0	AN	—	ADC Channel Input
	ICSPDAT	ST	CMOS	ICSP™ Data I/O
	ICDDAT	ST	CMOS	In-Circuit Debug Data
RA1/AN1/VREF+/ICSPCLK/ICDCLK	RA1	TTL	CMOS	General Purpose I/O
	AN1	AN	—	ADC Channel Input
	VREF+	AN	—	ADC Positive Voltage Reference Input
	ICSPCLK	ST	CMOS	ICSP Programming Clock
	ICDCLK	ST	CMOS	In-Circuit Debug Clock
RA2/AN2/TOCKI/INT/	RA2	TTL	CMOS	General Purpose I/O
	AN2	AN	—	ADC Channel Input
	TOCKI	ST	—	Timer0 Clock Input
	INT	ST	—	External Interrupt
RA3/VPP/$\overline{SS}$(1)/SDA(1)/SDI(1)/ $\overline{MCLR}$	RA3	TTL	CMOS	General Purpose Input with IOC and WPU
	VPP	HV	—	Programming Voltage
	$\overline{SS}$	ST	—	Slave Select Input
	SDA	I^2C	OD	I^2C Data Input/Output
	SDI	CMOS	—	SPI Data Input
	$\overline{MCLR}$	ST	—	Master Clear with Internal Pull-up
RA4/AN10/ADTRIG/CLKOUT/ RX(1)/DT(1)/SDO(1)/T1G	RA4	TTL	CMOS	General Purpose I/O
	AN10	AN	—	ADC Channel Input
	ADTRIG	ST	—	ADC Conversion Trigger Input
	CLKOUT	—	CMOS	FOSC/4 Output
	RX	ST	—	USART Asynchronous Input
	DT	ST	CMOS	USART Synchronous Data
	SDO	—	CMOS	SPI Data Output
	T1G	ST	—	Timer1 Gate Input
RA5/AN20/CLKIN/T1CKI	RA5	TTL	CMOS	General Purpose I/O
	AN20	AN	—	ADC Channel Input
	CLKIN	CMOS	—	External Clock Input (EC mode)
	T1CKI	ST	—	Timer1 Clock Input
RC0/AN13/SCL/SCK	RC0	TTL	CMOS	General Purpose I/O
	AN13	AN	—	ADC Channel Input
	SCL	I^2C	OD	I^2C Clock
	SCK	ST	CMOS	SPI Clock

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

TABLE 1-2: PIC16LF1554 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC1/AN23/SDA(1)/SDI(1)	RC1	TTL	CMOS	General Purpose I/O
	AN23	AN	—	ADC Channel Input
	SDA	I^2C	OD	I^2C Data Input/Output
	SDI	CMOS	—	SPI Data Input
RC2/AN12/AD1GRDB(1)/AD2GRDB(1)/PWM1/SDO(1)	RC2	TTL	CMOS	General Purpose I/O
	AN12	AN	—	ADC Channel Input
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B
	PWM1	—	CMOS	PWM Output
	SDO	—	CMOS	SPI Data Output
RC3/AN22/AD1GRDB(1)/AD2GRDB(1)/PWM2/TX(1)/CK(1)/$\overline{SS}$(1)	RC3	TTL	CMOS	General Purpose I/O
	AN22	AN	—	ADC Channel Input
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B
	PWM2	—	CMOS	PWM Output
	TX	—	CMOS	USART Asynchronous Transmit
	CK	ST	CMOS	USART Synchronous Clock
	$\overline{SS}$	ST	—	Slave Select Input
RC4/AN11/AD1GRDA(1)/AD2GRDA(1)/TX(1)/CK(1)	RC3	TTL	CMOS	General Purpose I/O
	AN11	AN	—	ADC Channel Input
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output B
	TX	—	CMOS	USART Asynchronous Transmit
	CK	ST	CMOS	USART Synchronous Clock
RC5/AN21/AD1GRDA(1)/AD2GRDA(1)/RX(1)/DT(1)	RC5	TTL	CMOS	General Purpose I/O
	AN21	AN	—	ADC Channel Input
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output B
	RX	ST	—	USART Asynchronous Input
	DT	ST	CMOS	USART Synchronous Data

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

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TABLE 1-3: PIC16LF1559 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/ISCPDAT/ICDDAT	RA0	TTL	CMOS	General Purpose I/O
	AN0	AN	—	ADC Channel Input
	ICSPDAT	ST	CMOS	ICSP™ Data I/O
	ICDDAT	ST	CMOS	In-Circuit Debug Data
RA1/AN1/VREF+/ICSPCLK/ICDCLK	RA1	TTL	CMOS	General Purpose I/O
	AN1	AN	—	ADC Channel Input
	VREF+	AN	—	ADC Positive Voltage Reference Input
	ICSPCLK	ST	CMOS	ICSP Programming Clock
	ICDCLK	ST	CMOS	In-Circuit Debug Clock
RA2/AN2/TOCKI/INT	RA2	TTL	CMOS	General Purpose I/O
	AN2	AN	—	ADC Channel Input
	TOCKI	ST	—	Timer0 Clock Input
	INT	ST	—	External Interrupt
RA3/VPP/$\overline{SS}$(1)/SDA(1)/SDI(1)/$\overline{MCLR}$	RA3	TTL	CMOS	General Purpose Input with IOC and WPU
	VPP	HV	—	Programming Voltage
	$\overline{SS}$	ST	—	Slave Select Input
	SDA	I^2C	OD	I^2C Data Input/Output
	SDI	CMOS	—	SPI Data Input
	$\overline{MCLR}$	ST	—	Master Clear with Internal Pull-up
RA4/AN10/ADTRIG/CLKOUT/T1G	RA4	TTL	CMOS	General Purpose I/O
	AN10	AN	—	ADC Channel Input
	ADTRIG	ST	—	ADC Conversion Trigger Input
	CLKOUT	—	CMOS	FOSC/4 Output
	T1G	ST	—	Timer1 Gate input.
RA5/AN20/CLKIN/T1CKI	RA5	TTL	CMOS	General Purpose I/O
	AN20	AN	—	ADC Channel Input
	CLKIN	CMOS	—	External Clock Input (EC mode)
	T1CKI	ST	—	Timer1 clock Input
RB4/AN26/SDA(1)/SDI(1)	RB4	TTL	CMOS	General Purpose I/O
	AN26	AN	—	ADC Channel Input
	SDA	I^2C	OD	I^2C Data Input/Output
	SDI	CMOS	—	SPI Data Input

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

TABLE 1-3: PIC16LF1559 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB5/AN16/RX(1)/DT(1)	RB5	TTL	CMOS	General Purpose I/O
	AN16	AN	—	ADC Channel Input
	RX	ST	—	USART Asynchronous Input
	DT	ST	CMOS	USART Synchronous Data
RB6/AN25/SCL/SCK	RB6	TTL	CMOS	General Purpose I/O
	AN25	AN	—	ADC Channel Input
	SCL	I^2C	OD	I^2C Clock
	SCK	ST	CMOS	SPI Clock
RB7/AN15/TX/CK	RB7	TTL	CMOS	General Purpose I/O
	AN15	AN	—	ADC Channel Input
	TX	—	CMOS	USART Asynchronous Transmit
	CK	ST	CMOS	USART Synchronous Clock
RC0/AN13	RC0	TTL	CMOS	General Purpose I/O
	AN13	AN	—	ADC Channel Input
RC1/AN23	RC1	TTL	CMOS	General Purpose I/O
	AN23	AN	—	ADC Channel Input
RC2/AN12/AD1GRDB(1)/AD2GRDB(1) /PWM1	RC2	TTL	CMOS	General Purpose I/O
	AN12	AN	—	ADC Channel Input
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B
	PWM1	—	CMOS	PWM Output
RC3/AN22/AD1GRDB(1)/AD2GRDB(1) /PWM2	RC3	TTL	CMOS	General Purpose I/O
	AN22	AN	—	ADC Channel Input
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B
	PWM2	—	CMOS	PWM Output
RC4/AN11/AD1GRDA(1) /AD2GRDA(1)	RC4	TTL	CMOS	General Purpose I/O
	AN11	AN	—	ADC Channel Input
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output B
RC5/AN21/AD1GRDA(1)/AD2GRDA(1)	RC5	TTL	CMOS	General Purpose I/O
	AN21	AN	—	ADC Channel Input
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output B
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output B

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

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TABLE 1-3: PIC16LF1559 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC6/AN14/$\overline{SS}$(1)	RC6	TTL	CMOS	General Purpose I/O
	AN14	AN	—	ADC Channel Input
	$\overline{SS}$	ST	—	Slave Select Input
RC7/AN24/SDO	RC7	TTL	CMOS	General Purpose I/O
	AN24	AN	—	ADC Channel Input
	SDO	—	CMOS	SPI Data Output

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

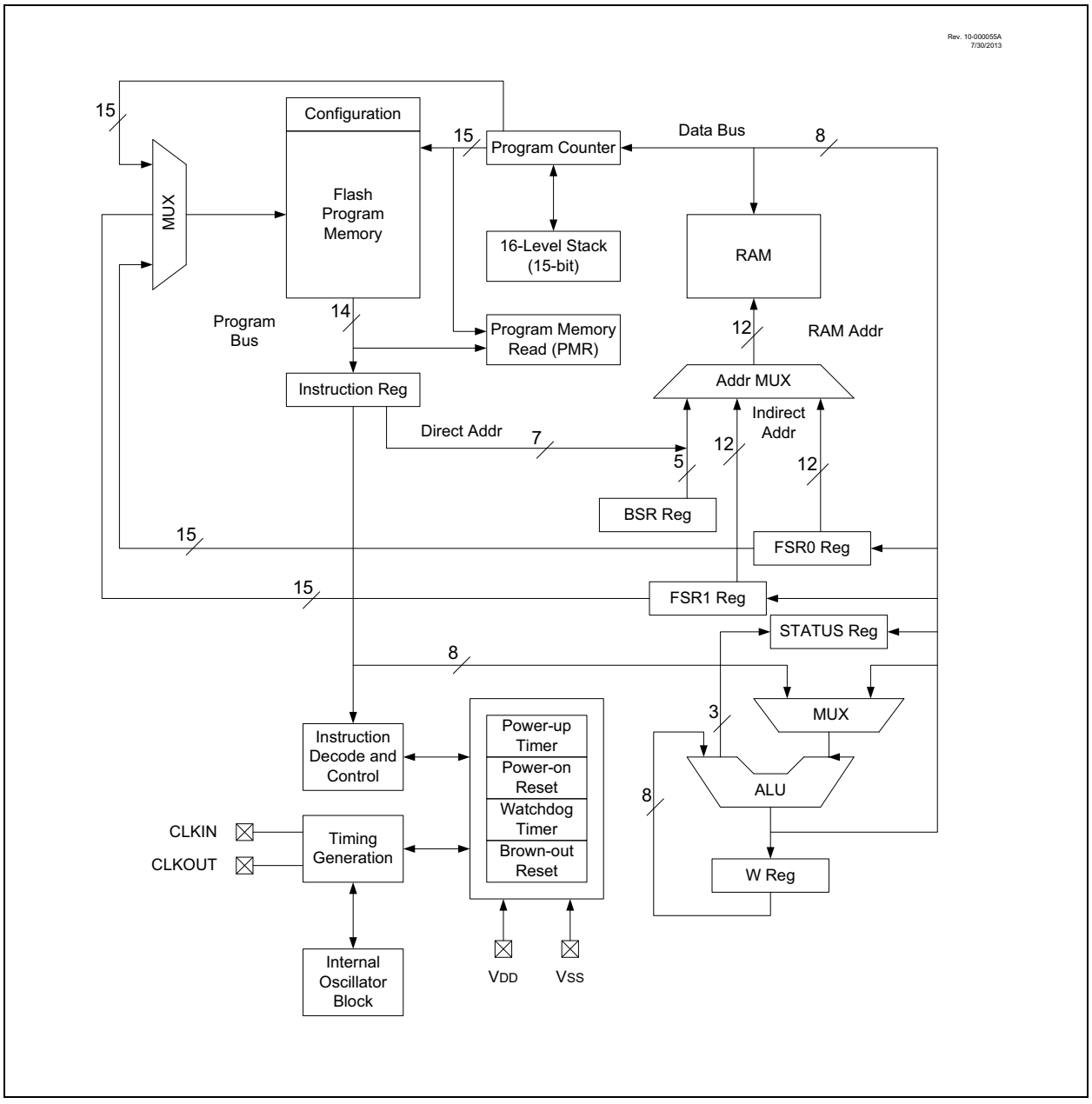
Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



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2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See section **Section 3.4 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.5 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 24.0 "Instruction Set Summary"** for more details.

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3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range (1)
PIC16LF1554	4,096	0FFFh	0F80h-0FFFh
PIC16LF1559	8,192	1FFFh	1F80h-1FFFh

Note 1: High-endurance Flash applies to low byte of each address in the range.

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FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16LF1554

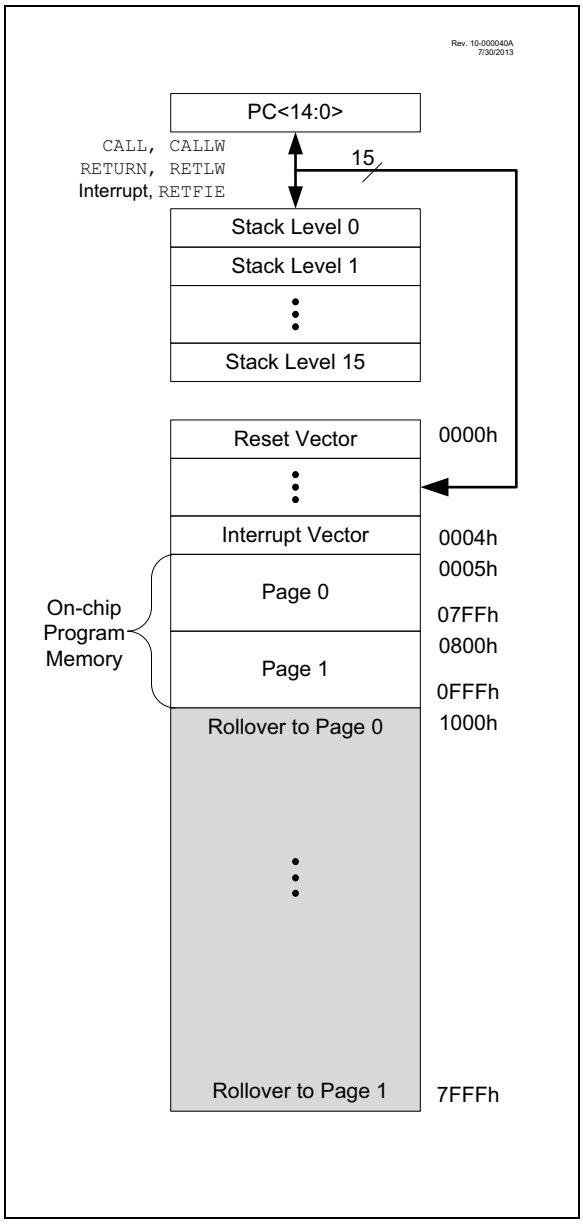
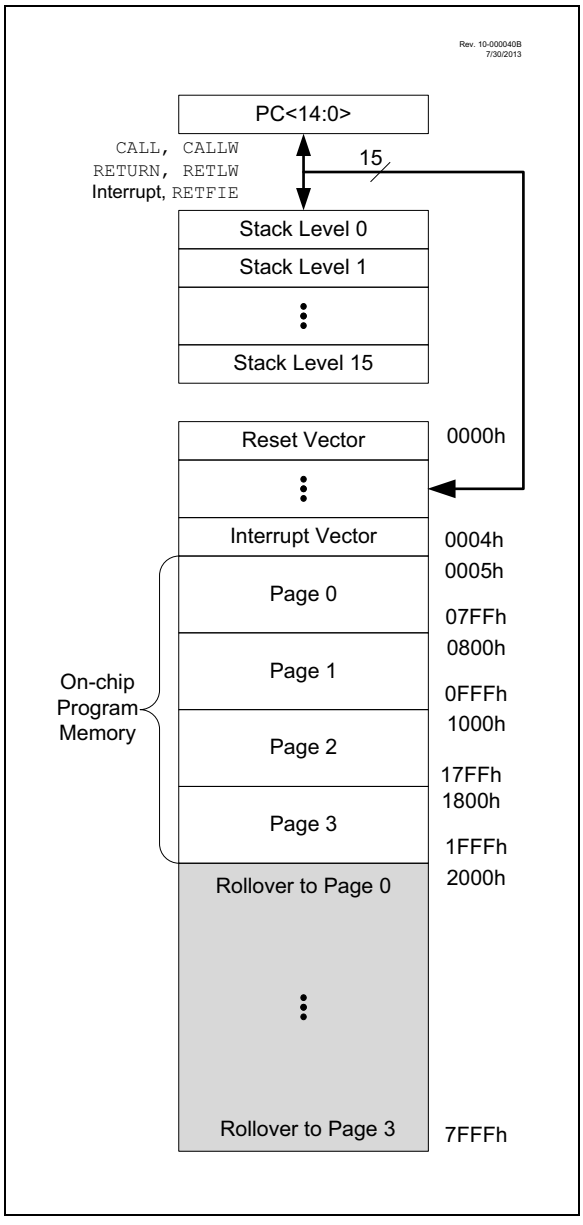


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16LF1559



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH operator will set bit 7 if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```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3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.5 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper five bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-8.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (refer to **Section 24.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

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3.2.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.2.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

3.2.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.5.2 "Linear Data Memory"** for more information.

3.2.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

3.2.5 DEVICE MEMORY MAPS

The memory maps for PIC16LF1554/1559 are as shown in Table 3-3 through Table 3-7.

FIGURE 3-3: BANKED MEMORY PARTITIONING

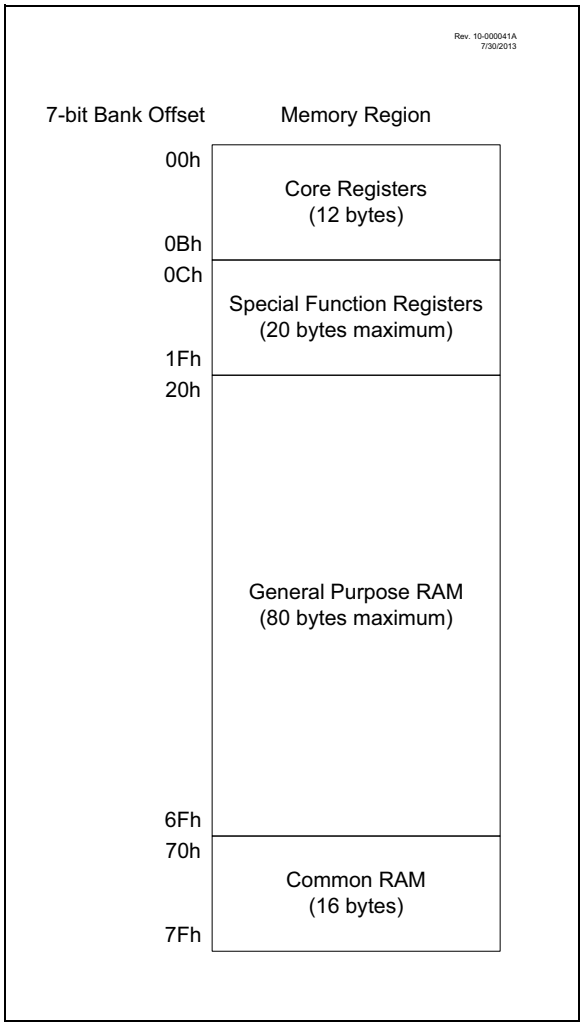

TABLE 3-3: PIC16LF1554 MEMORY MAP, BANKS 0-7

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	INDF0	080h	INDF0	100h	INDF0	180h	INDF0	200h	INDF0	280h	INDF0	300h	INDF0	380h	INDF0
001h	INDF1	081h	INDF1	101h	INDF1	181h	INDF1	201h	INDF1	281h	INDF1	301h	INDF1	381h	INDF1
002h	PCL	082h	PCL	102h	PCL	182h	PCL	202h	PCL	282h	PCL	302h	PCL	382h	PCL
003h	STATUS	083h	STATUS	103h	STATUS	183h	STATUS	203h	STATUS	283h	STATUS	303h	STATUS	383h	STATUS
004h	FSR0L	084h	FSR0L	104h	FSR0L	184h	FSR0L	204h	FSR0L	284h	FSR0L	304h	FSR0L	384h	FSR0L
005h	FSR0H	085h	FSR0H	105h	FSR0H	185h	FSR0H	205h	FSR0H	285h	FSR0H	305h	FSR0H	385h	FSR0H
006h	FSR1L	086h	FSR1L	106h	FSR1L	186h	FSR1L	206h	FSR1L	286h	FSR1L	306h	FSR1L	386h	FSR1L
007h	FSR1H	087h	FSR1H	107h	FSR1H	187h	FSR1H	207h	FSR1H	287h	FSR1H	307h	FSR1H	387h	FSR1H
008h	BSR	088h	BSR	108h	BSR	188h	BSR	208h	BSR	288h	BSR	308h	BSR	388h	BSR
009h	WREG	089h	WREG	109h	WREG	189h	WREG	209h	WREG	289h	WREG	309h	WREG	389h	WREG
00Ah	PCLATH	08Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH	20Ah	PCLATH	28Ah	PCLATH	30Ah	PCLATH	38Ah	PCLATH
00Bh	INTCON	08Bh	INTCON	10Bh	INTCON	18Bh	INTCON	20Bh	INTCON	28Bh	INTCON	30Bh	INTCON	38Bh	INTCON
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	—	30Ch	—	38Ch	—
00Dh	—	08Dh	—	10Dh	—	18Dh	—	20Dh	—	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	—	090h	—	110h	—	190h	—	210h	—	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	—	191h	PMADRL	211h	SSPBUF	291h	—	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	—	192h	PMADRH	212h	SSPADD	292h	—	312h	—	392h	IOCAN
013h	—	093h	—	113h	—	193h	PMDATL	213h	SSPMSK	293h	—	313h	—	393h	IOCAF
014h	—	094h	—	114h	—	194h	PMDATH	214h	SSPSTAT	294h	—	314h	—	394h	—
015h	TMR0	095h	OPTION	115h	—	195h	PMCON1	215h	SSPCON1	295h	—	315h	—	395h	—
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSPCON2	296h	—	316h	—	396h	—
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	SSPCON3	297h	—	317h	—	397h	—
018h	T1CON	098h	—	118h	—	198h	—	218h	—	298h	—	318h	—	398h	—
019h	T1GCON	099h	OSCCON	119h	—	199h	RCREG	219h	—	299h	—	319h	—	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TXREG	21Ah	—	29Ah	—	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL/ AD1RES0L(1)	11Bh	—	19Bh	SPBRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH/ AD1RES0H(1)	11Ch	—	19Ch	SPBRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0/ AD1CON0(1)	11Dh	APFCON	19Dh	RCSTA	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1/ ADCOMCON(1)	11Eh	—	19Eh	TXSTA	21Eh	—	29Eh	—	31Eh	—	39Eh	—
01Fh	—	09Fh	ADCON2/ AD1CON2(1)	11Fh	—	19Fh	BAUDCON	21Fh	—	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 96 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	Unimplemented Read as '0'	220h	Unimplemented Read as '0'	2A0h	Unimplemented Read as '0'	320h	Unimplemented Read as '0'	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h		0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: These ADC registers are the same as the registers in Bank 14.

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TABLE 3-4: PIC16LF1559 MEMORY MAP, BANKS 0-7

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	INDF0	080h	INDF0	100h	INDF0	180h	INDF0	200h	INDF0	280h	INDF0	300h	INDF0	380h	INDF0
001h	INDF1	081h	INDF1	101h	INDF1	181h	INDF1	201h	INDF1	281h	INDF1	301h	INDF1	381h	INDF1
002h	PCL	082h	PCL	102h	PCL	182h	PCL	202h	PCL	282h	PCL	302h	PCL	382h	PCL
003h	STATUS	083h	STATUS	103h	STATUS	183h	STATUS	203h	STATUS	283h	STATUS	303h	STATUS	383h	STATUS
004h	FSR0L	084h	FSR0L	104h	FSR0L	184h	FSR0L	204h	FSR0L	284h	FSR0L	304h	FSR0L	384h	FSR0L
005h	FSR0H	085h	FSR0H	105h	FSR0H	185h	FSR0H	205h	FSR0H	285h	FSR0H	305h	FSR0H	385h	FSR0H
006h	FSR1L	086h	FSR1L	106h	FSR1L	186h	FSR1L	206h	FSR1L	286h	FSR1L	306h	FSR1L	386h	FSR1L
007h	FSR1H	087h	FSR1H	107h	FSR1H	187h	FSR1H	207h	FSR1H	287h	FSR1H	307h	FSR1H	387h	FSR1H
008h	BSR	088h	BSR	108h	BSR	188h	BSR	208h	BSR	288h	BSR	308h	BSR	388h	BSR
009h	WREG	089h	WREG	109h	WREG	189h	WREG	209h	WREG	289h	WREG	309h	WREG	389h	WREG
00Ah	PCLATH	08Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH	20Ah	PCLATH	28Ah	PCLATH	30Ah	PCLATH	38Ah	PCLATH
00Bh	INTCON	08Bh	INTCON	10Bh	INTCON	18Bh	INTCON	20Bh	INTCON	28Bh	INTCON	30Bh	INTCON	38Bh	INTCON
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	—	30Ch	—	38Ch	—
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	—	090h	—	110h	—	190h	—	210h	—	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	—	191h	PMADRL	211h	SSPBUF	291h	—	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	—	192h	PMADRH	212h	SSPADD	292h	—	312h	—	392h	IOCAN
013h	—	093h	—	113h	—	193h	PMDATL	213h	SSPMSK	293h	—	313h	—	393h	IOCAF
014h	—	094h	—	114h	—	194h	PMDATH	214h	SSPSTAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION	115h	—	195h	PMCON1	215h	SSPCON1	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSPCON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	SSPCON3	297h	—	317h	—	397h	—
018h	T1CON	098h	—	118h	—	198h	—	218h	—	298h	—	318h	—	398h	—
019h	T1GCON	099h	OSCCON	119h	—	199h	RCREG	219h	—	299h	—	319h	—	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TXREG	21Ah	—	29Ah	—	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL/ AD1RES0L(1)	11Bh	—	19Bh	SPBRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH/ AD1RES0H(1)	11Ch	—	19Ch	SPBRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0/ AD1CON0(1)	11Dh	APFCON	19Dh	RCSTA	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1/ ADCOMCON(1)	11Eh	—	19Eh	TXSTA	21Eh	—	29Eh	—	31Eh	—	39Eh	—
01Fh	—	09Fh	ADCON2/ AD1CON2(1)	11Fh	—	19Fh	BAUDCON	21Fh	—	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 96 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 16 Bytes	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		330h	Unimplemented Read as '0'	3EFh	
070h	Accesses 70h – 7Fh	0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: These ADC registers are the same as the registers in Bank 14.

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