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PIC16LF1566/1567

28/40/44-Pin Flash, 8-Bit Microcontrollers with XLP Technology

Description

The PIC16LF1566/1567 microcontrollers deliver unique on-chip features for the design of mTouch® solutions and general purpose applications in 28/40/44-pin count packages. Two 10-bit high-speed ADCs with automated hardware CVD modules connect up to 34 analog channels to achieve a total sampling rate of 600k samples per second. This family provides mutual capacitance output drivers on all analog channels, two PWMs, two MSSP modules with low input voltage options and one EUSART, which makes this family an excellent solution to implement low-power and noise-robust capacitive sensing and other front-end sampling applications with minimal software overhead.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - 0-32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Three 8-bit Timers
- One 16-bit Timer
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-Out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

Memory

- Up to 8k Words Flash Program Memory
- 1024 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Operating Current:
  - 8 µA @ 32 kHz, 1.8V, typical
  - 32 µA/MHz @ 1.8V, typical

Digital Peripherals

- PWM: Two 10-bit Pulse-Width Modulators
  - Output on up to five pins per PWM at the same time
- Dual Master Synchronous Serial Port (MSSP) with SPI and I^2C:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
  - Configurable low input voltage threshold for I^2C
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, R-485, and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Interrupt-on-Change with edge-select

Intelligent Analog Peripherals

- Dual 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 35 external channels
  - Conversion available during Sleep
  - Temperature indicator
  - Simultaneous sampling on two ADCs
  - Connect multiple channels together for sampling
  - External conversion trigger
  - Fixed Voltage Reference as a channel
  - External pin as positive ADC voltage reference
  - Combined 600k samples per second
- Hardware Capacitive Voltage Divider (CVD)
  - Double-sample conversions
  - Two sets of result registers
  - 7-bit precharge timer
  - 7-bit acquisition timer
  - Two guard ring output drives
  - Mutual capacitance TX output on any analog channel
  - 30 pF adjustable sample and hold capacitor
- Internal Voltage Reference Module

Clocking Structure

- 16 MHz Internal Oscillator Block:
  - ±1% at calibration
  - Selectable frequency range from 0 to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Two external clock modes up to 32 MHz
- Oscillator Start-up Timer (OST)

Programming/Debug Features

- In-Circuit Debug Integrated On-Chip
- Emulation Header for Advanced Debug:
  - Provides trace, background debug and up to 32 hardware break points
- In-Circuit Serial Programming™ (ICSP™) via Two Pin

TABLE 1: PIC16LF1566/1567 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	SRAM (bytes)	I/Os (1)	10-bit ADCs(4)	Analog Channels(2)(3) CVD RX Channels	CVD TX Channels(5)	Timers 8/16-bit	EUSART	MSSP	PWM	Debug
PIC12LF1552	**(A)**	2048	0	256	6	1	4	1	1 / 0	-	1	-	-
PIC16LF1554	**(B)**	4096	0	256	12	2	10	2	2 / 1	1	1	2	I
PIC16LF1559	**(B)**	8192	0	512	18	2	16	2	2 / 1	1	1	2	I
PIC16LF1566	**(C)**	8192	0	1024	25	2	23	23	3 / 1	1	2	2	I
PIC16LF1567	**(C)**	8192	0	1024	36	2	34	34	3 / 1	1	2	2	I

Note 1: The $\overline{\text{MCLR}}$ pin is input-only.

2: Analog channels are split between the available ADCs.

3: Maximum usable analog channels assuming one pin must be assigned to output.

4: If V_{DD} > 2.4V, ADC may be overclocked 4x (T_{AD} = 0.25 µs).

5: Includes functionality of ADxGRDA output pin.

Data Sheet Index (Unshaded devices are described in this document.)

A: DS40001674 PIC12LF1552 Data Sheet, 8-Pin Flash, 8-Bit Microcontrollers

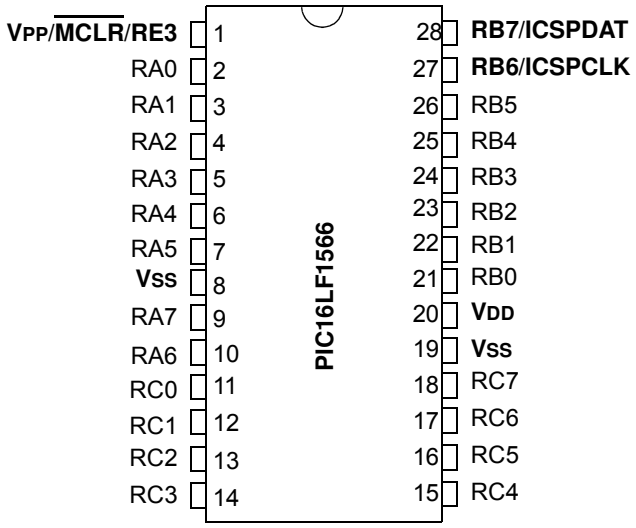
B: DS40001761 PIC16LF1554/1559 Data Sheet, 20-Pin Flash, 8-Bit Microcontrollers with XLP Technology

C: DS40001817 PIC16LF1566/1567 Data Sheet 28/40/44-Pin Flash, 8-Bit Microcontrollers with XLP Technology

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

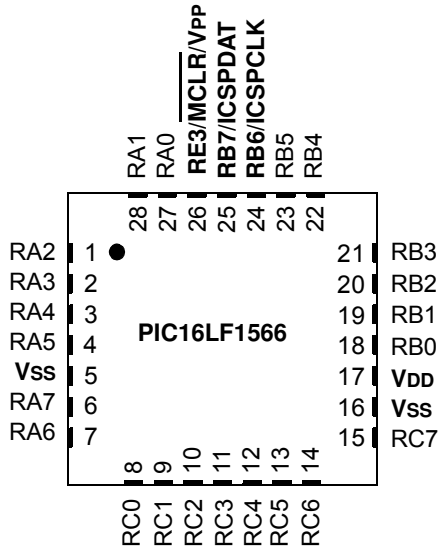
PIN DIAGRAMS

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP DIAGRAM FOR PIC16LF1566



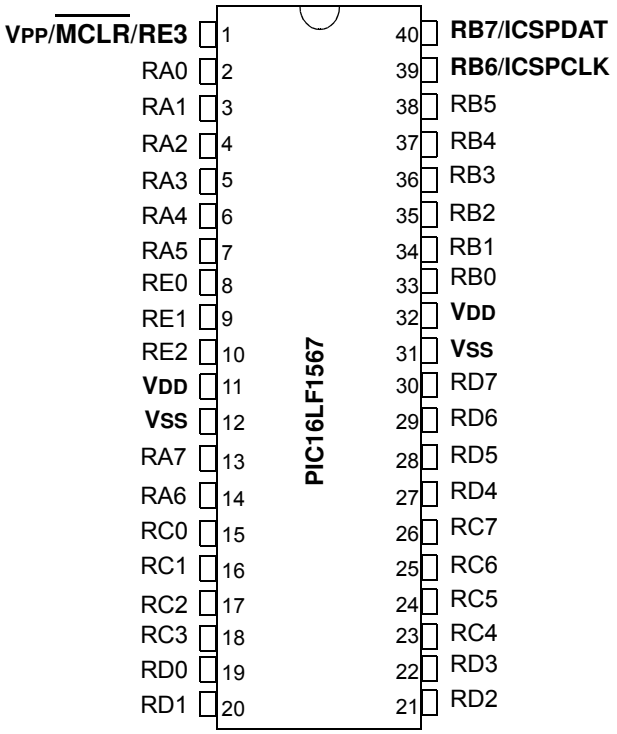
Note: See Table 2 for the pin allocation tables.

FIGURE 2: 28-PIN UQFN DIAGRAM FOR PIC16LF1566



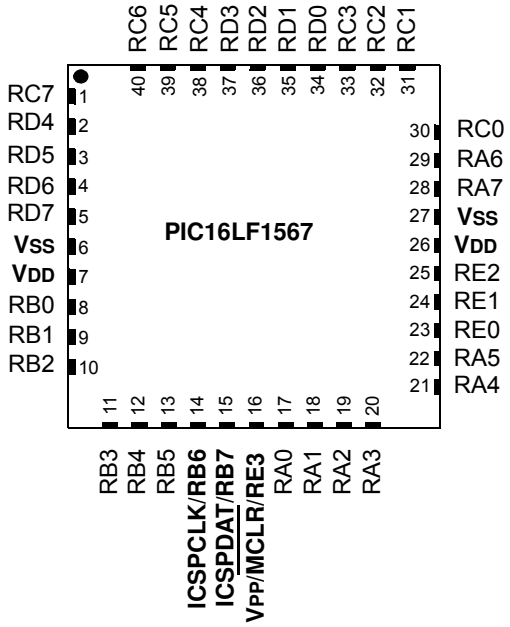
Note: See Table 2 or the pin allocation tables.

FIGURE 3: 40-PIN PDIP DIAGRAM FOR PIC16LF1567



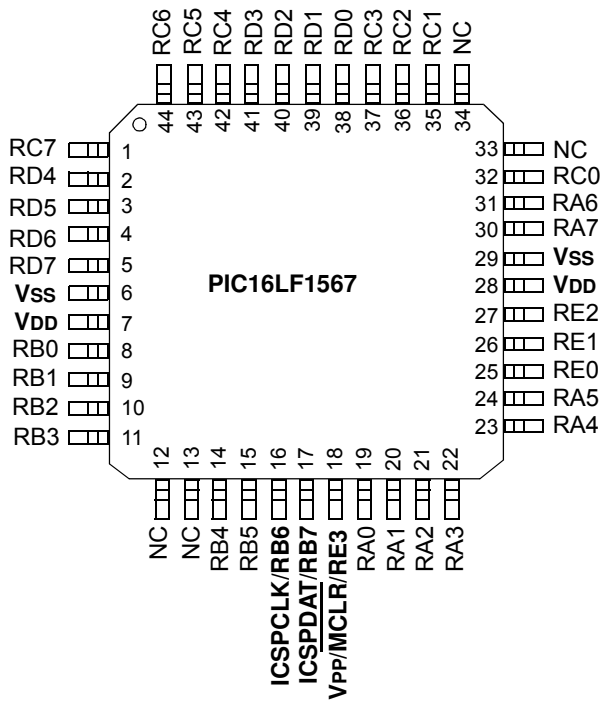
Note: See Table 3 for the pin allocation tables.

FIGURE 4: 40-PIN UQFN DIAGRAM FOR PIC16LF1567



Note: See Table 3 for the pin allocation tables.

FIGURE 5: 44-PIN TQFP DIAGRAM FOR PIC16LF1567



Note: See Table 3 for the pin allocation table.

PIN ALLOCATION TABLES

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16LF1566)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN20	—	—	PWM10	—	SS1(1)	—	—	—
RA1	3	28	AN10	—	—	PWM11	—	SS2	—	—	—
RA2	4	1	AN0	VREF-	—	PWM12	—	—	—	—	—
RA3	5	2	AN1	VREF+	—	PWM13	—	—	—	—	—
RA4	6	3	AN2	—	T0CKI	—	—	—	—	—	—
RA5	7	4	AN21	—	—	—	—	SS1(1)	—	—	—
RA6	10	7	AN22	ADTRIG	—	—	—	—	—	—	CLKOUT
RA7	9	6	AN11	—	—	—	—	—	—	—	CLKIN
RB0	21	18	AN16	—	—	PWM20	—	—	INT IOC	Y	—
RB1	22	19	AN27	—	—	PWM21	—	—	IOC	Y	—
RB2	23	20	AN17	—	—	PWM22	—	—	IOC	Y	—
RB3	24	21	AN28	—	—	PWM23	—	—	IOC	Y	—
RB4	25	22	AN18	AD1GRDA(1) AD2GRDA(1)	—	—	—	—	IOC	Y	—
RB5	26	23	AN29	AD1GRDA(1) AD2GRDA(1)	T1G	—	—	—	IOC	Y	—
RB6	27	24	AN19	AD1GRDB(1) AD2GRDB(1)	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RB7	28	25	AN40	AD1GRDB(1) AD2GRDB(1)	—	—	—	—	IOC	Y	ICSPDAT ICDDAT
RC0	11	8	AN12	—	T1CKI	—	—	SDO2	—	—	—
RC1	12	9	AN23	—	—	PWM2	—	SCL2 SCK2	—	—	—
RC2	13	10	AN13	—	—	PWM1	—	SDA2 SDI2	—	—	—
RC3	14	11	AN24	—	—	—	—	SCL1 SCK1	—	—	—
RC4	15	12	AN14	—	—	—	—	SDA1 SDI1	—	—	—
RC5	16	13	AN25	—	—	—	—	SDO1 I^2CLVL	—	—	—

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16LF1566) (CONTINUED)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-up	Basic
RC6	17	14	AN15	—	—	—	TX CK	—	—	—	—
RC7	18	15	AN26	—	—	—	RX DT	—	—	—	—
RE3	1	26	—	—	—	—	—	—	—	Y	$\overline{\text{MCLR}}$ V_{PP}
V_{DD}	20	17	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8	5	—	—	—	—	—	—	—	—	V_{SS}
V_{SS}	19	16	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Pin functions can be assigned to one of two pin locations via software.

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16LF1567)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-Up	Basic
RA0	2	17	19	AN20	—	—	PWM10	—	SS1(1)	—	—	—
RA1	3	18	20	AN10	—	—	PWM11	—	SS2	—	—	—
RA2	4	19	21	AN0	VREF-	—	PWM12	—	—	—	—	—
RA3	5	20	22	AN1	VREF+		PWM13	—	—	—	—	—
RA4	6	21	23	AN2	—	T0CKI	—	—	—	—	—	—
RA5	7	22	24	AN21	—	—	—	—	SS1(1)	—	—	—
RA6	14	29	31	AN22	ADTRIG	—	—	—	—	—	—	CLKOUT
RA7	13	28	30	AN11	—	—	—	—	—	—	—	CLKIN
RB0	33	8	8	AN16	—	—	PWM20	—	—	INT IOC	Y	—
RB1	34	9	9	AN27	—	—	PWM21	—	—	IOC	Y	—
RB2	35	10	10	AN17	—	—	PWM22	—	—	IOC	Y	—
RB3	36	11	11	AN28	—	—	PWM23	—	—	IOC	Y	—
RB4	37	12	14	AN18	AD1GRDA(1) AD2GRDA(1)	—	—	—	—	IOC	Y	—
RB5	38	13	15	AN29	AD1GRDA(1) AD2GRDA(1)	T1G	—	—	—	IOC	Y	—
RB6	39	14	16	AN19	AD1GRDB(1) AD2GRDB(1)	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RB7	40	15	17	AN40	AD1GRDB(1) AD2GRDB(1)	—	—	—	—	IOC	Y	ICSPDAT ICDDAT
RC0	15	30	32	AN12	—	T1CKI	—	—	SDO2	—	—	—
RC1	16	31	35	AN23	—	—	PWM2	—	SCL2 SCK2	—	—	—
RC2	17	32	36	AN13	—	—	PWM1	—	SDA2 SDI2	—	—	—
RC3	18	33	37	AN24	—	—	—	—	SCL1 SCK1	—	—	—
RC4	23	38	42	AN14	—	—	—	—	SDA1 SDI1	—	—	—
RC5	24	39	43	AN25	—	—	—	—	SDO1 I2CLVL	—	—	—
RC6	25	40	44	AN15	—	—	—	TX CK	—	—	—	—
RC7	26	1	1	AN26	—	—	—	RX DT	—	—	—	—
RD0	19	34	38	AN42	—	—	—	—	—	—	—	—

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16LF1567) (CONTINUED)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-Up	Basic
RD1	20	35	39	AN32	—	—	—	—	—	—	—	—
RD2	21	36	40	AN43	—	—	—	—	—	—	—	—
RD3	22	37	41	AN33	—	—	—	—	—	—	—	—
RD4	27	2	2	AN34	—	—	—	—	—	—	—	—
RD5	28	3	3	AN44	—	—	—	—	—	—	—	—
RD6	29	4	4	AN35	—	—	—	—	—	—	—	—
RD7	30	5	5	AN45	—	—	—	—	—	—	—	—
RE0	8	23	25	AN30	—	—	—	—	—	—	—	—
RE1	9	24	26	AN41	—	—	—	—	—	—	—	—
RE2	10	25	27	AN31	—	—	—	—	—	—	—	—
RE3	1	16	18	—	—	—	—	—	—	—	Y	$\overline{\text{MCLR}}$ V_{PP}
V_{DD}	11	7	7	—	—	—	—	—	—	—	—	V_{DD}
V_{DD}	—	26	28	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	12	6	6	—	—	—	—	—	—	—	—	V_{SS}
V_{SS}	31	27	29	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Pin functions can be assigned to one of two pin locations via software.

Table of Contents

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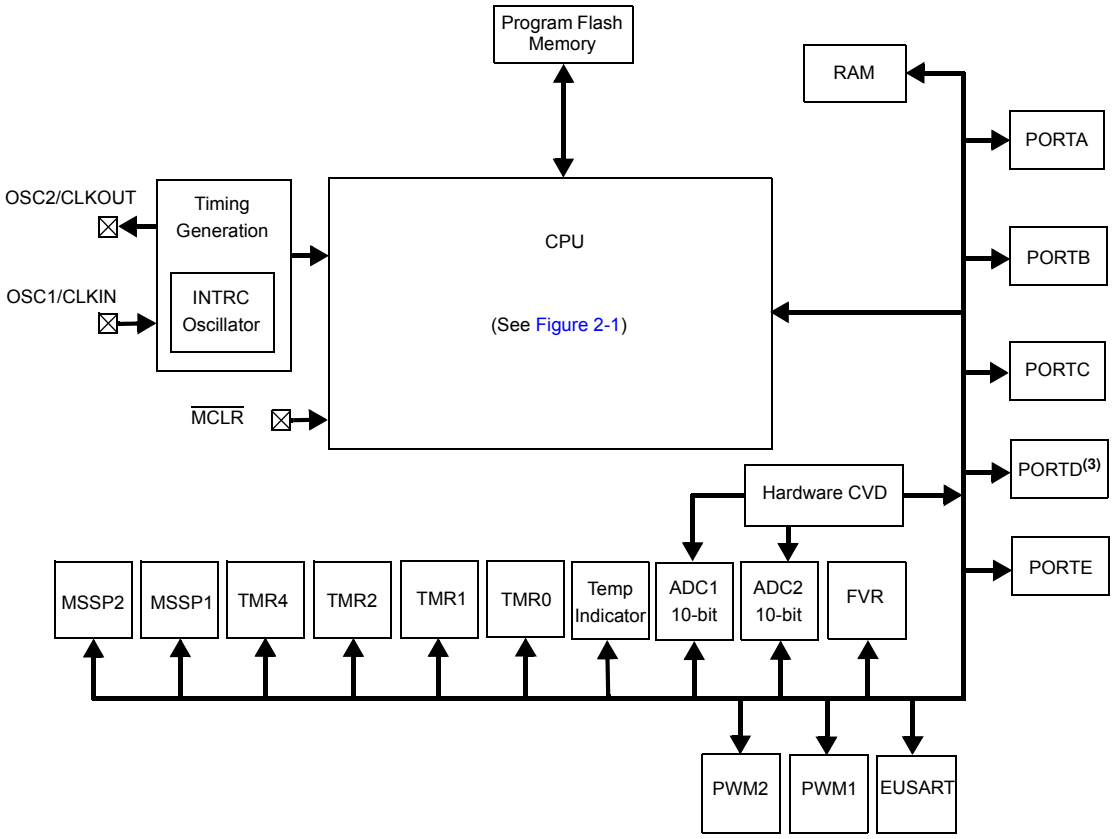
1.0 DEVICE OVERVIEW

The PIC16LF1566/1567 devices are described within this data sheet. The block diagram of these devices is shown in Figure 1-1, the available peripherals are shown in Table 1-1 and the pinout descriptions are shown in Table 1-2 and Table 1-3.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16LF1566	PIC16LF1567
Analog-to-Digital Converter (ADC)			
	ADC1	●	●
	ADC2	●	●
Hardware Capacitive Voltage Divider (CVD)		●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)		●	●
Fixed Voltage Reference (FVR)		●	●
Temperature Indicator		●	●
Master Synchronous Serial Ports			
	MSSP1	●	●
	MSSP2	●	●
PWM Modules			
	PWM1	●	●
	PWM2	●	●
Timers			
	Timer0	●	●
	Timer1	●	●
	Timer2	●	●
	Timer4	●	●

FIGURE 1-1: PIC16LF1566/1567 BLOCK DIAGRAM(1,2)



Note 1: See applicable chapters for more information on peripherals.
2: See Table 1-1 for peripherals available on specific devices.
3: PIC16LF1567 only.

TABLE 1-2: PIC16LF1566 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN20/PWM10/SS1(1)	RA0	TTL	CMOS	General Purpose I/O.
	AN20	AN	—	ADC Channel Input for ADC2.
	PWM10	—	CMOS	PWM Output for PWM1.
	SS1	ST	—	Slave Select Input for MSSP1.
RA1/AN10/PWM11/SS2	RA1	TTL	CMOS	General Purpose I/O.
	AN10	AN	—	ADC Channel Input for ADC1.
	PWM11	—	CMOS	PWM Output for PWM1.
	SS2	ST	—	Slave Select Input for MSSP2.
RA2/AN0/PWM12	RA2	TTL	CMOS	General Purpose I/O.
	AN0	AN	—	ADC Channel Input for both ADC1 and ADC2.
	PWM12	—	CMOS	PWM Output for PWM1.
	VREF-	AN	—	ADC Negative Voltage Reference Input
RA3/AN1/ V_{REF+}/PWM13	RA3	TTL	CMOS	General Purpose I/O.
	AN1	AN	—	ADC Channel Input for both ADC1 and ADC2.
	V_{REF+}	AN	—	ADC Positive Voltage Reference Input.
	PWM13	—	CMOS	PWM Output for PWM1.
RA4/AN2/T0CKI	RA4	TTL	CMOS	General Purpose I/O.
	AN2	AN	—	ADC Channel Input for both ADC1 and ADC2.
	T0CKI	ST	—	Timer0 Clock Input.
RA5/AN21/SS1(1)	RA5	TTL	CMOS	General Purpose I/O.
	AN21	AN	—	ADC Channel Input for ADC2.
	SS1	ST	—	Slave Select Input for MSSP1.
RA6/AN22/ADTRIG/CLKOUT	RA6	TTL	CMOS	General Purpose I/O.
	AN22	AN	—	ADC Channel Input for ADC2.
	ADTRIG	ST	—	ADC Conversion Trigger Input.
	CLKOUT	—	CMOS	F_{OSC}/4 Output.
RA7/AN11/CLKIN	RA7	TTL	CMOS	General Purpose I/O.
	AN11	AN	—	ADC Channel Input for ADC1.
	CLKIN	CMOS	—	External Clock Input (EC mode).
RB0/AN16/PWM20/INT	RB0	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN16	AN	—	ADC Channel Input for ADC1.
	PWM20	—	CMOS	PWM Output for PWM2.
	INT	ST	—	External Interrupt.
RB1/AN27/PWM21	RB1	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN27	AN	—	ADC Channel Input for ADC2.
	PWM21	—	CMOS	PWM Output for PWM2.
RB2/AN17/PWM22	RB2	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN17	AN	—	ADC Channel Input for ADC1.
	PWM22	—	CMOS	PWM Output for PWM2.

TABLE 1-2: PIC16LF1566 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3/AN28/PWM23	RB3	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN28	AN	—	ADC Channel Input for ADC2.
	PWM23	—	CMOS	PWM Output for PWM2.
RB4/AN18/AD1GRDA(1)/AD2GRDA(1)	RB4	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN18	AN	—	ADC Channel Input for ADC1.
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output A.
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output A.
RB5/AN29/AD1GRDA(1)/AD2GRDA(1)/T1G	RB5	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN29	AN	—	ADC Channel Input for ADC2.
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output A.
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output A.
	T1G	ST	—	Timer1 Gate Input.
RB6/AN19/AD1GRDB(1)/AD2GRDB(1)/ ICSPCLK/ICDCLK	RB6	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN19	AN	—	ADC Channel Input for ADC1.
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B.
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B.
	ICSPCLK	ST	CMOS	ICSP™ Programming Clock.
	ICDCLK	ST	CMOS	In-Circuit Debug Clock.
RB7/AN40/AD1GRDB(1)/AD2GRDB(1)/ ICSPDAT/ICDDAT	RB7	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN40	AN	—	ADC Channel Input for ADC2.
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B.
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Debug Data.
RC0/AN12/T1CKI/SDO2	RC0	TTL	CMOS	General Purpose I/O.
	AN12	AN	—	ADC Channel Input for ADC1.
	T1CKI	ST	—	Timer1 Clock Input.
	SDO2	—	CMOS	SPI Data Output for MSSP2.
RC1/AN23/PWM2/SCL2/SCK2	RC1	TTL	CMOS	General Purpose I/O.
	AN23	AN	—	ADC Channel Input for ADC2.
	PWM2	—	CMOS	PWM Output for PWM2.
	SCL2	I^2C	OD	I^2C Clock for MSSP2.
	SCK2	ST	CMOS	SPI Clock for MSSP2.
RC2/AN13/PWM1/SDA2/SDI2	RC2	TTL	CMOS	General Purpose I/O.
	AN13	AN	—	ADC Channel Input for ADC1.
	PWM1	—	CMOS	PWM Output for PWM1.
	SDA2	I^2C	OD	I^2C Data for MSSP2.
	SDI2	CMOS	—	SPI Data Input for MSSP2.
RC3/AN24/SCL1/SCK1	RC3	TTL	CMOS	General Purpose I/O.
	AN24	AN	—	ADC Channel Input for ADC2.
	SCL1	I^2C	OD	I^2C Clock for MSSP1.
	SCK1	ST	CMOS	SPI Clock for MSSP1.

TABLE 1-2: PIC16LF1566 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/AN14/SDA1/SDI1	RC4	TTL	CMOS	General Purpose I/O.
	AN14	AN	—	ADC Channel Input for ADC1.
	SDA1	I^2C	OD	I^2C Data for MSSP1.
	SDI1	CMOS	—	SPI Data Input for MSSP1.
RC5/AN25/SDO1/I2CLVL	RC5	TTL	CMOS	General Purpose I/O.
	AN25	AN	—	ADC Channel Input for ADC2.
	SDO1	—	CMOS	SPI Data Output for MSSP1.
	I2CLVL	AN	—	I^2C Voltage Level Input.
RC6/AN15/TX/CK	RC6	TTL	—	General Purpose I/O.
	AN15	AN	—	ADC Channel Input for ADC1.
	TX	—	CMOS	EUSART Asynchronous Transmit.
	CK	ST	CMOS	EUSART Synchronous Clock.
RC7/AN26/RX/DT	RC7	TTL	CMOS	General Purpose I/O.
	AN26	AN	—	ADC Channel Input for ADC2.
	RX	ST	—	EUSART Asynchronous Input.
	DT	ST	CMOS	EUSART Synchronous Data.
RE3/V_{PP}/$\overline{MCLR}$	RE3	TTL	—	General Purpose Input with WPU.
	V_{PP}	HV	—	Programming Voltage.
	$\overline{MCLR}$	ST	—	Master Clear with Internal Pull-up.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

TABLE 1-3: PIC16LF1567 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN20/PWM10/SS1(1)	RA0	TTL	CMOS	General Purpose I/O.
	AN20	AN	—	ADC Channel Input for ADC2.
	PWM10	—	CMOS	PWM Output for PWM1.
	SS1	ST	—	Slave Select Input for MSSP1.
RA1/AN10/PWM11/SS2	RA1	TTL	CMOS	General Purpose I/O.
	AN10	AN	—	ADC Channel Input for ADC1.
	PWM11	—	CMOS	PWM Output for PWM1.
	SS2	ST	—	Slave Select Input for MSSP2.
RA2/AN0/PWM12	RA2	TTL	CMOS	General Purpose I/O.
	AN0	AN	—	ADC Channel Input for both ADC1 and ADC2.
	V_{REF-}	AN	—	ADC Negative Voltage Reference Input
	PWM12	—	CMOS	PWM Output for PWM1.
RA3/AN1/V_{REF+}/PWM13	RA3	TTL	CMOS	General Purpose I/O.
	AN1	AN	—	ADC Channel Input for both ADC1 and ADC2.
	V_{REF+}	AN	—	ADC Positive Voltage Reference Input.
	PWM13	—	CMOS	PWM Output for PWM1.
RA4/AN2/T0CKI	RA4	TTL	CMOS	General Purpose I/O.
	AN2	AN	—	ADC Channel Input for both ADC1 and ADC2.
	T0CKI	ST	—	Timer0 Clock Input.
RA5/AN21/SS1(1)	RA5	TTL	CMOS	General Purpose I/O.
	AN21	AN	—	ADC Channel Input for ADC2.
	SS1	ST	—	Slave Select Input for MSSP1.
RA6/AN22/ADTRIG/CLKOUT	RA6	TTL	CMOS	General Purpose I/O.
	AN22	AN	—	ADC Channel Input for ADC2.
	ADTRIG	ST	—	ADC Conversion Trigger Input.
	CLKOUT	—	CMOS	F_{OSC}/4 Output.
RA7/AN11/CLKIN	RA7	TTL	CMOS	General Purpose I/O.
	AN11	AN	—	ADC Channel Input for ADC1.
	CLKIN	CMOS	—	External Clock Input (EC mode).
RB0/AN16/PWM20/INT	RB0	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN16	AN	—	ADC Channel Input for ADC1.
	PWM20	—	CMOS	PWM Output for PWM2.
	INT	ST	—	External Interrupt.
RB1/AN27/PWM21	RB1	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN27	AN	—	ADC Channel Input for ADC2.
	PWM21	—	CMOS	PWM Output for PWM2.
RB2/AN17/PWM22	RB2	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN17	AN	—	ADC Channel Input for ADC1.
	PWM22	—	CMOS	PWM Output for PWM2.

TABLE 1-3: PIC16LF1567 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3/AN28/PWM23	RB3	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN28	AN	—	ADC Channel Input for ADC2.
	PWM23	—	CMOS	PWM Output for PWM2.
RB4/AN18/AD1GRDA(1)/AD2GRDA(1)	RB4	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN18	AN	—	ADC Channel Input for ADC1.
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output A.
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output A.
RB5/AN29/AD1GRDA(1)/AD2GRDA(1)/ T1G	RB5	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN29	AN	—	ADC Channel Input for ADC2.
	AD1GRDA	—	CMOS	ADC1 Guard Ring Output A.
	AD2GRDA	—	CMOS	ADC2 Guard Ring Output A.
	T1G	ST	—	Timer1 Gate Input
RB6/AN19/AD1GRDB(1)/AD2GRDB(1)/ ICSPCLK/ICDCLK	RB6	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN19	AN	—	ADC Channel Input for ADC1.
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B.
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B.
	ICSPCLK	ST	CMOS	ICSP™ Programming Clock.
	ICDCLK	ST	CMOS	In-Circuit Debug Clock.
RB7/AN40/AD1GRDB(1)/AD2GRDB(1)/ ICSPDAT/ICDDAT	RB7	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN40	AN	—	ADC Channel Input for ADC2.
	AD1GRDB	—	CMOS	ADC1 Guard Ring Output B.
	AD2GRDB	—	CMOS	ADC2 Guard Ring Output B.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Debug Data.
RC0/AN12/T1CKI/SDO2	RC0	TTL	CMOS	General Purpose I/O.
	AN12	AN	—	ADC Channel Input for ADC1.
	T1CKI	ST	—	Timer1 Clock Input.
	SDO2	—	CMOS	SPI Data Output for MSSP2.
RC1/AN23/PWM2/SCL2/SCK2	RC1	TTL	CMOS	General Purpose I/O.
	AN23	AN	—	ADC Channel Input for ADC2.
	PWM2	—	CMOS	PWM Output for PWM2.
	SCL2	I^2C	OD	I^2C Clock for MSSP2.
	SCK2	ST	CMOS	SPI Clock for MSSP2.
RC2/AN13/PWM1/SDA2/SDI2	RC2	TTL	CMOS	General Purpose I/O.
	AN13	AN	—	ADC Channel Input for ADC1.
	PWM1	—	CMOS	PWM Output for PWM1.
	SDA2	I^2C	OD	I^2C Data for MSSP2.
	SDI2	CMOS	—	SPI Data Input for MSSP2.
RC3/AN24/SCL1/SCK1	RC3	TTL	CMOS	General Purpose I/O.
	AN24	AN	—	ADC Channel Input for ADC2.
	SCL1	I^2C	OD	I^2C Clock for MSSP1.
	SCK1	ST	CMOS	SPI Clock for MSSP1.

TABLE 1-3: PIC16LF1567 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/AN14/SDA1/SDI1	RC4	TTL	CMOS	General Purpose I/O.
	AN14	AN	—	ADC Channel Input for ADC1.
	SDA1	I^2C	OD	I^2C Data for MSSP1.
	SDI1	CMOS	—	SPI Data Input for MSSP1.
RC5/AN25/SDO1/I2CLVL	RC5	TTL	CMOS	General Purpose I/O.
	AN25	AN	—	ADC Channel Input for ADC2.
	SDO1	—	CMOS	SPI Data Output for MSSP1.
	I2CLVL	AN	—	I^2C Voltage Level Input.
RC6/AN15/TX/CK	RC6	TTL	CMOS	General Purpose I/O.
	AN15	AN	—	ADC Channel Input for ADC1.
	TX	—	CMOS	EUSART Asynchronous Transmit.
	CK	ST	CMOS	EUSART Synchronous Clock.
RC7/AN26/RX/DT	RC7	TTL	CMOS	General Purpose I/O.
	AN26	AN	—	ADC Channel Input for ADC2.
	RX	ST	—	EUSART Asynchronous Input.
	DT	ST	CMOS	EUSART Synchronous Data.
RD0/AN42	RD0	TTL	CMOS	General Purpose I/O.
	AN42	AN	—	ADC Channel Input for ADC2.
RD1/AN32	RD1	TTL	CMOS	General Purpose I/O.
	AN32	AN	—	ADC Channel Input for ADC1.
RD2/AN43	RD2	TTL	CMOS	General Purpose I/O.
	AN43	AN	—	ADC Channel Input for ADC2.
RD3/AN33	RD3	TTL	CMOS	General Purpose I/O.
	AN33	AN	—	ADC Channel Input for ADC1.
RD4/AN34	RD4	TTL	CMOS	General Purpose I/O.
	AN34	AN	—	ADC Channel Input for ADC1.
RD5/AN44	RD5	TTL	CMOS	General Purpose I/O.
	AN44	AN	—	ADC Channel Input for ADC2.
RD6/AN35	RD6	TTL	CMOS	General Purpose I/O.
	AN35	AN	—	ADC Channel Input for ADC1.
RD7/AN45	RD7	TTL	CMOS	General Purpose I/O.
	AN45	AN	—	ADC Channel Input for ADC2.
RE0/AN30	RE0	TTL	CMOS	General Purpose I/O.
	AN30	AN	—	ADC Channel Input for ADC1.
RE1/AN41	RE1	TTL	CMOS	General Purpose I/O.
	AN41	AN	—	ADC Channel Input for ADC2.
RE2/AN31	RE2	TTL	CMOS	General Purpose I/O.
	AN31	AN	—	ADC Channel Input for ADC1.
RE3/VPP/$\overline{MCLR}$	RE3	TTL	—	General Purpose Input with WPU.
	VPP	HV	—	Programming Voltage.
	$\overline{MCLR}$	ST	—	Master Clear with Internal Pull-up.

TABLE 1-3: PIC16LF1567 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

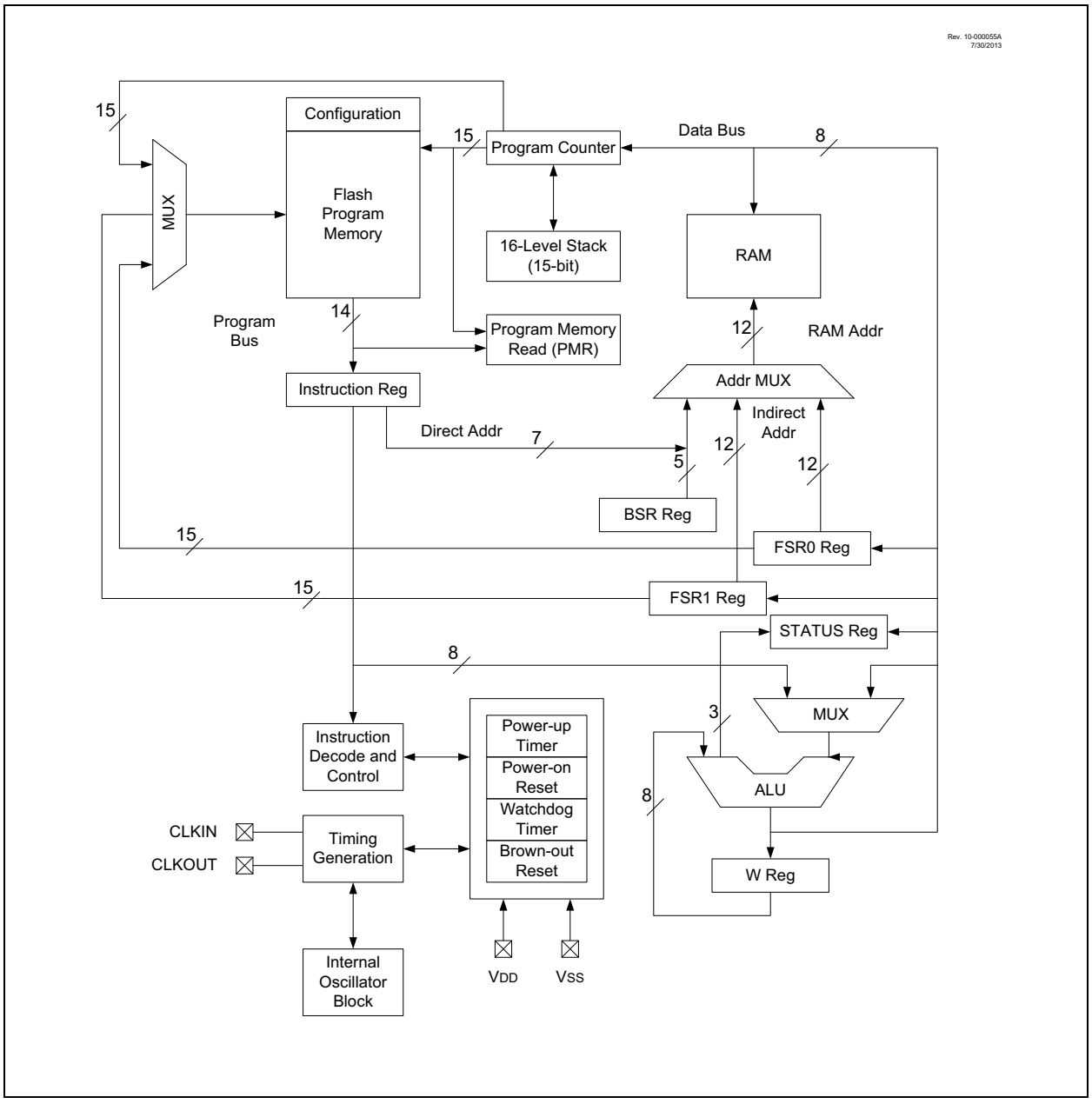
Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See section **Section 3.4 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.5 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 24.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

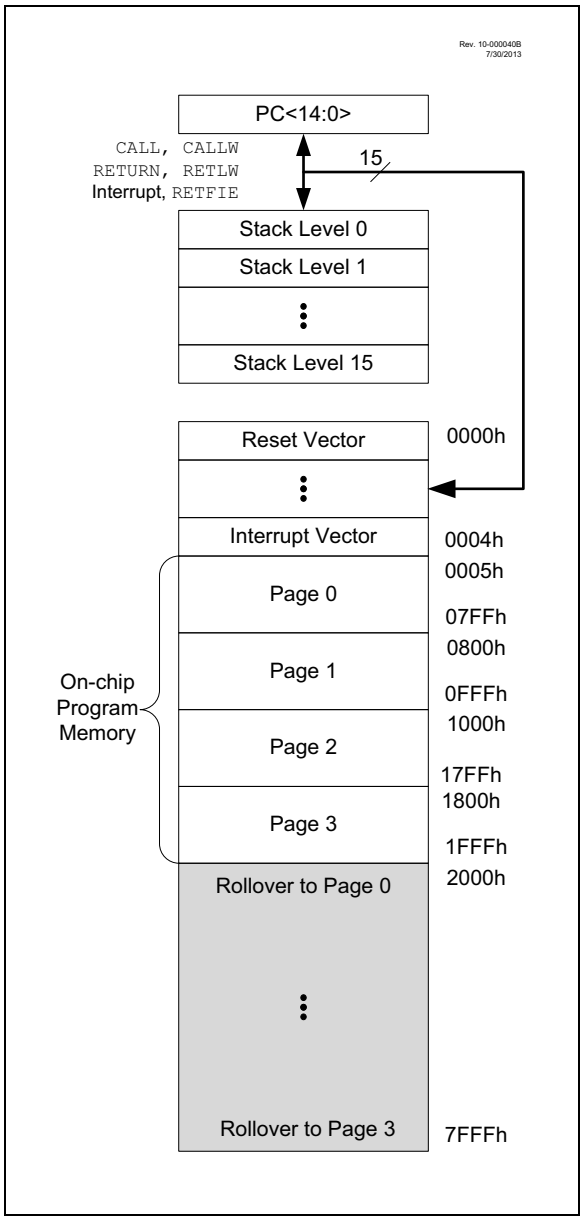
The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range (1)
PIC16LF1566	8,192	1FFFh	1F80h-1FFFh
PIC16LF1567	8,192	1FFFh	1F80h-1FFFh

Note 1: High-endurance Flash applies to low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16LF1566/1567



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH operator will set bit 7 if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
     DW          DATA0    ; First constant
     DW          DATA1    ; Second constant
     DW          DATA2
     DW          DATA3
my_function
     ;… LOTS OF CODE…
     MOVLW     DATA_INDEX
     ADDLW     LOW constants
     MOVWF     FSR1L
     MOVLW     HIGH constants; MSb is set
automatically
     MOVWF     FSR1H
     BTFSC     STATUS,C     ; carry from ADDLW?
     INCF      FSR1H,f      ; yes
     MOVIW     0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-2):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.5 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper five bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-10.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u u1uu' (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (refer to **Section 24.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and Digit $\overline{Borrow}$ out bits, respectively, in subtraction.

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Digit Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit(1) (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

3.2.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.2.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

3.2.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.5.2 "Linear Data Memory"** for more information.

3.2.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

3.2.5 DEVICE MEMORY MAPS

The memory maps for PIC16LF1554/1559 are as shown in Table 3-3 through Table 3-7.