Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC16(L)F1574/5/8/9

14/20-Pin MCUs with High-Precision 16-Bit PWMs

Description

PIC16(L)F1574/5/8/9 microcontrollers combine the capabilities of 16-bit PWMs with Analog to suit a variety of applications. These devices deliver four 16-bit PWMs with independent timers for applications where high resolution is needed, such as LED lighting, stepper motors, power supplies and other general purpose applications. The core independent peripherals (16-bit PWMs, Complementary Waveform Generator), Enhanced Universal Synchronous Asynchronous Receiver Transceiver (EUSART) and Analog (ADCs, Comparator and DAC) enable closed-loop feedback and communication for use in multiple market segments. The Peripheral Pin Select (PPS) functionality allows for I/O pin remapping of the digital peripherals for increased flexibility. The EUSART peripheral enables the communication for applications such as LIN.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Two 8-Bit Timers
- One 16-Bit Timer
- Four additional 16-Bit Timers available using the 16-Bit PWMs
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

Memory

- Up to 14 KB Flash Program Memory
- Up to 1024 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes
- High-Endurance Flash Data Memory (HEF)
  - 128 bytes if nonvolatile data storage
  - 100k erase/write cycles

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1574/5/8/9)
  - 2.3V to 5.5V (PIC16F1574/5/8/9)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C
- Internal Voltage Reference module
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

eXtreme Low-Power (XLP) Features:

- Sleep mode: 20 nA @ 1.8V, typical
- Watchdog Timer: 260 nA @ 1.8V, typical
- Operating Current:
  - 30 µA/MHz @ 1.8V, typical

Digital Peripherals

- 16-Bit PWM:
  - Four 16-bit PWMs with independent timers
  - Multiple output modes (standard, center-aligned, set and toggle on register match)
  - User settings for phase, duty cycle, period, offset and polarity
  - 16-bit timer capability
  - Interrupts generated based on timer matches with offset, duty cycle, period and phase registers
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Multiple signal sources
- Enhanced Universal Synchronous Asynchronous Receiver Transceiver (EUSART):
  - Supports LIN applications
- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals

Device I/O Port Features

- Up to 18 I/Os
- Individually Selectable Weak Pull-ups
- Interrupt-on-Change Pins Option with Edge-Selectable Option

Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 12 external channels
  - Conversion available during Sleep
- Two Comparators:
  - Low-Power/High-Speed modes
  - Fixed Voltage Reference at (non)inverting input(s)
  - Comparator outputs externally accessible
  - Synchronization with Timer1 clock source
  - Software hysteresis enable
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Clocking Structure

- Precision Internal Oscillator:
  - Factory calibrated ±1%, typical
  - Software-selectable clock speeds from 31 kHz to 32 MHz
- External Oscillator Block with:
  - Two external clock modes up to 32 MHz
- Digital Oscillator Input Available

TABLE 1: PIC12(L)F1571/2 AND PIC16(L)F1574/5/8/9 FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (Kwords)	Program Flash Memory (Kbytes)	Data SRAM (bytes)	I/O Pins	8-Bit/16-Bit Timers	Comparators	16-Bit PWM	10-Bit ADC (ch)	5-Bit DAC	CWG	EUSART	PPS	Debug(1)
PIC12(L)F1571	(A)	1	1.75	128	6	2/4(2)	1	3	4	1	1	0	N	I
PIC12(L)F1572	(A)	2	3.5	256	6	2/4(2)	1	3	4	1	1	1	N	I
PIC16(L)F1574	(B)	4	7	512	12	2/5(3)	2	4	8	1	1	1	Y	I
PIC16(L)F1575	(B)	8	14	1024	12	2/5(3)	2	4	8	1	1	1	Y	I
PIC16(L)F1578	(B)	4	7	512	18	2/5(3)	2	4	12	1	1	1	Y	I
PIC16(L)F1579	(B)	8	14	1024	18	2/5(3)	2	4	12	1	1	1	Y	I

Note 1: I – Debugging integrated on chip.

2: Three additional 16-bit timers available when not using the 16-bit PWM outputs.

3: Four additional 16-bit timers available when not using the 16-bit PWM outputs.

Data Sheet Index:

A) DS-40001723 PIC12(L)F1571/2 Data Sheet, 8-Pin Flash, 8-bit MCU with High-Precision 16-bit PWM

B) Future Release PIC16(L)F1574/5/8/9 Data Sheet, 8-Pin Flash, 8-bit MCU with High-Precision 16-bit PWM

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

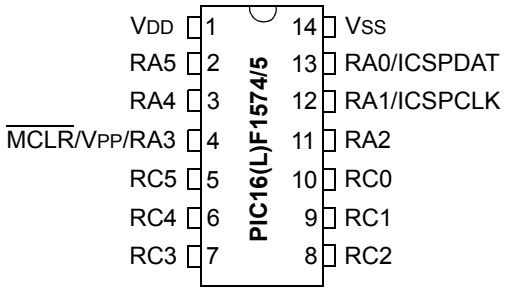
TABLE 2: PACKAGES

Packages	PDIP	SOIC	TSSOP	SSOP	UQFN
PIC16(L)F1574	●	●	●		●
PIC16(L)F1575	●	●	●		●
PIC16(L)F1578	●	●		●	●
PIC16(L)F1579	●	●		●	●

Note: Pin details are subject to change.

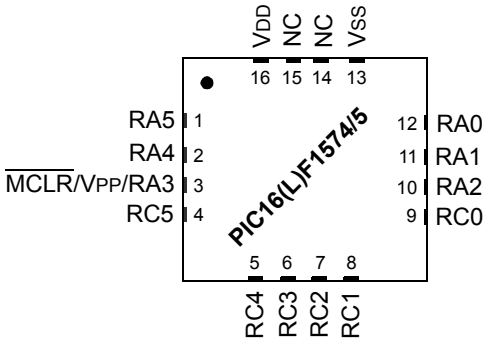
PIN DIAGRAMS

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP



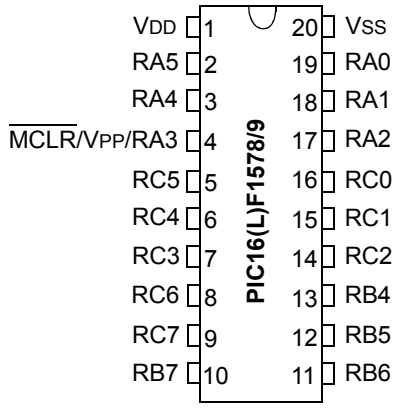
Note: See Table 3 for the pin allocation table.

FIGURE 2: 16-PIN UQFN (4x4)



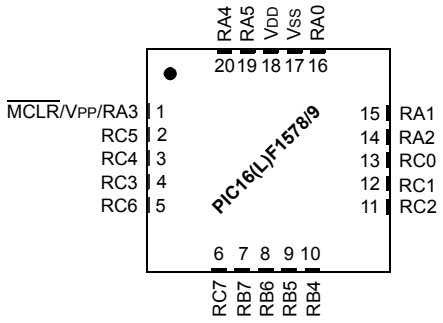
Note: See Table 3 for the pin allocation table.

FIGURE 3: 20-PIN PDIP, SOIC, SSOP



Note: See Table 4 for the pin allocation table.

FIGURE 4: 20-PIN UQFN (4x4)



Note: See Table 4 for the pin allocation table.

PIN ALLOCATION TABLES

TABLE 3: 14/16-PIN ALLOCATION TABLE (PIC16(L)F1574/5)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	Timers	PWM	EUSART	CWG	Interrupt	Pull-up	Basic
RA0	13	12	AN0	DAC1OUT1	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0-/C2IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	11	10	AN2	—	—	T0CKI(1)	—	—	CWG1IN(1)	INT(1)/IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$/VPP
RA4	3	2	AN3	—	—	T1G(1)	—	—	—	IOC	Y	CLKOUT
RA5	2	1	—	—	—	T1CKI(1)	—	—	—	IOC	Y	CLKIN
RC0	10	9	AN4	—	C2IN+	—	—	—	—	IOC	Y	—
RC1	9	8	AN5	—	C1IN1-/C2IN1-	—	—	—	—	IOC	Y	—
RC2	8	7	AN6	—	C1IN2-/C2IN2-	—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	C1IN3-/C2IN3-	—	—	—	—	IOC	Y	—
RC4	6	5	ADCACT(1)	—	—	—	—	CK(1)	—	IOC	Y	—
RC5	5	4	—	—	—	—	—	RX(1,3)	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	VDD
Vss	14	13	—	—	—	—	—	—	—	—	—	Vss
OUT(2)	—	—	—	—	C1OUT	—	PWM1OUT	DT(3)	CWG1A	—	—	—
	—	—	—	—	C2OUT	—	PWM2OUT	CK	CWG1B	—	—	—
	—	—	—	—	—	—	PWM3OUT	TX	—	—	—	—
	—	—	—	—	—	—	PWM4OUT	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS Output Selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1578/9)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	Timers	PWM	EUSART	CWG	Interrupt	Pull-up	Basic
RA0	19	16	AN0	DAC1OUT1	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	15	AN1	VREF+	C1IN0-/C2IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	14	AN2	—	—	T0CKI(1)	—	—	CWG1IN(1)	INT(1)/IOC	Y	—
RA3	4	1	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$/VPP
RA4	3	20	AN3	—	—	T1G(1)	—	—	—	IOC	Y	CLKOUT
RA5	2	19	—	—	—	T1CKI(1)	—	—	—	IOC	Y	CLKIN
RB4	13	10	AN10	—	—	—	—	—	—	IOC	Y	—
RB5	12	9	AN11	—	—	—	—	RX(1,3)	—	IOC	Y	—
RB6	11	8	—	—	—	—	—	—	—	IOC	Y	—
RB7	10	7	—	—	—	—	—	CK(1)	—	IOC	Y	—
RC0	16	13	AN4	—	C2IN+	—	—	—	—	IOC	Y	—
RC1	15	12	AN5	—	C1IN1-/C2IN1-	—	—	—	—	IOC	Y	—
RC2	14	11	AN6	—	C1IN2-/C2IN2-	—	—	—	—	IOC	Y	—
RC3	7	4	AN7	—	C1IN3-/C2IN3-	—	—	—	—	IOC	Y	—
RC4	6	3	ADCACT(1)	—	—	—	—	—	—	IOC	Y	—
RC5	5	2	—	—	—	—	—	—	—	IOC	Y	—
RC6	8	5	AN8	—	—	—	—	—	—	IOC	Y	—
RC7	9	6	AN9	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	VDD
Vss	20	17	—	—	—	—	—	—	—	—	—	Vss
OUT(2)	—	—	—	—	C1OUT	—	PWM1OUT	DT(3)	CWG1A	—	—	—
	—	—	—	—	C2OUT	—	PWM2OUT	CK	CWG1B	—	—	—
	—	—	—	—	—	—	PWM3OUT	TX	—	—	—	—
	—	—	—	—	—	—	PWM4OUT	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS Output Selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE OF CONTENTS

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Website at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Website; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our website at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

The PIC16(L)F1574/5/8/9 are described within this data sheet. The block diagram of these devices are shown in Figure 1-1, the available peripherals are shown in Table 1-1, and the pinout descriptions are shown in Table 1-2 and Table 1-3.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1574	PIC16(L)F1575	PIC16(L)F1578	PIC16(L)F1579
Analog-to-Digital Converter (ADC)		●	●	●	●
Complementary Wave Generator (CWG)		●	●	●	●
Digital-to-Analog Converter (DAC)		●	●	●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)		●	●	●	●
Fixed Voltage Reference (FVR)		●	●	●	●
Temperature Indicator		●	●	●	●
Comparators					
	C1	●	●	●	●
	C2	●	●	●	●
PWM Modules					
	PWM1	●	●	●	●
	PWM2	●	●	●	●
	PWM3	●	●	●	●
	PWM4	●	●	●	●
Timers					
	Timer0	●	●	●	●
	Timer1	●	●	●	●
	Timer2	●	●	●	●

1.1 Register and Bit Naming Conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

Example 2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt, and Mirror Bits

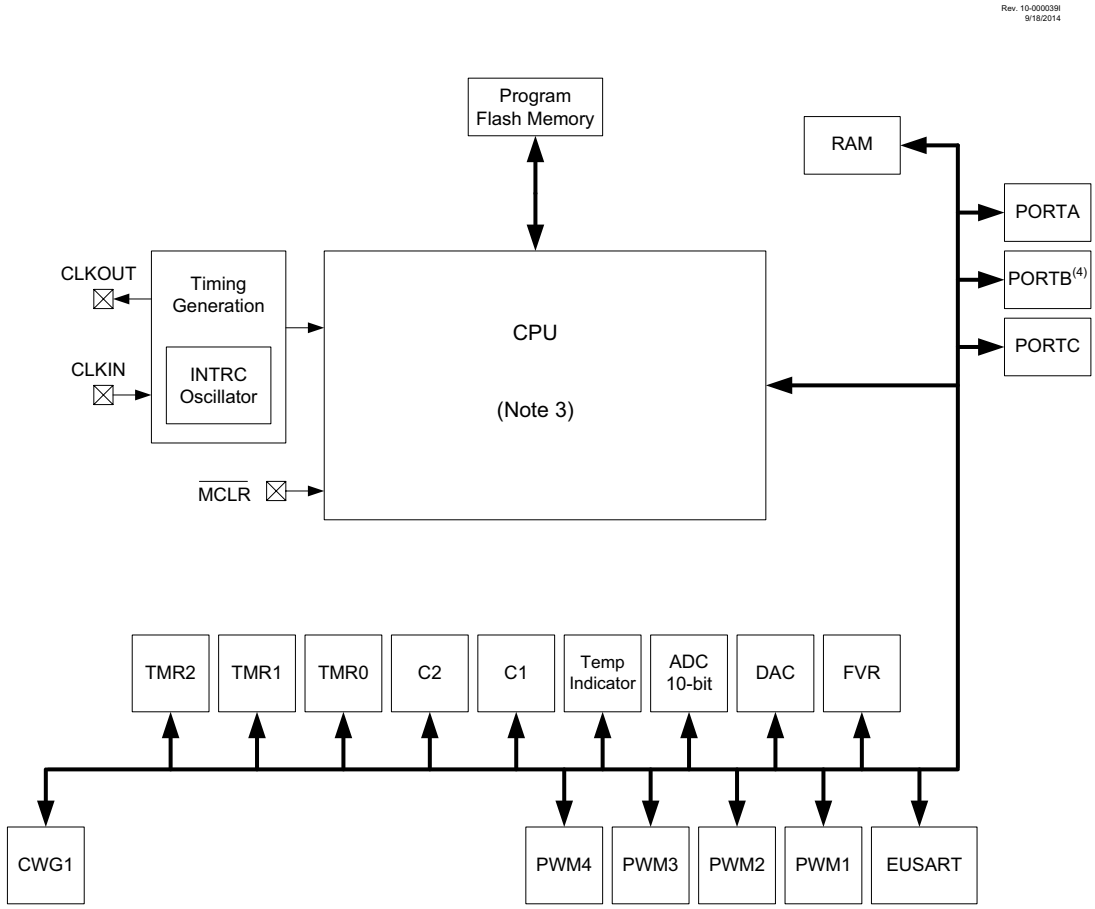
Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

- EUSART
- MSSP

FIGURE 1-1: PIC16(L)F1574/5/8/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.
2: See Table 1-1 for peripherals available on specific devices.
3: See Figure 2-1.
4: PIC16(L)F1578/9 only.

TABLE 1-2: PIC16(L)F1574/5 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/DAC1OUT1/ ICSPDAT	RA0	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN0	AN	—	ADC Channel input.
	C1IN+	AN	—	Comparator positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RA1/AN1/VREF+/C1IN0-/C2IN0-/ ICSPCLK	RA1	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN1	AN	—	ADC Channel input.
	VREF+	AN	—	Voltage Reference input.
	C1IN0-	AN	—	Comparator negative input.
	C2IN0-	AN	—	Comparator negative input.
	ICSPCLK	ST	—	ICSP Programming Clock.
RA2/AN2/T0CKI(1)/CWG1IN(1)/ INT(1)	RA2	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN2	AN	—	ADC Channel input.
	T0CKI	TTL/ST	—	Timer0 clock input.
	CWG1IN	TTL/ST	—	CWG complementary input.
	INT	TTL/ST	—	External interrupt.
RA3/VPP/$\overline{\text{MCLR}}$	RA3	TTL/ST	—	General purpose input with IOC and WPU.
	VPP	HV	—	Programming voltage.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
RA4/AN3/T1G(1)/CLKOUT	RA4	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN3	AN	—	ADC Channel input.
	T1G	TTL/ST	—	Timer1 Gate input.
	CLKOUT	CMOS/OD	CMOS	FOSC/4 output.
RA5/CLKIN/T1CKI(1)	RA5	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	CLKIN	CMOS	—	External clock input (EC mode).
	T1CKI	TTL/ST	—	Timer1 clock input.
RC0/AN4/C2IN+	RC0	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN4	AN	—	ADC Channel input.
	C2IN+	AN	—	Comparator positive input.
RC1/AN5/C1IN1-/C2IN1-	RC1	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN5	AN	—	ADC Channel input.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
RC2/AN6/C1IN2-/C2IN2-	RC2	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN6	AN	—	ADC Channel input.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
RC3/AN7/C1IN3-/C2IN3-	RC3	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN7	AN	—	ADC Channel input.
	C1IN3-	AN	—	Comparator negative input.
	C2IN3-	AN	—	Comparator negative input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-1.

3: These USART functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1574/5 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/ADCACT(1)/CK(1)	RC4	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	ADCACT	TTL/ST	—	ADC Auto-conversion Trigger input.
	CK	ST	CMOS	USART synchronous clock.
RC5/RX(1,3)	RC5	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	RX	ST	—	USART asynchronous input.
OUT(2)	C1OUT	—	CMOS	Comparator output.
	C2OUT	—	CMOS	Comparator output.
	PWM1OUT	—	CMOS	PWM1 output.
	PWM2OUT	—	CMOS	PWM2 output.
	PWM3OUT	—	CMOS	PWM3 output.
	PWM4OUT	—	CMOS	PWM4 output.
	CWG1A	—	CMOS	Complementary Output Generator Output A.
	CWG1B	—	CMOS	Complementary Output Generator Output B.
	TX/CK	—	CMOS	USART asynchronous TX data/synchronous clock output.
	DT(3)	—	CMOS	USART synchronous data output.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-1.

3: These USART functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1578/9 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/DAC1OUT/ ICSPDAT	RA0	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN0	AN	—	ADC Channel input.
	C1IN+	AN	—	Comparator positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RA1/AN1/VREF+/C1IN0-/C2IN0-/ ICSPCLK	RA1	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN1	AN	—	ADC Channel input.
	VREF+	AN	—	Voltage Reference input.
	C1IN0-	AN	—	Comparator negative input.
	C2IN0-	AN	—	Comparator negative input.
	ICSPCLK	ST	—	ICSP Programming Clock.
RA2/AN2/T0CKI(1)/CWG1IN(1)/ INT(1)	RA2	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN2	AN	—	ADC Channel input.
	T0CKI	TTL/ST	—	Timer0 clock input.
	CWG1IN	TTL/ST	—	CWG complementary input.
	INT	TTL/ST	—	External interrupt.
RA3/VPP/$\overline{\text{MCLR}}$	RA3	TTL/ST	—	General purpose input with IOC and WPU.
	VPP	HV	—	Programming voltage.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
RA4/AN3/T1G(1)/CLKOUT	RA4	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN3	AN	—	ADC Channel input.
	T1G	TTL/ST	—	Timer1 Gate input.
	CLKOUT	—	CMOS	FOSC/4 output.
RA5/CLKIN/T1CKI(1)	RA5	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	CLKIN	CMOS	—	External clock input (EC mode).
	T1CKI	TTL/ST	—	Timer1 clock input.
RB4/AN10	RB4	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN10	AN	—	ADC Channel input.
RB5/AN11/RX(1)	RB5	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN11	AN	—	ADC Channel input.
	RX	ST	—	USART asynchronous input.
RB6	RB6	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
RB7/CK	RB7	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	CK	ST	CMOS	USART synchronous clock.
RC0/AN4/C2IN+	RC0	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN4	AN	—	ADC Channel input.
	C2IN+	AN	—	Comparator positive input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-1.

3: These USART functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1578/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC1/AN5/C1IN1-/C2IN1-	RC1	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN5	AN	—	ADC Channel input.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
RC2/AN6/C1IN2-/C2IN2-	RC2	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN6	AN	—	ADC Channel input.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
RC3/AN7/C1IN3-/C2IN3-	RC3	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN7	AN	—	ADC Channel input.
	C1IN3-	AN	—	Comparator negative input.
	C2IN3-	AN	—	Comparator negative input.
RC4/ADCACT(1)	RC4	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	ADCACT	TTL/ST	—	ADC Auto-conversion Trigger input.
RC5	RC5	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
OUT(2)	C1OUT	—	CMOS	Comparator output.
	C2OUT	—	CMOS	Comparator output.
	PWM1OUT	—	CMOS	PWM1 output.
	PWM2OUT	—	CMOS	PWM2 output.
	PWM3OUT	—	CMOS	PWM3 output.
	PWM4OUT	—	CMOS	PWM4 output.
	CWG1A	—	CMOS	Complementary Output Generator Output A.
	CWG1B	—	CMOS	Complementary Output Generator Output B.
	TX/CK	—	CMOS	USART asynchronous TX data/synchronous clock output.
	DT(3)	—	CMOS	USART synchronous data output.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-1.

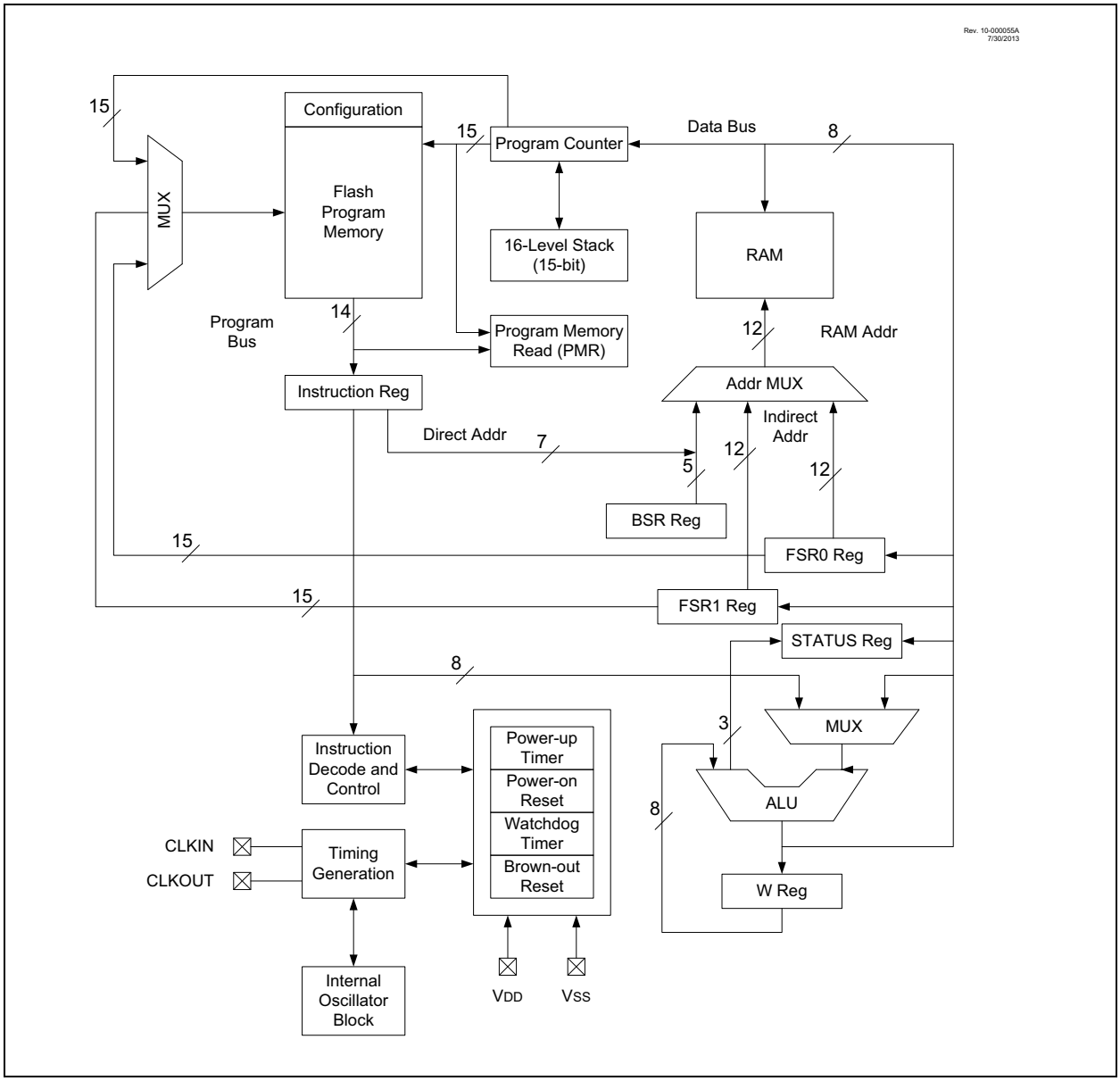
3: These USART functions are bidirectional. The output pin selections must be the same as the input pin selections.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See section **Section 3.5 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.6 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 26.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (See Figure 3-1).

3.2 High-Endurance Flash

This device has a 128-byte section of high-endurance Program Flash Memory (PFM) in lieu of data EEPROM. This area is especially well suited for nonvolatile data storage that is expected to be updated frequently over the life of the end product. See **Section 10.2 "Flash Program Memory Overview"** for more information on writing data to PFM. See **Section 3.3.2 "Special Function Register"** for more information about using the SFR registers to read byte data stored in PFM.

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range (1)
PIC16(L)F1574/8	4,096	0FFFh	0F80h-0FFFh
PIC16(L)F1575/9	8,192	1FFFh	1F80h-1FFFh

Note 1: High-endurance Flash applies to the low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1574/8

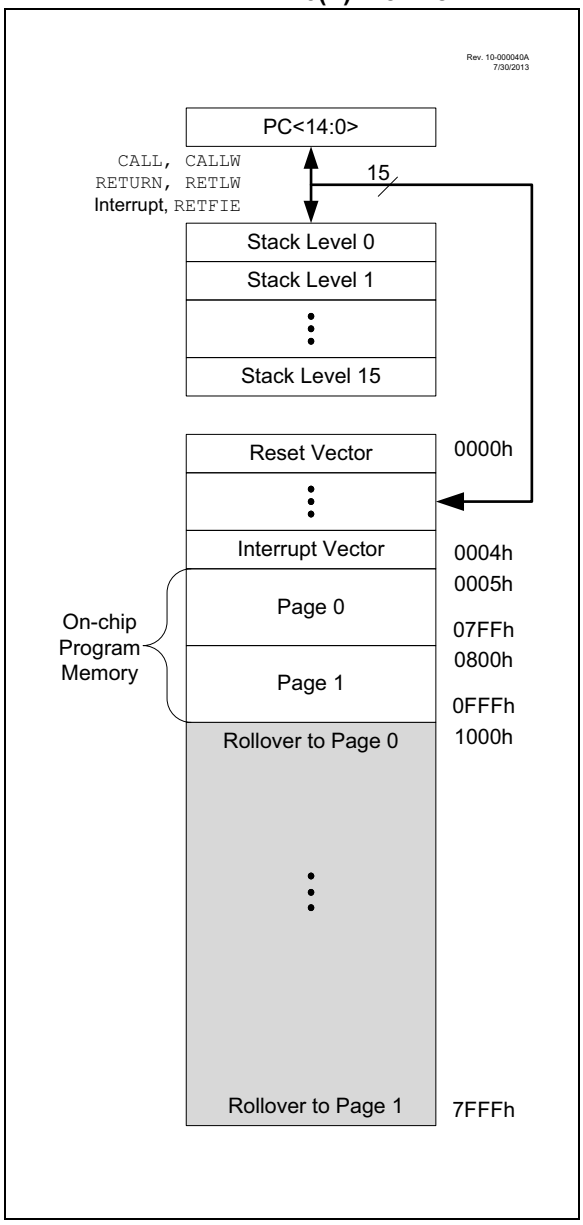
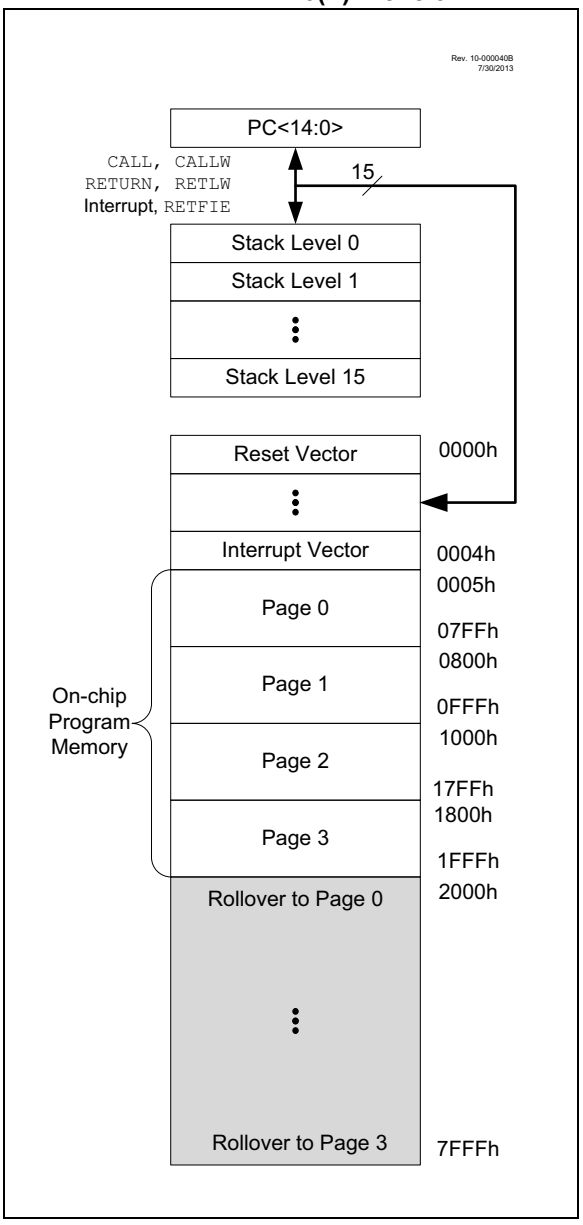


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1575/9



3.2.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.2.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.2.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH operator will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
  DW      DATA0         ;First constant
  DW      DATA1         ;Second constant
  DW      DATA2
  DW      DATA3
my_function
  ;… LOTS OF CODE…
  MOVLW   DATA_INDEX
  ADDLW   LOW constants
  MOVWF   FSR1L
  MOVLW   HIGH constants;MSb is set
                          automatically
  MOVWF   FSR1H
  BTFSC   STATUS,C      ;carry from ADDLW?
  INCF    FSR1H,f       ;yes
  MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.3 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.6 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper five bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

3.3.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-14.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.3.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 26.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

3.3.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.3.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

3.3.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.6.2 "Linear Data Memory"** for more information.

3.3.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

3.3.5 DEVICE MEMORY MAPS

The memory maps are as shown in Table 3-3 through Table 3-13.

FIGURE 3-3: BANKED MEMORY PARTITIONING

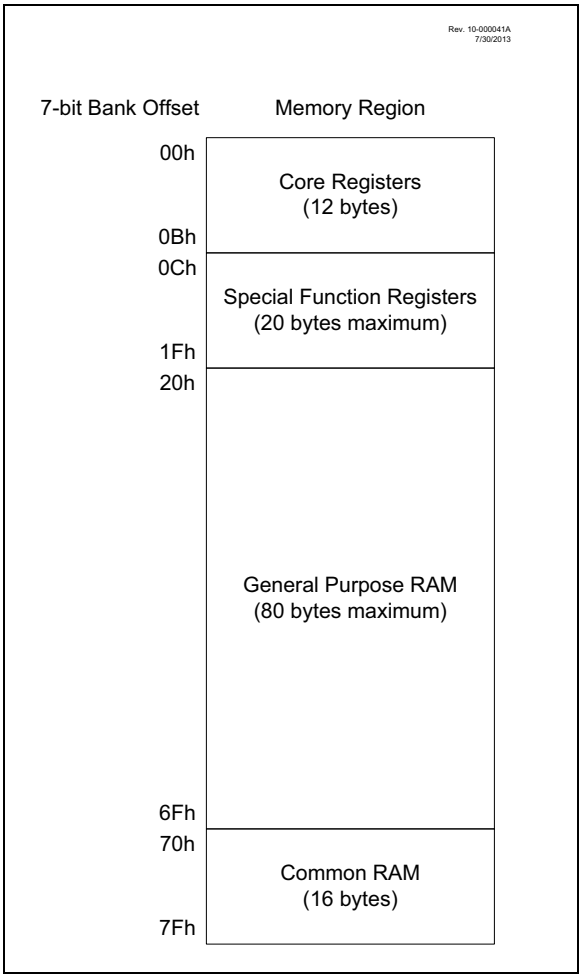


TABLE 3-3: PIC16(L)F1574 MEMORY MAP, BANKS 0-7

	BANK0	BANK1	BANK2	BANK3	BANK4	BANK5	BANK6	BANK7
000h	Core Registers (Table 3-2)	080h Core Registers (Table 3-2)	100h Core Registers (Table 3-2)	180h Core Registers (Table 3-2)	200h Core Registers (Table 3-2)	280h Core Registers (Table 3-2)	300h Core Registers (Table 3-2)	380h Core Registers (Table 3-2)
00Bh		08Bh	10Bh	18Bh	20Bh	28Bh	30Bh	38Bh
00Ch	PORTA	08Ch TRISA	10Ch LATA	18Ch ANSELA	20Ch WPUA	28Ch ODCONA	30Ch SLRCONA	38Ch INLVLA
00Dh	—	08Dh —	10Dh —	18Dh —	20Dh —	28Dh —	30Dh —	38Dh —
00Eh	PORTC	08Eh TRISC	10Eh LATC	18Eh ANSELC	20Eh WPUC	28Eh ODCONC	30Eh SLRCONC	38Eh INLVLC
00Fh	—	08Fh —	10Fh —	18Fh —	20Fh —	28Fh —	30Fh —	38Fh —
010h	—	090h —	110h —	190h —	210h —	290h —	310h —	390h —
011h	PIR1	091h PIE1	111h CM1CON0	191h PMADRL	211h —	291h —	311h —	391h IOCAP
012h	PIR2	092h PIE2	112h CM1CON1	192h PMADRH	212h —	292h —	312h —	392h IOCAN
013h	PIR3	093h PIE3	113h CM2CON0	193h PMDATL	213h —	293h —	313h —	393h IOCAF
014h	—	094h —	114h CM2CON1	194h PMDATH	214h —	294h —	314h —	394h —
015h	TMR0	095h OPTION_REG	115h CMOUT	195h PMCON1	215h —	295h —	315h —	395h —
016h	TMR1L	096h PCON	116h BORCON	196h PMCON2	216h —	296h —	316h —	396h —
017h	TMR1H	097h WDTCON	117h FVRCON	197h VREGCON(1)	217h —	297h —	317h —	397h IOCCP
018h	T1CON	098h OSCTUNE	118h DACCON0	198h —	218h —	298h —	318h —	398h IOCCN
019h	T1GCON	099h OSCCON	119h DACCON1	199h RCREG	219h —	299h —	319h —	399h IOCCF
01Ah	TMR2	09Ah OSCSTAT	11Ah —	19Ah TXREG	21Ah —	29Ah —	31Ah —	39Ah —
01Bh	PR2	09Bh ADRESL	11Bh —	19Bh SPBRGL	21Bh —	29Bh —	31Bh —	39Bh —
01Ch	T2CON	09Ch ADRESH	11Ch —	19Ch SPBRGH	21Ch —	29Ch —	31Ch —	39Ch —
01Dh	—	09Dh ADCON0	11Dh —	19Dh RCSTA	21Dh —	29Dh —	31Dh —	39Dh —
01Eh	—	09Eh ADCON1	11Eh —	19Eh TXSTA	21Eh —	29Eh —	31Eh —	39Eh —
01Fh	—	09Fh ADCON2	11Fh —	19Fh BAUDCON	21Fh —	29Fh —	31Fh —	39Fh —
020h	General Purpose Register 80 Bytes	0A0h General Purpose Register 80 Bytes	120h General Purpose Register 80 Bytes	1A0h General Purpose Register 80 Bytes	220h General Purpose Register 80 Bytes	2A0h General Purpose Register 80 Bytes	320h General Purpose Register 16 Bytes	3A0h Unimplemented Read as '0'
06Fh		0EFh	16Fh	1EFh	26Fh	2EFh	32Fh	3EFh
070h	Common RAM	0F0h Accesses 70h – 7Fh	170h Accesses 70h – 7Fh	1F0h Accesses 70h – 7Fh	270h Accesses 70h – 7Fh	2F0h Accesses 70h – 7Fh	330h Unimplemented Read as '0'	3F0h Accesses 70h – 7Fh
07Fh		0FFh	17Fh	1FFh	27Fh	2FFh	36Fh	3FFh
							370h Accesses 70h – 7Fh	
							37Fh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16LF1574.