Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC16(L)F1713/6

Cost Effective 8-Bit Intelligent Analog Flash Microcontrollers

Description:

PIC16(L)F1713/6 microcontrollers combine Intelligent Analog integration with low cost and extreme low power (XLP) to suit a variety of general purpose applications. These 28-pin devices deliver on-chip op amps, Core Independent Peripherals (CLC, NCO and COG), Peripheral Pin Select and Zero-Cross Detect, providing for increased design flexibility.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - 0-32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-bit Timers
- One 16-bit Timer
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

Memory:

- Up to 8 Kwords Flash Program Memory
- Up to 1024 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes
- High-Endurance Flash Data Memory (HEF)
  - 128 bytes if nonvolatile data storage
  - 100k erase/write cycles

Operating Characteristics:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1713/6)
  - 2.3V to 5.5V (PIC16F1713/6)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals:

- Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Complementary Output Generator (COG):
  - Rising/falling edge dead-band control/ blanking
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0Hz < FNCO < 32 MHz
  - Resolution: FNCO/220
- Capture/Compare/PWM (CCP) module
- PWM: Two 10-bit Pulse-Width Modulators
- Serial Communications:
  - SPI, I^2C, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, auto-wake-up on start
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Intelligent Analog Peripherals:

- Operational Amplifiers:
  - Two configurable rail-to-rail op amps
  - Selectable internal and external channels
  - 2 MHz gain bandwidth product
- High-Speed Comparators:
  - Up to two comparators
  - 50 ns response time
  - Rail-to-rail inputs
- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 28 external channels
  - Conversion available during Sleep
  - Temperature indicator
- Zero-Cross Detector (ZCD):
  - Detect when AC signal on pin crosses ground
- 8-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Internal Voltage Reference module

Clocking Structure:

- 16 MHz Internal Oscillator Block:
  - ±1% at calibration
  - Selectable frequency range from 0 to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Two external clock modes up to 20 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

Programming/Debug Features:

- In-Circuit Debug Integrated On-Chip
- Emulation Header for Advanced Debug:
  - Provides trace, background debug and up to 32 hardware break points
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

PIC16(L)F1713/6 Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash (bytes)	I/Os(2)	10-bit ADC (ch)	5/8-bit DAC	High-Speed/ Comparators	Op Amp	Zero Cross	Timers (8/16-bit)	CCP	PWM	COG	EUSART	MSSP (I^2C/SPI)	CLC	NCO	PPS	Debug(1)	XLP
PIC16(L)F1713	(1)	4096	512	128	25	17	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1716	(1)	8192	1024	128	25	17	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1717	(2)	8192	1024	128	36	28	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1718	(2)	16384	2048	128	25	17	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1719	(2)	16384	2048	128	36	28	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – using Debug Header; E – using Emulation Header.
2: One pin is input-only.

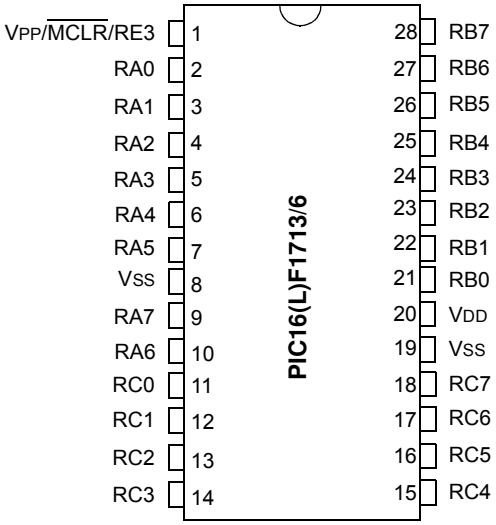
Data Sheet Index: (Unshaded devices are described in this document.)

1: DS40001726 PIC16(L)F1713/6 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.
2: DS40001740 PIC16(L)F1717/8/9 Data Sheet, 28/40-Pin Flash, 8-bit Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

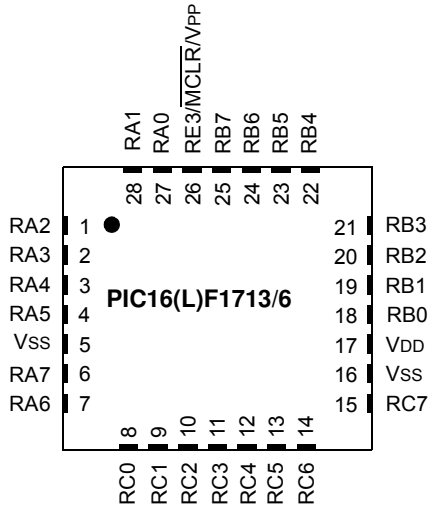
Pin Diagrams

FIGURE 1: 28-PIN PDIP, SOIC, SSOP



Note: See Table 1 for the pin allocation table.

FIGURE 2: 28-PIN (U)QFN



Note: See Table 1 for the pin allocation table.

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1713/6)

I/O[2]	PDIP, SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	NCO	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	2	27	AN0		C1IN0- C2IN0-											CLCIN0[1]	IOC	Y	
RA1	3	28	AN1		C1IN1- C2IN1-	OPA1OUT										CLCIN1[1]	IOC	Y	
RA2	4	1	AN2	Vref-	C1IN0+ C2IN0+		DAC1OUT1										IOC	Y	
RA3	5	2	AN3	Vref+	C1IN1+												IOC	Y	
RA4	6	3				OPA1IN+			T0CKI[1]								IOC	Y	
RA5	7	4	AN4			OPA1IN-	DAC2OUT1							nSS[1]			IOC	Y	
RA6	10	7															IOC	Y	OSC2 CLKOUT
RA7	9	6															IOC	Y	OSC1 CLKIN
RB0	21	18	AN12		C2IN1+			ZCD					COG1IN[1]				INT[1] IOC	Y	
RB1	22	19	AN10		C1IN3- C2IN3-	OPA2OUT											IOC	Y	
RB2	23	20	AN8			OPA2IN-											IOC	Y	
RB3	24	21	AN9		C1IN2- C2IN2-	OPA2IN+											IOC	Y	
RB4	25	22	AN11														IOC	Y	
RB5	26	23	AN13						T1G[3]								IOC	Y	
RB6	27	24														CLCIN2[1]	IOC	Y	ICSPCLK
RB7	28	25					DAC1OUT2 DAC2OUT2									CLCIN3[1]	IOC	Y	ICSPDAT
RC0	11	8							T1CKI[1], SOSCO								IOC	Y	
RC1	12	9							SOSCI	CCP2[1]							IOC	Y	
RC2	13	10	AN14							CCP1[1]							IOC	Y	
RC3	14	11	AN15											SCL/ SCK[1]			IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: Alternate outputs are excluded from solid shaded areas.

5: Alternate inputs are excluded from dot shaded areas.

I/O(2)	PDIP, SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator		Op Amp	DAC	Zero Cross	Timers			CCP		NCO	PWM		COG				MSSP			EUSART		CLC				Interrupt	Pull-up	Basic
RC4	15	12	AN16																			SDI(1)									IOC	Y	
																						SDA(1)											
RC5	16	13	AN17																												IOC	Y	
RC6	17	14	AN18																						CK(3)						IOC	Y	
RC7	18	15	AN19																						RX(3)						IOC	Y	
RE3	1	26																													IOC	Y	MCLR Vpp
Vdd	20	17																															Vdd
Vss	8	5																															Vss
	19	16																															
OUT(4)					C1OUT	C2OUT							CCP1	CCP2	NCO1OUT	PWM3OUT	PWM4OUT	COG1A	COG1B	COG1C	COG1D	SDA(3)	SCK/SCL(3)	SDO	TX/CK	DT(3)	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT			
IN(5)										T1G	T1CKI	T0CKI	CCP1	CCP2				COG1IN				SDI	SCK/SCL(3)	SS	RX(3)	CK	CLCIN0	CLCIN1	CLCIN2	CLCIN3	INT		

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: Alternate outputs are excluded from solid shaded areas.

5: Alternate inputs are excluded from dot shaded areas.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Website at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Website; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our website at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

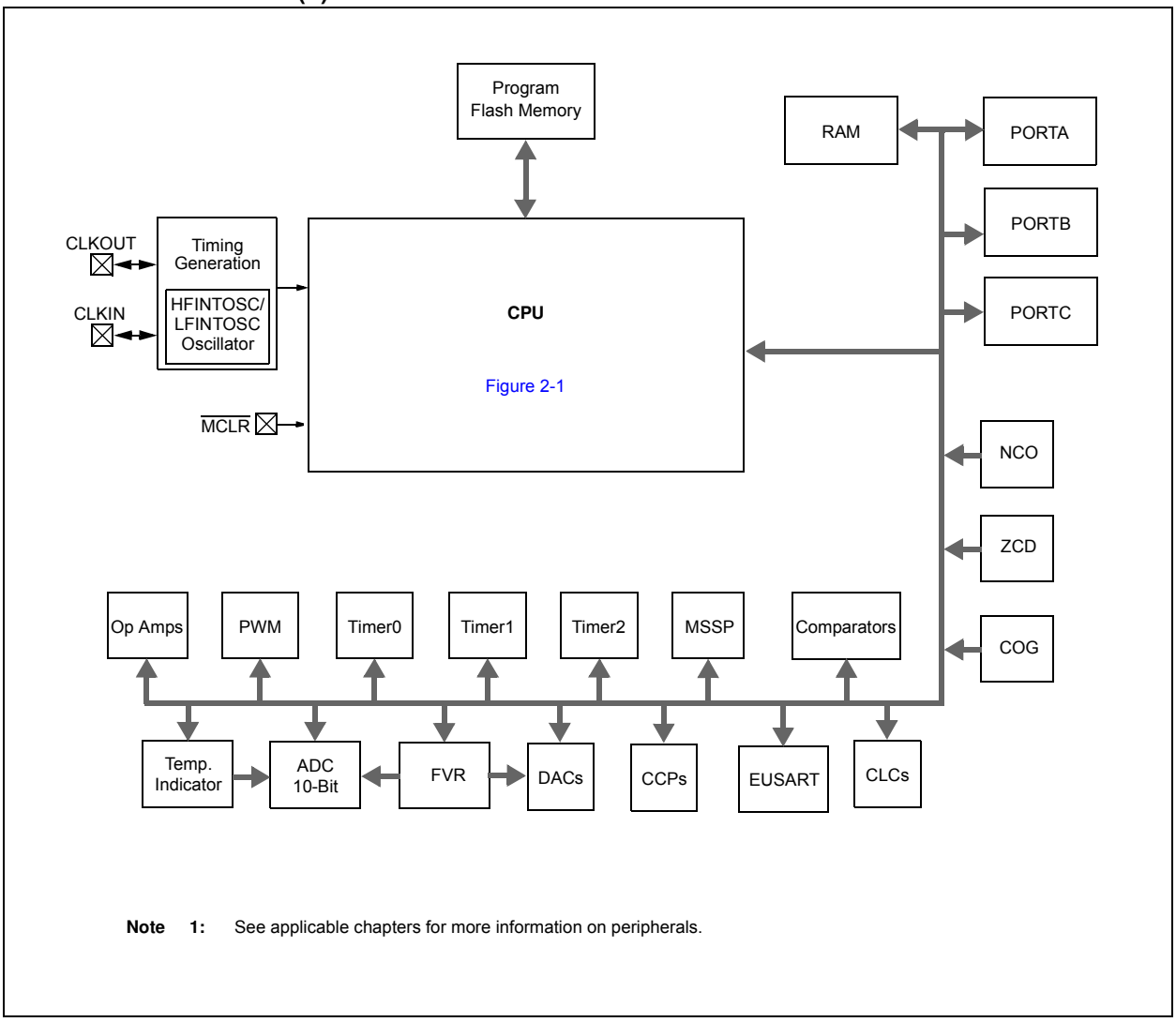
The PIC16(L)F1713/6 are described within this data sheet. They are available in 28-pin SPDIP, SSOP, SOIC, QFN, and UQFN packages. Figure 1-1 shows a block diagram of the PIC16(L)F1713/6 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1713	PIC16(L)F1716
Analog-to-Digital Converter (ADC)		•	•
Complementary Output Generator (COG)		•	•
Fixed Voltage Reference (FVR)		•	•
Zero-Cross Detection (ZCD)		•	•
Temperature Indicator		•	•
Numerically Controlled Oscillator (NCO)		•	•
Digital-to-Analog Converter (DAC)			
	DAC1	•	•
	DAC2	•	•
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	•	•
	CCP2	•	•
Comparators			
	C1	•	•
	C2	•	•
Configurable Logic Cell (CLC)			
	CLC1	•	•
	CLC2	•	•
	CLC3	•	•
	CLC4	•	•
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)			
	EUSART	•	•
Master Synchronous Serial Ports			
	MSSP	•	•
Op Amp			
	Op Amp 1	•	•
	Op Amp 2	•	•
Pulse Width Modulator (PWM)			
	PWM3	•	•
	PWM4	•	•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	•	•

FIGURE 1-1: PIC16(L)F1713/6 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1713/6 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/ CLCIN0(1)	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0-	AN	—	Comparator C2 negative input.
	C2IN0-	AN	—	Comparator C3 negative input.
	CLCIN0	TTL/ST	—	Configurable Logic Cell source input.
RA1/AN1/C1IN1-/C2IN1-/ OPA1OUT/CLCIN1(1)	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
	CLCIN1	TTL/ST	—	Configurable Logic Cell source input.
RA2/AN2/VREF-/C1IN0+/C2IN0+/ DAC1OUT1	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	VREF-	AN	—	ADC Negative Voltage Reference input.
	C1IN0+	AN	—	Comparator C2 positive input.
	C2IN0+	AN	—	Comparator C3 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
RA3/AN3/VREF+/C1IN1+	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC Voltage Reference input.
	C1IN1+	AN	—	Comparator C1 positive input.
RA4/OPA1IN+/T0CKI(1)	RA4	TTL/ST	CMOS	General purpose I/O.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	T0CKI	TTL/ST	—	Timer0 gate input.
RA5/AN4/OPA1IN-/DAC2OUT1/ $\overline{SS}$(1)	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	DAC2OUT1	—	AN	Digital-to-Analog Converter output.
	$\overline{SS}$	TTL/ST	—	Slave Select enable input.
RA6/OSC2/CLKOUT	RA6	TTL/ST	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA7/OSC1/CLKIN	RA7	TTL/ST	CMOS	General purpose I/O.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	TTL/ST	—	External clock input (EC mode).
RB0/AN12/C2IN1+/ZCD/ COGIN(1)	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	ZCD	AN	—	Zero-Cross Detection Current Source/Sink.
	COGIN	TTL/ST	—	Complementary Output Generator input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1713/6 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB1/AN10/C1IN3-/C2IN3-/ OPA2OUT	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
RB2/AN8/OPA2IN-	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
RB3/AN9/C1IN2-/C2IN2-/ OPA2IN+	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
RB4/AN11	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
RB5/AN13/T1G(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	T1G	TTL/ST	—	Timer1 gate input.
RB6/CLCIN2(1)/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	CLCIN2	TTL/ST	—	Configurable Logic Cell source input.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/DAC1OUT2/DAC2OUT2/ CLCIN3(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	DAC2OUT2	—	AN	Digital-to-Analog Converter output.
	CLCIN3	TTL/ST	—	Configurable Logic Cell source input.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1CKI(1)/SOSCO	RC0	TTL/ST	CMOS	General purpose I/O.
	T1CKI	TTL/ST	—	Timer1 clock input.
	SOSCO	XTAL	XTAL	Secondary Oscillator Connection.
RC1/SOSCI/CCP2(1)	RC1	TTL/ST	CMOS	General purpose I/O.
	SOSCI	XTAL	XTAL	Secondary Oscillator Connection.
	CCP2	TTL/ST	—	Capture input
RC2/AN14/CCP1(1)	RC2	TTL/ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	CCP1	TTL/ST	—	Capture input
RC3/AN15/SCL/SCK(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	AN15	AN	—	ADC Channel 15 input.
	SCL/SCK	I^2C	—	I^2C/SPI clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1713/6 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/AN16/SDI(1)/SDA(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	SDI	TTL/ST	—	SPI Data input
	SDA	I^2C	—	I^2C Data input
RC5/AN17	RC5	TTL/ST	CMOS	General purpose I/O.
	AN17	AN	—	ADC Channel 17 input.
RC6/AN18/CK(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	CK	TTL/ST		EUSART synchronous clock
RC7/AN19/RX(1)	RC7	TTL/ST	CMOS	General purpose I/O.
	AN18	AN	—	ADC Channel 18 input.
	RX	TTL/ST	—	EUSART receive
RE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master clear input
	VPP	HV	—	Programming enable
VDD	VDD	Power	—	Positive supply
VSS		Power	—	Ground reference
OUT(2)	C1OUT		CMOS	Comparator 1 output
	C2OUT		CMOS	Comparator 2 output
	CCP1		CMOS	Compare/PWM1 output
	CCP2		CMOS	Compare/PWM2 output
	NCO1OUT		CMOS	Numerically controlled oscillator output
	PWM3OUT		CMOS	PWM3 output
	PWM4OUT		CMOS	PWM4 output
	COGA		CMOS	Complementary output generator output A
	COGB		CMOS	Complementary output generator output B
	COGC		CMOS	Complementary output generator output C
	COGD		CMOS	Complementary output generator output D
	SDA(3)		OD	I^2C Data output
	SCK		CMOS	SPI clock output
	SCL(3)		OD	I^2C clock output
	SDO		CMOS	SPI data output
	TX/CK		CMOS	EUSART asynchronous TX data/synchronous clock out
	DT(3)		CMOS	EUSART synchronous data output
	CLC1OUT		CMOS	Configurable logic cell 1 output
	CLC2OUT		CMOS	Configurable logic cell 2 output
	CLC3OUT		CMOS	Configurable logic cell 3 output
	CLC4OUT		CMOS	Configurable logic cell 4 output

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

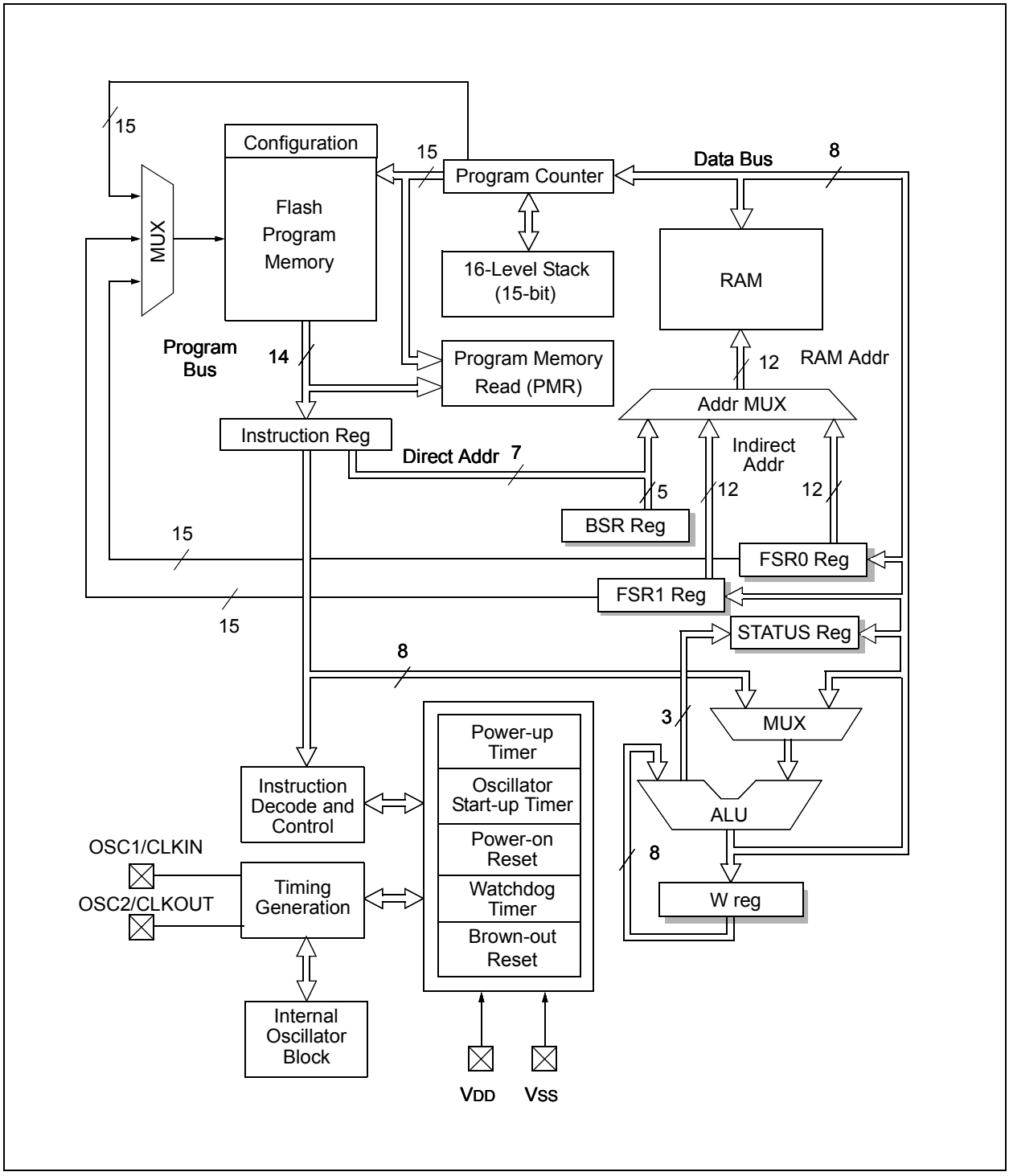
Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"** for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 3.6 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.7 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 33.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

Note 1: The method to access Flash memory through the PMCON registers is described in **Section 10.0 "Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 and Table 3-2 show the memory sizes implemented for the PIC16(L)F1713/6 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1).

3.2 High Endurance Flash

This device has a 128-byte section of high-endurance program Flash memory (PFM) in lieu of data EEPROM. This area is especially well suited for nonvolatile data storage that is expected to be updated frequently over the life of the end product. See **Section 10.2 "Flash Program Memory Overview"** for more information on writing data to PFM. See **Section 3.2.1.2 "Indirect Read with FSR"** for more information about using the FSR registers to read byte data stored in PFM.

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range(1)
PIC16(L)F1713	4,096	FFFh	F80h-FFFh
PIC16(L)F1716	16,384	3FFFh	3F80h-3FFFh

Note 1: High-endurance Flash applies to the low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1713

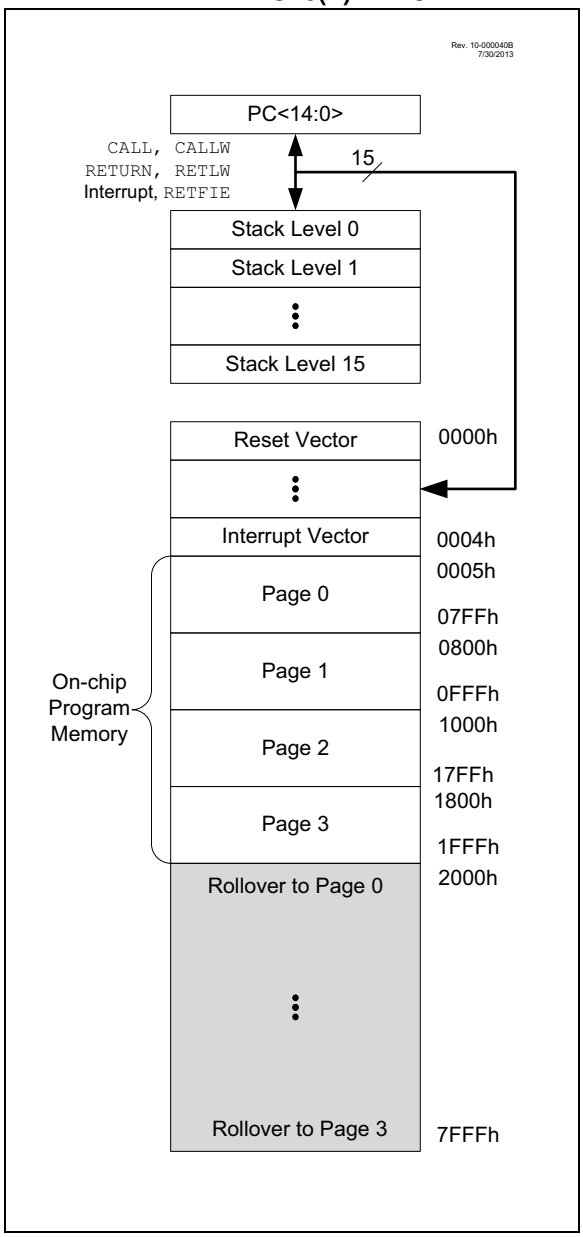
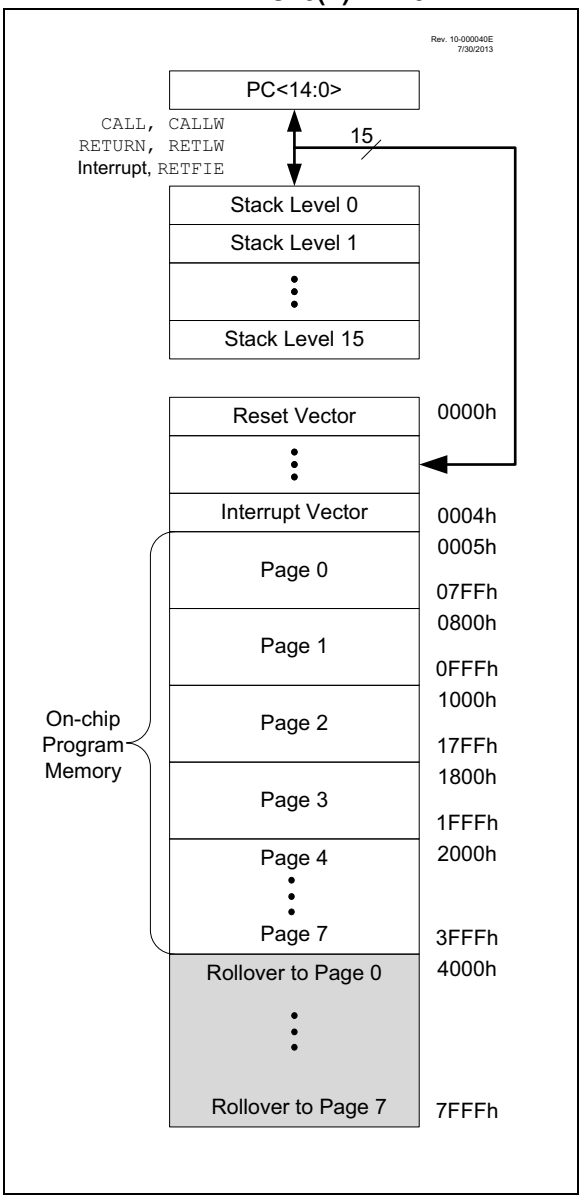


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1716



3.2.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.2.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.2.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The high directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
  DW DATA0              ;First constant
  DW DATA1              ;Second constant
  DW DATA2
  DW DATA3
my_function
  ;… LOTS OF CODE…
  MOVLW   DATA_INDEX
  ADDLW   LOW constants
  MOVWF   FSR1L
  MOVLW   HIGH constants;MSb sets
                         automatically
  MOVWF   FSR1H
  BTFSC   STATUS, C     ;carry from ADDLW?
  INCF    FSR1H, f      ;yes
  MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.3 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.7 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper five bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

3.3.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-10.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.3.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 33.0 "Instruction Set Summary"**).

Note:	The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

3.4 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT Time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

3.4.1 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.4.2 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

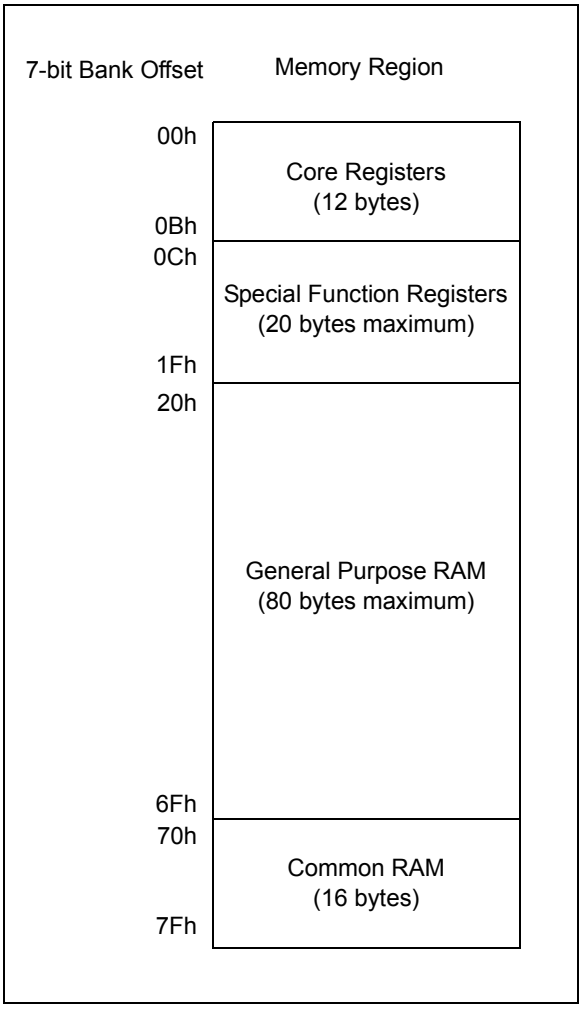
3.4.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.7.2 "Linear Data Memory"** for more information.

3.4.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.4.4 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Tables 3-3 through 3-9.

TABLE 3-3: PIC16(L)F1713 MEMORY MAP (BANKS 0-7)

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	—	190h	—	210h	WPUE	290h	—	310h	—	390h	INLVLE
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	PMADRL	211h	SSP1BUF	291h	CCPR1L	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	PMADRH	212h	SSP1ADD	292h	CCPR1H	312h	—	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	PMDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	—	094h	—	114h	CM2CON1	194h	PMDATH	214h	SSP1STAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	PMCON1	215h	SSP1CON1	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSP1CON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON(1)	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DAC1CON0	198h	—	218h	—	298h	CCPR2L	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DAC1CON1	199h	RC1REG	219h	—	299h	CCPR2H	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	DAC2CON0	19Ah	TX1REG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	DAC2CON1	19Bh	SP1BRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	ZCD1CON	19Ch	SP1BRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	—	19Dh	RC1STA	21Dh	—	29Dh	—	31Dh	—	39Dh	IOCEP
01Eh	—	09Eh	ADCON1	11Eh	—	19Eh	TX1STA	21Eh	—	29Eh	CCPTMRS	31Eh	—	39Eh	IOCEN
01Fh	—	09Fh	ADCON2	11Fh	—	19Fh	BAUD1CON	21Fh	—	29Fh	—	31Fh	—	39Fh	IOCEF
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 16 Bytes	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		32Fh		3EFh	
070h	Common RAM 70h – 7Fh	0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	330h	Unimplemented Read as '0'	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		36Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16(L)F1713/6.

TABLE 3-4: PIC16(L)F1716 MEMORY MAP (BANKS 0-7)

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	—	190h	—	210h	WPUE	290h	—	310h	—	390h	INLVLE
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	PMADRL	211h	SSP1BUF	291h	CCPR1L	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	PMADRH	212h	SSP1ADD	292h	CCPR1H	312h	—	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	PMDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	—	094h	—	114h	CM2CON1	194h	PMDATH	214h	SSP1STAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	PMCON1	215h	SSP1CON1	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSP1CON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON(1)	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DAC1CON0	198h	—	218h	—	298h	CCPR2L	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DAC1CON1	199h	RC1REG	219h	—	299h	CCPR2H	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	DAC2CON0	19Ah	TX1REG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	DAC2CON1	19Bh	SP1BRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	ZCD1CON	19Ch	SP1BRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	—	19Dh	RC1STA	21Dh	—	29Dh	—	31Dh	—	39Dh	IOCEP
01Eh	—	09Eh	ADCON1	11Eh	—	19Eh	TX1STA	21Eh	—	29Eh	CCPTMRS	31Eh	—	39Eh	IOCEN
01Fh	—	09Fh	ADCON2	11Fh	—	19Fh	BAUD1CON	21Fh	—	29Fh	—	31Fh	—	39Fh	IOCEF
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 80 Bytes	3A0h	General Purpose Register 80 Bytes
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h	Common RAM 70h – 7Fh	0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16(L)F1713/6.

TABLE 3-5: PIC16(L)F1713 MEMORY MAP, BANK 8-23

BANK 8	BANK 9	BANK 10	BANK 11	BANK 12	BANK 13	BANK 14	BANK 15
400h Core Registers (Table 3-2) 40Bh	480h Core Registers (Table 3-2) 48Bh	500h Core Registers (Table 3-2) 50Bh	580h Core Registers (Table 3-2) 58Bh	600h Core Registers (Table 3-2) 60Bh	680h Core Registers (Table 3-2) 68Bh	700h Core Registers (Table 3-2) 70Bh	780h Core Registers (Table 3-2) 78Bh
40Ch —	48Ch —	50Ch —	58Ch —	60Ch —	68Ch —	70Ch —	78Ch —
40Dh —	48Dh —	50Dh —	58Dh —	60Dh —	68Dh —	70Dh —	78Dh —
40Eh —	48Eh —	50Eh —	58Eh —	60Eh —	68Eh —	70Eh —	78Eh —
40Fh —	48Fh —	50Fh —	58Fh —	60Fh —	68Fh —	70Fh —	78Fh —
410h —	490h —	510h —	590h —	610h —	690h —	710h —	790h —
411h —	491h —	511h OPA1CON	591h —	611h —	691h COG1PHR	711h —	791h —
412h —	492h —	512h —	592h —	612h —	692h COG1PHF	712h —	792h —
413h —	493h —	513h —	593h —	613h —	693h COG1BLKR	713h —	793h —
414h —	494h —	514h —	594h —	614h —	694h COG1BLKF	714h —	794h —
415h TMR4	495h —	515h OPA2CON	595h —	615h —	695h COG1DBR	715h —	795h —
416h PR4	496h —	516h —	596h —	616h —	696h COG1DBF	716h —	796h —
417h T4CON	497h —	517h —	597h —	617h PWM3DCL	697h COG1CON0	717h —	797h —
418h —	498h NCO1ACCL	518h —	598h —	618h PWM3DCH	698h COG1CON1	718h —	798h —
419h —	499h NCO1ACCH	519h —	599h —	619h PWM3CON	699h COG1RIS	719h —	799h —
41Ah —	49Ah NCO1ACCU	51Ah —	59Ah —	61Ah PWM4DCL	69Ah COG1RSIM	71Ah —	79Ah —
41Bh —	49Bh NCO1INCL	51Bh —	59Bh —	61Bh PWM4DCH	69Bh COG1FIS	71Bh —	79Bh —
41Ch TMR6	49Ch NCO1INCH	51Ch —	59Ch —	61Ch PWM4CON	69Ch COG1FSIM	71Ch —	79Ch —
41Dh PR6	49Dh NCO1INCU	51Dh —	59Dh —	61Dh —	69Dh COG1ASD0	71Dh —	79Dh —
41Eh T6CON	49Eh NCO1CON	51Eh —	59Eh —	61Eh —	69Eh COG1ASD1	71Eh —	79Eh —
41Fh —	49Fh NCO1CLK	51Fh —	59Fh —	61Fh —	69Fh COG1STR	71Fh —	79Fh —
420h Unimplemented Read as '0' 46Fh	4A0h Unimplemented Read as '0' 4EFh	520h Unimplemented Read as '0' 56Fh	5A0h Unimplemented Read as '0' 5EFh	620h Unimplemented Read as '0' 66Fh	6A0h Unimplemented Read as '0' 6EFh	720h Unimplemented Read as '0' 76Fh	7A0h Unimplemented Read as '0' 7EFh
470h Accesses 70h – 7Fh 47Fh	4F0h Accesses 70h – 7Fh 4FFh	570h Accesses 70h – 7Fh 57Fh	5F0h Accesses 70h – 7Fh 5FFh	670h Accesses 70h – 7Fh 67Fh	6F0h Accesses 70h – 7Fh 6FFh	770h Accesses 70h – 7Fh 77Fh	7F0h Accesses 70h – 7Fh 7FFh

BANK 16	BANK 17	BANK 18	BANK 19	BANK 20	BANK 21	BANK 22	BANK 23
800h Core Registers (Table 3-2) 80Bh	880h Core Registers (Table 3-2) 88Bh	900h Core Registers (Table 3-2) 90Bh	980h Core Registers (Table 3-2) 98Bh	A00h Core Registers (Table 3-2) A0Bh	A80h Core Registers (Table 3-2) A8Bh	B00h Core Registers (Table 3-2) B0Bh	B80h Core Registers (Table 3-2) B8Bh
80Ch Unimplemented Read as '0' 86Fh	88Ch Unimplemented Read as '0' 8EFh	90Ch Unimplemented Read as '0' 96Fh	98Ch Unimplemented Read as '0' 9EFh	A0Ch Unimplemented Read as '0' A6Fh	A8Ch Unimplemented Read as '0' AEFh	B0Ch Unimplemented Read as '0' B6Fh	B8Ch Unimplemented Read as '0' BEFh
870h Accesses 70h – 7Fh 87Fh	8F0h Accesses 70h – 7Fh 8FFh	970h Accesses 70h – 7Fh 97Fh	9F0h Accesses 70h – 7Fh 9FFh	A70h Accesses 70h – 7Fh A7Fh	AF0h Accesses 70h – 7Fh AFFh	B70h Accesses 70h – 7Fh B7Fh	BF0h Accesses 70h – 7Fh BFFh

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-6: PIC16(L)F1716 MEMORY MAP, BANK 8-23

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	—	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	—	48Dh	—	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	—	490h	—	510h	—	590h	—	610h	—	690h	—	710h	—	790h	—
411h	—	491h	—	511h	OPA1CON	591h	—	611h	—	691h	COG1PHR	711h	—	791h	—
412h	—	492h	—	512h	—	592h	—	612h	—	692h	COG1PHF	712h	—	792h	—
413h	—	493h	—	513h	—	593h	—	613h	—	693h	COG1BLKR	713h	—	793h	—
414h	—	494h	—	514h	—	594h	—	614h	—	694h	COG1BLKF	714h	—	794h	—
415h	TMR4	495h	—	515h	OPA2CON	595h	—	615h	—	695h	COG1DBR	715h	—	795h	—
416h	PR4	496h	—	516h	—	596h	—	616h	—	696h	COG1DBF	716h	—	796h	—
417h	T4CON	497h	—	517h	—	597h	—	617h	PWM3DCL	697h	COG1CON0	717h	—	797h	—
418h	—	498h	NCO1ACCL	518h	—	598h	—	618h	PWM3DCH	698h	COG1CON1	718h	—	798h	—
419h	—	499h	NCO1ACCH	519h	—	599h	—	619h	PWM3CON	699h	COG1RIS	719h	—	799h	—
41Ah	—	49Ah	NCO1ACCU	51Ah	—	59Ah	—	61Ah	PWM4DCL	69Ah	COG1RSIM	71Ah	—	79Ah	—
41Bh	—	49Bh	NCO1INCL	51Bh	—	59Bh	—	61Bh	PWM4DCH	69Bh	COG1FIS	71Bh	—	79Bh	—
41Ch	TMR6	49Ch	NCO1INCH	51Ch	—	59Ch	—	61Ch	PWM4CON	69Ch	COG1FSIM	71Ch	—	79Ch	—
41Dh	PR6	49Dh	NCO1INCU	51Dh	—	59Dh	—	61Dh	—	69Dh	COG1ASD0	71Dh	—	79Dh	—
41Eh	T6CON	49Eh	NCO1CON	51Eh	—	59Eh	—	61Eh	—	69Eh	COG1ASD1	71Eh	—	79Eh	—
41Fh	—	49Fh	NCO1CLK	51Fh	—	59Fh	—	61Fh	—	69Fh	COG1STR	71Fh	—	79Fh	—
420h	General Purpose Register 80 Bytes	4A0h	General Purpose Register 80 Bytes	520h	General Purpose Register 80 Bytes	5A0h	General Purpose Register 80 Bytes	620h	General Purpose Register 48 Bytes	6A0h	Unimplemented Read as '0'	720h	Unimplemented Read as '0'	7A0h	Unimplemented Read as '0'
46Fh		4EFh		56Fh		5EFh		64Fh	Unimplemented Read as '0'	6EFh		76Fh		7EFh	
470h	Accesses 70h – 7Fh	4F0h	Accesses 70h – 7Fh	570h	Accesses 70h – 7Fh	5F0h	Accesses 70h – 7Fh	670h	Accesses 70h – 7Fh	6F0h	Accesses 70h – 7Fh	770h	Accesses 70h – 7Fh	7F0h	Accesses 70h – 7Fh
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	Unimplemented Read as '0'	88Ch	Unimplemented Read as '0'	90Ch	Unimplemented Read as '0'	98Ch	Unimplemented Read as '0'	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Accesses 70h – 7Fh	8F0h	Accesses 70h – 7Fh	970h	Accesses 70h – 7Fh	9F0h	Accesses 70h – 7Fh	A70h	Accesses 70h – 7Fh	AF0h	Accesses 70h – 7Fh	B70h	Accesses 70h – 7Fh	BF0h	Accesses 70h – 7Fh
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-7: PIC16(L)F1713/6 MEMORY MAP, BANK 24-31

BANK 24	BANK 25	BANK 26	BANK 27	BANK 28	BANK 29	BANK 30	BANK 31
C00h Core Registers (Table 3-2) C0Bh	C80h Core Registers (Table 3-2) C8Bh	D00h Core Registers (Table 3-2) D0Bh	D80h Core Registers (Table 3-2) D8Bh	E00h Core Registers (Table 3-2) E0Bh	E80h Core Registers (Table 3-2) E8Bh	F00h Core Registers (Table 3-2) F0Bh	F80h Core Registers (Table 3-2) F8Bh
C0Ch —	C8Ch —	D0Ch —	D8Ch —	E0Ch See Table 3-9 for register mapping details	E8Ch See Table 3-9 for register mapping details	F0Ch See Table 3-9 for register mapping details	F8Ch See Table 3-9 for register mapping details
C0Dh —	C8Dh —	D0Dh —	D8Dh —	E0Dh	E8Dh	F0Dh	F8Dh
C0Eh —	C8Eh —	D0Eh —	D8Eh —	E0Eh	E8Eh	F0Eh	F8Eh
C0Fh —	C8Fh —	D0Fh —	D8Fh —	E0Fh	E8Fh	F0Fh	F8Fh
C10h —	C90h —	D10h —	D90h —	E10h	E90h	F10h	F90h
C11h —	C91h —	D11h —	D91h —	E11h	E91h	F11h	F91h
C12h —	C92h —	D12h —	D92h —	E12h	E92h	F12h	F92h
C13h —	C93h —	D13h —	D93h —	E13h	E93h	F13h	F93h
C14h —	C94h —	D14h —	D94h —	E14h	E94h	F14h	F94h
C15h —	C95h —	D15h —	D95h —	E15h	E95h	F15h	F95h
C16h —	C96h —	D16h —	D96h —	E16h	E96h	F16h	F96h
C17h —	C97h —	D17h —	D97h —	E17h	E97h	F17h	F97h
C18h —	C98h —	D18h —	D98h —	E18h	E98h	F18h	F98h
C19h —	C99h —	D19h —	D99h —	E19h	E99h	F19h	F99h
C1Ah —	C9Ah —	D1Ah —	D9Ah —	E1Ah	E9Ah	F1Ah	F9Ah
C1Bh —	C9Bh —	D1Bh —	D9Bh —	E1Bh	E9Bh	F1Bh	F9Bh
C1Ch —	C9Ch —	D1Ch —	D9Ch —	E1Ch	E9Ch	F1Ch	F9Ch
C1Dh —	C9Dh —	D1Dh —	D9Dh —	E1Dh	E9Dh	F1Dh	F9Dh
C1Eh —	C9Eh —	D1Eh —	D9Eh —	E1Eh	E9Eh	F1Eh	F9Eh
C1Fh —	C9Fh —	D1Fh —	D9Fh —	E1Fh	E9Fh	F1Fh	F9Fh
C20h Unimplemented Read as '0' C6Fh	CA0h Unimplemented Read as '0' CEFh	D20h Unimplemented Read as '0' D6Fh	DA0h Unimplemented Read as '0' DEFh	E20h	EA0h	F20h	FA0h FEFh
C70h Accesses 70h – 7Fh CFFh	CF0h Accesses 70h – 7Fh CFFh	D70h Accesses 70h – 7Fh D7Fh	DF0h Accesses 70h – 7Fh DFFh	E70h Accesses 70h – 7Fh E7Fh	EF0h Accesses 70h – 7Fh EFFh	F70h Accesses 70h – 7Fh F7Fh	FF0h Accesses 70h – 7Fh FFFh

Legend: = Unimplemented data memory locations, read as '0'.