Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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PIC16(L)F1777/8/9

28/40/44-Pin, 8-Bit Flash Microcontroller

Description

PIC16(L)F1777/8/9 microcontrollers feature a high level of integration of intelligent analog and digital peripherals for a wide range of applications, such as lighting, power supplies, battery charging, motor control and other general purpose applications. These devices deliver multiple op amps, 5-/10-bit DACs, high-speed comparators, 10-bit ADC, 10-/16-bit PWMs, programmable ramp generator (PRG) and other peripherals that can be connected internally to create closed-loop systems without using pins or the printed circuit board (PCB) area. The 10-/16-bit PWMs, digital signal modulators and tri-state output op amp can be used together to create a LED dimming engine for lighting applications. The peripheral pin select (PPS) functionality provides flexibility, eases PCB layout and peripheral utilization by allowing digital peripheral pin mapping to an I/O.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Five 8-Bit Timers
- Three 16-Bit Timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (EWDT):
  - Low-power 31 kHz WDT
  - Software selectable prescaler
  - Software selectable enable

Memory

- Up to 28 Kbytes Program Flash Memory (PFM)
- Up to 2 Kbytes Data RAM
- Direct, Indirect and Relative Addressing modes
- High-Endurance Flash (HEF):
  - 128B of nonvolatile data storage
  - 100K Erase/Write cycles

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1777/8/9)
  - 2.3V to 5.5V (PIC16F1777/8/9)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 31 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Intelligent Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 28 external channels
  - Conversion available during Sleep
- Four Operational Amplifiers (OPA):
  - Selectable internal and external channels
  - Tri-state output
  - Part of LED dimming engine
  - Selectable internal and external channels
- Eight High-Speed Comparators (HS Comp):
  - Up to nine external inverting inputs
  - Up to 12 external non-inverting inputs
  - Fixed Voltage Reference at inverting and non-inverting input(s)
  - Comparator outputs externally accessible
- Digital-to-Analog Converters (DAC):
  - Four 10-bit resolution DACs
  - 10-bit resolution, rail-to-rail
  - Conversion during Sleep
  - Internal connections to ADCs and HS Comparators
- Voltage Reference:
  - Fixed Voltage Reference (FVR)
  - 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detector (ZCD):
  - Detect high-voltage AC signal
- Four Programmable Ramp Generators (PRG):
  - Slope compensation
  - Ramp generation
- High-Current Drive I/Os:
  - Up to 100 mA sink or source @ 5V

Digital Peripherals

- Four Configurable Logic Cells (CLC):
  - Integrated combinational and state logic
- Four Complementary Output Generators (COG):
  - Push-pull, Full-Bridge and Steering modes
- Four Capture/Compare/PWM (CCP) Modules
- Pulse-Width Modulator (PWM):
  - Four 16-bit PWMs
  - Independent timers
  - Multiple output modes (Edge-, Center-Aligned, set and toggle on register match)
  - User settings for phase, duty cycle, period, offset and polarity
  - 16-bit timer capability
  - Three 10-bit PWMs
- Digital Signal Modulator (DSM):
  - Modulates a carrier signal with a digital data to create custom carrier synchronized output waveforms
  - Part of LED dimming engine
- Peripheral Pin Select (PPS):
  - I/O remapping of digital peripherals
- Serial Communications:
  - Enhanced USART (EUSART)
  - SPI, I^2C, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, auto-wake-up on start
- Up to 25 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select

Clocking Structure

- Precision Internal Oscillator:
  - ±1% at calibration
  - Selectable frequency range 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 4x Phase-Locked Loop (PLL) for up to 32 MHz Internal Operation
- External Oscillator Block with Three External Clock modes up to 32 MHz

TABLE 1: PIC16(L)F1773/6/7/8/9 FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (bytes)	Program Flash Memory (word)	High Endurance Flash (B)	Data SRAM (Bytes)	I/O Pins(1)	8-Bit/16-Bit Timers	High-Speed Comparator	10-bit ADC (ch)	5/10-bit DAC	CCP	10-bit/16-bit PWM	COG	CLC	Op Amp	Zero Cross Detect	Programmable Ramp Gen	High-Current I/Os	Peripheral Pin Select	EUSART	I^2C/SPI	Debug(2)
PIC16(L)F1773	(A)	7K	4K	128	512	25	5/3	6	17	3/3	3	3/3	3	4	3	1	3	2	Y	1	1	I
PIC16(L)F1776	(A)	14K	8K	128	1K	25	5/3	6	17	3/3	3	3/3	3	4	3	1	3	2	Y	1	1	I
PIC16(L)F1777	(B)	14K	8K	128	1K	36	5/3	8	28	4/4	4	4/4	4	4	4	1	4	2	Y	1	1	I
PIC16(L)F1778	(B)	28K	16K	128	2K	25	5/3	6	17	3/3	3	3/3	3	4	3	1	3	2	Y	1	1	I
PIC16(L)F1779	(B)	28K	16K	128	2K	36	5/3	8	28	4/4	4	4/4	4	4	4	1	4	2	Y	1	1	I

Note 1: One pin is input-only.
2: I – Debugging integrated on chip.

Data Sheet Index:

A: DS40001810 PIC16(L)F1773/6 Data Sheet, 28-Pin, 8-bit Flash Microcontrollers
B: DS40001819 PIC16(L)F1777/8/9 Data Sheet, 28/40/44-Pin, 8-bit Flash Microcontrollers

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

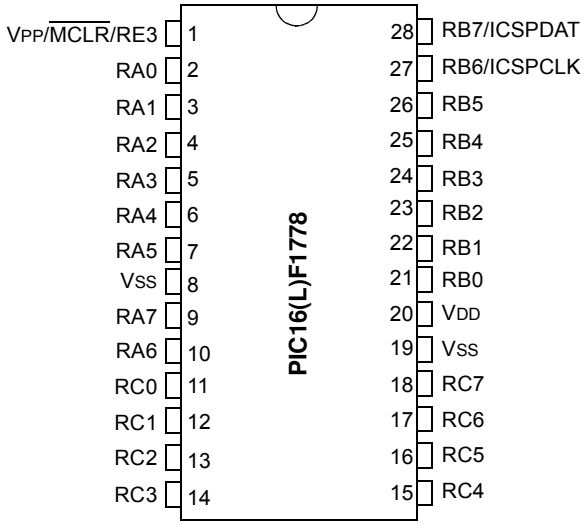
TABLE 2: PACKAGES

Packages	SPDIP	PDIP	SOIC	SSOP	UQFN	QFN	TQFP
PIC16(L)F1778	•		•	•	•		
PIC16(L)F1777/9		•			•	•	•

Note: Pin details are subject to change.

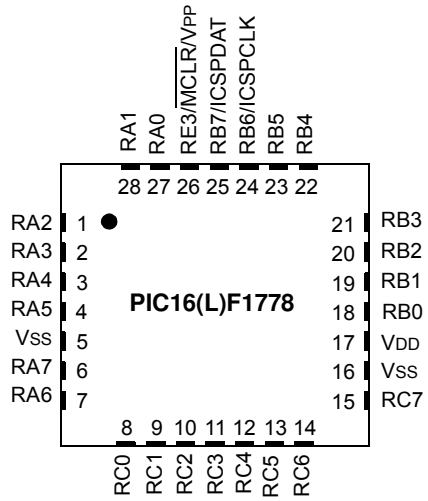
PIN DIAGRAMS

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP



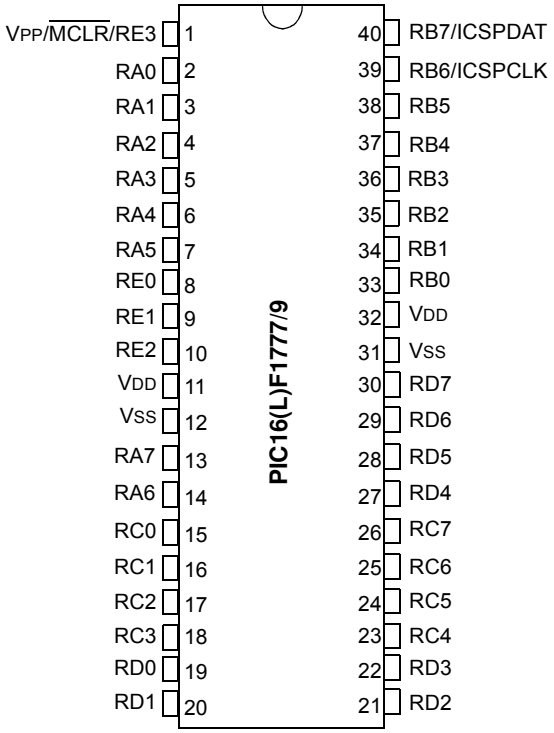
Note: See Table 3 for location of all peripheral functions.

FIGURE 2: 28-PIN UQFN (6x6x0.5 mm)



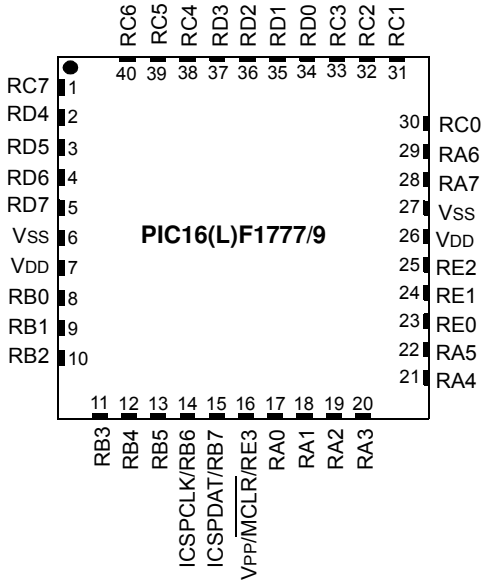
Note: See Table 3 for location of all peripheral functions.

FIGURE 3: 40-PIN PDIP



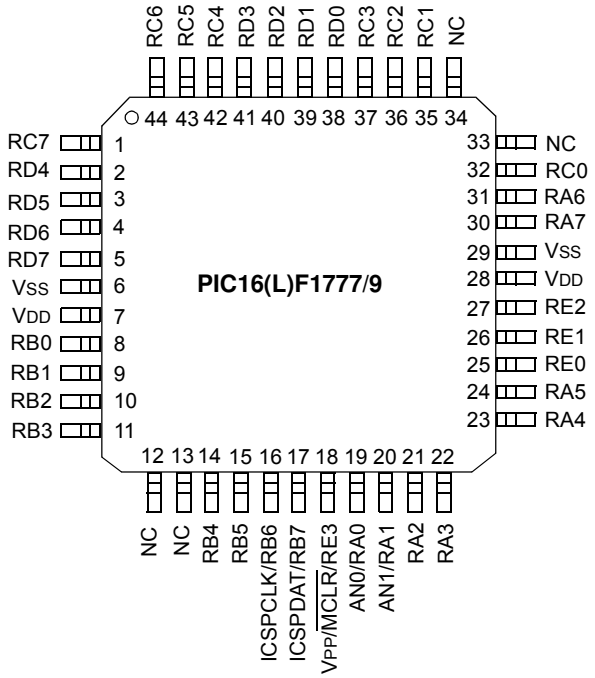
Note: See Table 4 for location of all peripheral functions.

FIGURE 4: 40-PIN UQFN (5x5x0.5 mm)



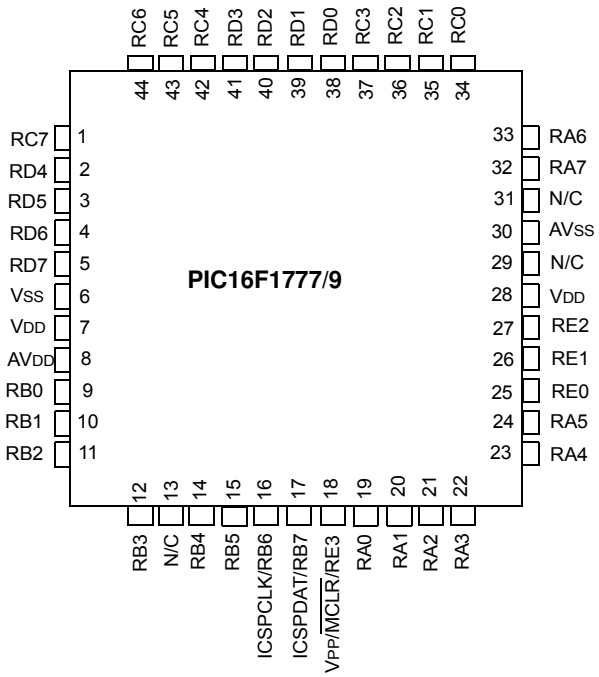
Note: See Table 4 for location of all peripheral functions.

FIGURE 5: 44-PIN TQFP (10x10 mm)



Note: See Table 4 for location of all peripheral functions.

FIGURE 6: 44-PIN QFN (8X8 mm)



Note: See Table 4 for location of all peripheral functions.

PIN ALLOCATION TABLES

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1778)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RA0	2	27	AN0	—	—	—	C1IN0- C2IN0- C3IN0- C4IN0- C5IN0- C6IN0-	—	—	—	—	—	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RA1	3	28	AN1	—	—	OPA1OUT OPA2IN1+ OPA2IN1-	C1IN1- C2IN1- C3IN1- C4IN1-	—	PRG1IN0 PRG2IN1	—	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	—	—
RA2	4	1	AN2 VREF-	DAC1REF0- DAC2REF0- DAC3REF0- DAC4REF0- DAC5REF0- DAC7REF0-	DAC1OUT1	—	C1IN0+ C2IN0+ C3IN0+ C4IN0+ C5IN0+ C6IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RA3	5	2	AN3 VREF+	DAC1REF0+ DAC2REF0+ DAC3REF0+ DAC4REF0+ DAC5REF0+ DAC7REF0+	—	—	C1IN1+	—	—	—	—	—	—	—	MD1CL(1)	—	—	IOC	Y	—	—
RA4	6	3	—	—	DAC4OUT1	OPA1IN0+	—	—	PRG1R(1)	T0CKI	—	—	—	—	MD1CH(1)	—	—	IOC	Y	—	—
RA5	7	4	AN4	—	DAC2OUT1	OPA1IN0-	—	—	PRG1F(1)	—	—	—	—	—	MD1MOD(1)	—	$\overline{SS}$	IOC	Y	—	—
RA6	10	7	—	—	—	—	C6IN1+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC2 CLKOUT
RA7	9	6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC1 CLKIN
RB0	21	18	AN12	—	—	—	C2IN1+	ZCD	—	—	—	—	COG1IN(1)	—	—	—	—	IOC INT	Y	HIB0	—
RB1	22	19	AN10	—	—	OPA2OUT OPA1IN1+ OPA1IN1-	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1	—	—	—	COG2IN(1)	—	—	—	—	IOC	Y	HIB1	—
RB2	23	20	AN8	—	DAC3OUT1	OPA2IN0-	—	—	—	—	—	—	COG3IN(1)	—	—	—	—	IOC	Y	—	—
RB3	24	21	AN9	—	—	OPA2IN0+	C1IN2- C2IN2- C3IN2-	—	—	—	—	—	—	—	MD3CL(1)	—	—	IOC	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1778) (CONTINUED)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RB4	25	22	AN11	—	—	—	C3IN1+	—	—	T5G	—	—	—	—	MD3CH(1)	—	—	IOC	Y	—	—
RB5	26	23	AN13	DAC5REF1- DAC7REF1-	—	—	C4IN2-	—	—	T1G	—	CCP7(1)	—	—	MD3MOD(1)	—	—	IOC	Y	—	—
RB6	27	24	—	DAC5REF1+ DAC7REF1+	—	—	C4IN1+	—	—	—	—	—	—	CLCIN2(1)	—	—	—	IOC	Y	—	ICSPCLK
RB7	28	25	—	—	DAC1OUT2 DAC2OUT2 DAC3OUT2 DAC4OUT2 DAC5OUT2 DAC7OUT2	—	C5IN1+	—	—	T6IN(1)	—	—	—	CLCIN3(1)	—	—	—	IOC	Y	—	ICSPDAT
RC0	11	8	—	—	DAC5OUT1	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SOSCO	—	—	—	—	—	—	—	IOC	Y	—	—
RC1	12	9	—	—	DAC7OUT1	—	—	—	PRG2R(1)	SOSCI	—	CCP2(1)	—	—	—	—	—	IOC	Y	—	—
RC2	13	10	AN14	—	—	—	C5IN2- C6IN2-	—	PRG2F(1)	T5CKI	—	CCP1(1)	—	—	—	—	—	IOC	Y	—	—
RC3	14	11	AN15	—	—	—	C1IN4- C2IN4- C3IN4- C4IN4- C5IN4- C6IN4-	—	—	T2IN(1)	—	—	—	—	MD2CL(1)	—	SCL	IOC	Y	—	—
RC4	15	12	AN16	—	—	—	C5IN3- C6IN3-	—	PRG3R(1)	T8IN(1)	—	—	—	—	MD2CH(1)	—	SDA	IOC	Y	—	—
RC5	16	13	AN17	—	—	OPA3IN0+	—	—	PRG3F(1)	T4IN(1)	—	—	—	—	MD2MOD(1)	—	—	IOC	Y	—	—
RC6	17	14	AN18	—	—	OPA3OUT	C5IN1- C6IN1-	—	PRG3IN0	—	—	—	—	—	—	—	—	IOC	Y	—	—
RC7	18	15	AN19	—	—	OPA3IN0-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	—	—	$\overline{MCLR}$ V_{PP}
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VSS	19	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1778) (CONTINUED)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
OUT(2)	—	—	—	—	—	—	C1OUT C2OUT C3OUT C4OUT C5OUT C6OUT	—	—	—	PWM3 PWM4 PWM5 PWM6 PWM9 PWM11	CCP1 CCP2 CCP7	COG1A COG1B COG1C COG1D COG2A COG2B COG2C COG2D COG3A COG3B COG3C COG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	MD1OUT MD2OUT MD3OUT	DT(3) TX CK	SDO SDA(3) SCK SCL(3)	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1777/9)

I/O	40-Pin PDIP	40-Pin (U)QFN	44-Pin TQFP	44-Pin QFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RA0	2	17	19	19	AN0	—	—	—	C1IN0- C2IN0- C3IN0- C4IN0- C5IN0- C6IN0- C7IN0- C8IN0-	—	—	—	—	—	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RA1	3	18	20	20	AN1	—	—	OPA1OUT OPA2IN1+ OPA2IN1-	C1IN1- C2IN1- C3IN1- C4IN1-	—	PRG1IN0 PRG2IN1	—	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	—	—
RA2	4	19	21	21	AN2	DAC1REF0- DAC2REF0- DAC3REF0- DAC4REF0- DAC5REF0- DAC6REF0- DAC7REF0- DAC8REF0-	DAC1OUT1	—	C1IN0+ C2IN0+ C3IN0+ C4IN0+ C5IN0+ C6IN0+ C7IN0+ C8IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RA3	5	20	22	22	AN3	DAC1REF0+ DAC2REF0+ DAC3REF0+ DAC4REF0+ DAC5REF0+ DAC6REF0+ DAC7REF0+ DAC8REF0+	—	—	C1IN1+	—	—	—	—	—	—	—	MD1CL(1)	—	—	IOC	Y	—	—
RA4	6	21	23	23	—	—	—	OPA1IN0+	—	—	PRG1R(1)	—	—	—	—	—	MD1CH(1)	—	—	IOC	Y	—	—
RA5	7	22	24	24	AN4	—	DAC2OUT1	OPA1IN0-	—	—	PRG1F(1)	—	—	—	—	—	MD1MOD(1)	—	$\overline{SS}$	IOC	Y	—	—
RA6	14	29	31	33	—	—	—	—	C6IN1+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC2 CLKOUT
RA7	13	28	30	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC1 CLKIN
RB0	33	8	8	9	AN12	—	—	—	C2IN1+	ZCD	—	—	—	CCP8(1)	COG1IN(1)	—	MD4CL(1)	—	—	IOC INT	Y	HIB0	—
RB1	34	9	9	10	AN10	—	—	OPA2OUT OPA1IN1+ OPA1IN1-	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1 PRG4R(1)	—	—	—	COG2IN(1)	—	MD4CH(1)	—	—	IOC	Y	HIB1	—
RB2	35	10	10	11	AN8	—	DAC3OUT1	OPA2IN0-	—	—	PRG4F(1)	—	—	—	COG3IN(1)	—	MD4MOD(1)	—	—	IOC	Y	—	—
RB3	36	11	11	12	AN9	—	—	OPA2IN0+	C1IN2- C2IN2- C3IN2-	—	—	—	—	—	—	—	MD3CL(1)	—	—	IOC	Y	—	—
RB4	37	12	14	14	AN11	—	—	—	C3IN1+	—	—	—	—	—	—	—	MD3CH(1)	—	—	IOC	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1777/9) (CONTINUED)

I/O	40-Pin PDIP	40-Pin (U)QFN	44-Pin TQFP	44-Pin QFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RB5	38	13	15	15	AN13	DAC5REF1- DAC7REF1-	—	—	C4IN2-	—	—	—	—	CCP7(1)	—	—	MD3MOD(1)	—	—	IOC	Y	—	—
RB6	39	14	16	16	—	DAC5REF1+ DAC7REF1+	—	—	C4IN1+	—	—	—	—	—	—	CLCIN2(1)	—	—	—	IOC	Y	—	ICSPCLK
RB7	40	15	17	17	—	—	DAC1OUT2 DAC2OUT2 DAC3OUT2 DAC4OUT2 DAC5OUT2 DAC6OUT2 DAC7OUT2 DAC8OUT2	—	C5IN1+	—	—	T6IN(1)	—	—	—	CLCIN3(1)	—	—	—	IOC	Y	—	ICSPDAT
RC0	15	30	32	34	—	—	DAC5OUT1	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SOSCO	—	—	—	—	—	—	—	IOC	Y	—	—
RC1	16	31	35	35	—	—	DAC7OUT1	—	—	—	PRG2R(1)	SOSCI	—	CCP2(1)	—	—	—	—	—	IOC	Y	—	—
RC2	17	32	36	36	AN14	—	—	—	C5IN2- C6IN2-	—	PRG2F(1)	—	—	CCP1(1)	—	—	—	—	—	IOC	Y	—	—
RC3	18	33	37	37	AN15	—	—	—	—	—	—	T2IN(1)	—	—	—	—	MD2CL(1)	—	SCL	IOC	Y	—	—
RC4	23	38	42	42	AN16	—	—	—	C5IN3- C6IN3-	—	PRG3R(1)	T8IN(1)	—	—	—	—	MD2CH(1)	—	SDA	IOC	Y	—	—
RC5	24	39	43	43	AN17	—	—	OPA3IN0+	—	—	PRG3F(1)	T4IN(1)	—	—	—	—	MD2MOD(1)	—	—	IOC	Y	—	—
RC6	25	40	44	44	AN18	—	—	OPA3OUT OPA4IN1+ OPA4IN1-	C5IN1- C6IN1- C7IN1- C8IN1-	—	PRG3IN0 PRG4IN1	—	—	—	—	—	—	—	—	IOC	Y	—	—
RC7	26	1	1	1	AN19	—	—	OPA3IN0-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RD0	19	34	38	38	AN20	—	—	OPA4IN0+	—	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD1	20	35	39	39	AN21	—	—	OPA4OUT OPA3IN1+ OPA3IN1-	C1IN4- C2IN4- C3IN4- C4IN4- C5IN4- C6IN4- C7IN4- C8IN4-	—	PRG3IN1 PRG4IN0	—	—	—	—	—	—	—	—	—	Y	—	—
RD2	21	36	40	40	AN22	—	DAC4OUT1	OPA4IN0-	—	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD3	22	37	41	41	AN23	—	—	—	C8IN2-	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD4	27	2	2	2	AN24	—	—	—	C7IN2-	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD5	28	3	3	3	AN25	—	—	—	C7IN3- C8IN3-	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD6	29	4	4	4	AN26	—	—	—	C7IN1+	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD7	30	5	5	5	AN27	—	—	—	C8IN1+	—	—	—	—	—	—	—	—	—	—	—	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1777/9) (CONTINUED)

I/O	40-Pin PDIP	40-Pin (U)QFN	44-Pin TQFP	44-Pin QFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RE0	8	23	25	25	AN5	DAC6REF1+ DAC8REF1+	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RE1	9	24	26	26	AN6	DAC6REF1- DAC8REF1-	DAC6OUT1	—	—	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RE2	10	25	27	27	AN7	—	DAC8OUT1	—	—	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	$\overline{MCLR}$ V_{PP}
V_{DD}	11	7	7	7,8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{DD}	32	26	28	28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	12	6	6	6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{SS}	31	27	29	30	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	—		—	—	—	—	C1OUT C2OUT C3OUT C4OUT C5OUT C6OUT C7OUT C8OUT	—	—	—	PWM3 PWM4 PWM5 PWM6 PWM9 PWM10 PWM11 PWM12	CCP1 CCP2 CCP7 CCP8	COG1A COG1B COG1C COG1D COG2A COG2B COG2C COG2D COG3A COG3B COG3C COG3D COG4A COG4B COG4C COG4D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	MD1OUT MD2OUT MD3OUT MD4OUT	DT(3) TX CK	SDO SDA(3) SCK SCL(3)	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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1.0 DEVICE OVERVIEW

The PIC16(L)F1777/8/9 are described within this data sheet. See Table 2 for available package configurations.

Figure 1-1 shows a block diagram of the PIC16(L)F1777/8/9 devices. Table 1-2 shows the pinout descriptions.

Refer to Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1778	PIC16(L)F1777/9
Analog-to-Digital Converter (ADC)		•	•
Fixed Voltage Reference (FVR)		•	•
Zero-Cross Detection (ZCD)		•	•
Temperature Indicator		•	•
Complementary Output Generator (COG)			
	COG1	•	•
	COG2	•	•
	COG3	•	•
	COG4		•
Programmable Ramp Generator (PRG)			
	PRG1	•	•
	PRG2	•	•
	PRG3	•	•
	PRG4		•
10-bit Digital-to-Analog Converter (DAC)			
	DAC1	•	•
	DAC2	•	•
	DAC5	•	•
	DAC6		•
5-bit Digital-to-Analog Converter (DAC)			
	DAC3	•	•
	DAC4	•	•
	DAC7	•	•
	DAC8		•
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	•	•
	CCP2	•	•
	CCP7	•	•
	CCP8		•
Comparators			
	C1	•	•
	C2	•	•
	C3	•	•
	C4	•	•
	C5	•	•
	C6	•	•
	C7		•
	C8		•

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1778	PIC16(L)F1777/9
Configurable Logic Cell (CLC)			
	CLC1	•	•
	CLC2	•	•
	CLC3	•	•
	CLC4	•	•
Data Signal Modulator (DSM)			
	DSM1	•	•
	DSM2	•	•
	DSM3	•	•
	DSM4		•
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)			
	EUSART	•	•
Master Synchronous Serial Ports			
	MSSP	•	•
Op Amps			
	OPA1	•	•
	OPA2	•	•
	OPA3	•	•
	OPA4		•
10-bit Pulse-Width Modulator (PWM)			
	PWM3	•	•
	PWM4	•	•
	PWM9	•	•
	PWM10		•
16-bit Pulse-Width Modulator (PWM)			
	PWM5	•	•
	PWM6	•	•
	PWM11	•	•
	PWM12		•
8-bit Timers			
	Timer0	•	•
	Timer2	•	•
	Timer4	•	•
	Timer6	•	•
	Timer8	•	•
16-bit Timers			
	Timer1	•	•
	Timer3	•	•
	Timer5	•	•

1.1 Register and Bit naming conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral, thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to the Push-Pull mode:

EXAMPLE 1-1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

EXAMPLE 1-2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt, and Mirror Bits

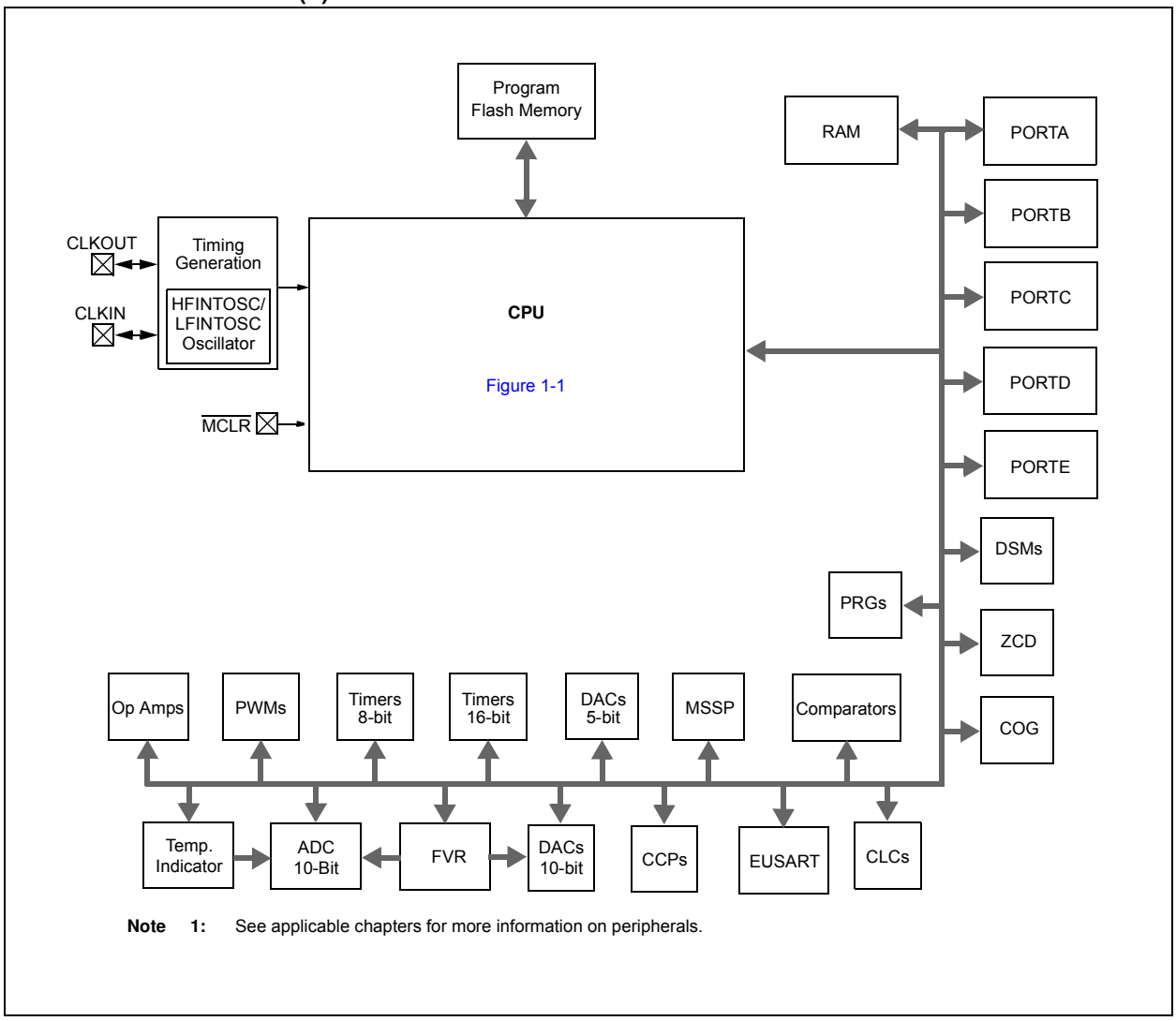
Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

- EUSART
- MSSP

FIGURE 1-1: PIC16(L)F1777/8/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/ C3IN0-/C4IN0-/C5IN0-/ C6IN0-/CLCIN0(1)	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0-	AN	—	Comparator 1 negative input.
	C2IN0-	AN	—	Comparator 2 negative input.
	C3IN0-	AN	—	Comparator 3 negative input.
	C4IN0-	AN	—	Comparator 4 negative input.
	C5IN0-	AN	—	Comparator 5 negative input.
	C6IN0-	AN	—	Comparator 6 negative input.
	CLCIN0(1)	TTL/ST	—	CLC input 0.
RA1/AN1/C1IN1-/C2IN1-/ C3IN1-/C4IN1-/PRG1IN0/ PRG2IN1/OPA1OUT/OPA2IN1+/ OPA2IN1-/CLCIN1(1)	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	Channel 1 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	C3IN1-	AN	—	Comparator 3 negative input.
	C4IN1-	AN	—	Comparator 4 negative input.
	PRG1IN0	AN	—	Ramp generator 1 reference voltage input.
	PRG2IN1	AN	—	Ramp generator 2 reference voltage input.
	OPA1OUT	—	AN	Operational amplifier 1 output.
	OPA2IN1+	AN	—	Operational amplifier 2 non-inverting input.
	OPA2IN1-	AN	—	Operational amplifier 2 inverting input.
	CLCIN1(1)	TTL/ST	—	CLC input 1.
RA2/AN2/VREF-/DAC1REF0-/ DAC2REF0-/DAC3REF0-/ DAC4REF0-/DAC5REF0-/ DAC7REF0-/C1IN0+/C2IN0+/ C3IN0+/C4IN0+/C5IN0+/ C6IN0+/DAC1OUT1	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	VREF-	AN	—	ADC negative reference.
	DAC1REF0-	AN	—	DAC1 negative reference.
	DAC2REF0-	AN	—	DAC2 negative reference.
	DAC3REF0-	AN	—	DAC3 negative reference.
	DAC4REF0-	AN	—	DAC4 negative reference.
	DAC5REF0-	AN	—	DAC5 negative reference.
	DAC7REF0-	AN	—	DAC7 negative reference.
	C1IN0+	AN	—	Comparator 1 positive input.
	C2IN0+	AN	—	Comparator 2 positive input.
	C3IN0+	AN	—	Comparator 3 positive input.
	C4IN0+	AN	—	Comparator 4 positive input.
	C5IN0+	AN	—	Comparator 5 positive input.
	C6IN0+	AN	—	Comparator 6 positive input.
	DAC1OUT1	—	AN	DAC1 voltage output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA3/AN3/VREF+/DAC1REF0+/ DAC2REF0+/DAC3REF0+/ DAC4REF0+/DAC5REF0+/ DAC7REF0+/C1IN1+/MD1CL	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC positive reference.
	DAC1REF0+	AN	—	DAC1 positive reference.
	DAC2REF0+	AN	—	DAC2 positive reference.
	DAC3REF0+	AN	—	DAC3 positive reference.
	DAC4REF0+	AN	—	DAC4 positive reference.
	DAC5REF0+	AN	—	DAC5 positive reference.
	DAC7REF0+	AN	—	DAC7 positive reference.
	C1IN1+	AN	—	Comparator 1 positive input.
	MD1CL(1)	TTL/ST	—	Data signal modulator 1 low carrier input.
RA4/OPA1IN0+/PRG1R/ MD1CH/DAC4OUT1/T0CKI	RA4	TTL/ST	CMOS	General purpose I/O.
	OPA1IN0+	AN	—	Operational Amplifier 1 non-inverting input.
	PRG1R(1)	TTL/ST	—	Ramp generator set_rising input.
	MD1CH(1)	TTL/ST	—	Data signal modulator 1 high carrier input.
	DAC4OUT1	—	AN	DAC4 voltage output.
	T0CKI(1)	TTL/ST	—	Timer0 clock input.
RA5/AN4/OPA1IN0-/ DAC2OUT1/PRG1F/ MD1MOD/$\overline{SS}$	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	OPA1IN0-	AN	—	Operational amplifier 1 inverting input.
	DAC2OUT1	—	AN	DAC2 voltage output.
	PRG1F(1)	TTL/ST	—	Ramp generator set_falling input.
	MD1MOD(1)	TTL/ST	—	Data signal modulator modulation input.
	$\overline{SS}$	ST	—	Slave Select input.
RA6/CLKOUT/C6IN1+/OSC2	RA6	TTL/ST	CMOS	General purpose I/O.
	CLKOUT	—	CMOS	FOSC/4 output.
	C6IN1+	AN	—	Comparator 6 positive input.
	OSC2	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
RA7/CLKIN/OSC1	RA7	TTL/ST	CMOS	General purpose I/O.
	CLKIN	TTL/ST	—	CLC input.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
RB0/AN12/ZCD/HIB0/C2IN1+/ COG1IN	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	ZCD	AN	—	Zero-cross detection input.
	HIB0	HP	HP	High-Power output.
	C2IN1+	AN	—	Comparator 2 positive input.
	COG1IN(1)	TTL/ST	—	Complementary output generator 1 input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB1/AN10/PRG1IN1/PRG2IN0/ HIB1/C1IN3-/C2IN3-/C3IN3-/ C4IN3-/OPA2OUT/OPA1IN1+/ OPA1IN1-/COG2IN	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	PRG1IN1	AN	—	Ramp generator 1 reference voltage input.
	PRG2IN0	AN	—	Ramp generator 2 reference voltage input.
	HIB1	HP	HP	High-Power output.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	C3IN3-	AN	—	Comparator 3 negative input.
	C4IN3-	AN	—	Comparator 4 negative input.
	OPA2OUT	—	AN	Operational amplifier 2 output.
	OPA1IN1+	AN	—	Operational amplifier 1 non-inverting input.
	OPA1IN1-	AN	—	Operational amplifier 1 inverting input.
	COG2IN(1)	TTL/ST	—	Complementary output generator 2 input.
RB2/AN8/OPA2IN0-/ DAC3OUT1/COG3IN	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN0-	AN	—	Operational amplifier 2 inverting input.
	DAC3OUT1	—	AN	DAC3 voltage output.
	COG3IN(1)	TTL/ST	—	Complementary output generator 3 input.
RB3/AN9/C1IN2-/C2IN2-/ C3IN2-/OPA2IN0+/MD3CL	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	C1IN2-	AN	—	Comparator 1 negative input.
	C2IN2-	AN	—	Comparator 2 negative input.
	C3IN2-	AN	—	Comparator 3 negative input.
	OPA2IN0+	AN		Operational amplifier 2 non-inverting input.
	MD3CL(1)	TTL/ST	—	Data signal modulator 3 low carrier input.
RB4/AN11/C3IN1+/T5G/MD3CH	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
	C3IN1+	AN	—	Comparator 3 positive input.
	T5G(1)	TTL/ST	—	Timer5 gate input.
	MD3CH(1)	TTL/ST	—	Data signal modulator 3 high carrier input.
RB5/AN13/DAC5REF1-/ DAC7REF1-/C4IN2-/T1G/CCP7/ MD3MOD	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 11 input.
	DAC5REF1-	AN	—	DAC5 negative reference.
	DAC7REF1-	AN	—	DAC7 negative reference.
	C4IN2-	AN	—	Comparator 4 negative input.
	T1G(1)	TTL/ST	—	Timer1 gate input.
	CCP7(1)	TTL/ST	—	CCP7 capture input.
	MD3MOD(1)	TTL/ST	—	Data signal modulator modulation input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB6/DAC5REF1+/DAC7REF1+/ C4IN1+/CLCIN2/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	DAC5REF1+	AN	—	DAC5 positive reference.
	DAC7REF1+	AN	—	DAC7 positive reference.
	C4IN1+	AN	—	Comparator 2 positive input.
	CLCIN2(1)	TTL/ST	—	CLC input 2.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/C5IN1+/DAC1OUT2/ DAC2OUT2/DAC3OUT2/ DAC4OUT2/DAC5OUT2/ DAC7OUT2/T6IN/CLCIN3/ ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	C5IN1+	AN	—	Comparator 5 positive input.
	DAC1OUT2	—	AN	DAC1 voltage output.
	DAC2OUT2	—	AN	DAC2 voltage output.
	DAC3OUT2	—	AN	DAC3 voltage output.
	DAC4OUT2	—	AN	DAC4 voltage output.
	DAC5OUT2	—	AN	DAC5 voltage output.
	DAC7OUT2	—	AN	DAC7 voltage output.
	T6IN(1)	TTL/ST	—	Timer6 gate input.
	CLCIN3(1)	TTL/ST	—	CLC input 3.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/DAC5OUT1/T1CKI/T3CKI/ T3G/SOSCO	RC0	TTL/ST	CMOS	General purpose I/O.
	DAC5OUT1	—	AN	DAC5 voltage output.
	T1CKI(1)	AN	—	Comparator 4 negative input.
	T3CKI(1)	TTL/ST	—	Timer3 clock input.
	T3G(1)	TTL/ST	—	Timer3 gate input.
	SOSCO	—	XTAL	Secondary oscillator output.
RC1/DAC7OUT1/PRG2R/CCP2/ SOSCI	RC1	TTL/ST	CMOS	General purpose I/O.
	DAC7OUT1	—	AN	DAC7 voltage output.
	PRG2R(1)	TTL/ST	—	Ramp generator set_rising input.
	CCP2(1)	TTL/ST	—	CCP2 capture input.
	SOSCI	XTAL	—	Secondary oscillator input.
RC2/AN14/C5IN2-/C6IN2-/ PRG2F/CCP1/T5CKI	RC2	TTL/ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	C5IN2-	AN	—	Comparator 5 negative input.
	C6IN2-	AN	—	Comparator 6 negative input.
	PRG2F(1)	TTL/ST	—	Ramp generator set_falling input.
	CCP1(1)	TTL/ST	—	CCP1 capture input.
	T5CKI(1)	TTL/ST	—	Timer5 clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC3/AN15/C1IN4-/C2IN4-/C3IN4-/C4IN4-/C5IN4-/C6IN4-/T2IN//MD2CL/SCL	RC3	TTL/ST	CMOS	General purpose I/O.
	AN15	AN	—	ADC Channel 15 input.
	C1IN4-	AN	—	Comparator 1 negative input.
	C2IN4-	AN	—	Comparator 2 negative input.
	C3IN4-	AN	—	Comparator 3 negative input.
	C4IN4-	AN	—	Comparator 4 negative input.
	C5IN4-	AN	—	Comparator 5 negative input.
	C6IN4-	AN	—	Comparator 6 negative input.
	T2IN(1)	TTL/ST	—	Timer2 gate input.
	MD2CL(1)	TTL/ST	—	Data signal modulator 2 low carrier input.
	SCL	I^2C	OD	I^2C clock.
RC4/AN16/C5IN3-/C6IN3-/T8IN/PRG3R/MD2CH/SDA	RC4	TTL/ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	C5IN3-	AN	—	Comparator 5 negative input.
	C6IN3-	AN	—	Comparator 6 negative input.
	T8IN(1)	TTL/ST	—	Timer8 gate input.
	PRG3R(1)	TTL/ST	—	Ramp generator set_rising input.
	MD2CH(1)	TTL/ST	—	Data signal modulator 2 high carrier input.
	SDA	I^2C	OD	I^2C data input/output.
RC5/AN17/OPA3IN0+/T4IN/PRG3F/MD2MOD	RC5	TTL/ST	CMOS	General purpose I/O.
	AN17	AN	—	ADC Channel 17 input.
	OPA3IN0+	AN	—	Operational amplifier 3 inverting input.
	T4IN(1)	TTL/ST	—	Timer4 gate input.
	PRG3F(1)	TTL/ST	—	Ramp generator set_falling input.
	MD2MOD(1)	TTL/ST	—	Data signal modulator modulation input.
RC6/AN18/PRG3IN0/C5IN1-/C6IN1-/OPA3OUT	RC6	TTL/ST	CMOS	General purpose I/O.
	AN18	AN	—	ADC Channel 18 input.
	PRG3IN0	AN	—	Ramp generator 3 reference voltage input.
	C5IN1-	AN	—	Comparator 5 negative input.
	C6IN1-	AN	—	Comparator 6 negative input.
	OPA3OUT	—	AN	Operational amplifier 3 output.
RC7/AN19/OPA3IN0-	RC7	TTL/ST	CMOS	General purpose I/O.
	AN19	AN	—	ADC Channel 19 input.
	OPA3IN0-	AN	—	Operational amplifier 3 non-inverting input.
RE3/$\overline{MCLR}$	RE3	TTL/ST	CMOS	General purpose input.
	$\overline{MCLR}$	ST	—	Master clear input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

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HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	C3OUT		CMOS	Comparator 3 output.
	C4OUT		CMOS	Comparator 4 output.
	C5OUT		CMOS	Comparator 5 output.
	C6OUT		CMOS	Comparator 6 output.
	CCP1		CMOS	Compare/PWM1 output.
	CCP2		CMOS	Compare/PWM2 output.
	CCP7		CMOS	Compare/PWM7 output.
	MD1OUT		CMOS	Data signal modulator 1 output.
	MD2OUT		CMOS	Data signal modulator 2 output.
	MD3OUT		CMOS	Data signal modulator 3 output.
	PWM3OUT		CMOS	PWM3 output.
	PWM4OUT		CMOS	PWM4 output.
	PWM5OUT		CMOS	PWM5 output.
	PWM6OUT		CMOS	PWM6 output.
	PWM9OUT		CMOS	PWM9 output.
	PWM11OUT		CMOS	PWM11 output.
	COG1A		CMOS	Complementary output generator 1 output A.
	COG1B		CMOS	Complementary output generator 1 output B.
	COG1C		CMOS	Complementary output generator 1 output C.
	COG1D		CMOS	Complementary output generator 1 output D.
	COG2A		CMOS	Complementary output generator 2 output A.
	COG2B		CMOS	Complementary output generator 2 output B.
	COG2C		CMOS	Complementary output generator 2 output C.
	COG2D		CMOS	Complementary output generator 2 output D.
	COG3A		CMOS	Complementary output generator 3 output A.
	COG3B		CMOS	Complementary output generator 3 output B.
	COG3C		CMOS	Complementary output generator 3 output C.
	COG3D		CMOS	Complementary output generator 3 output D.
	SDA(3)		OD	I^2C data output.
	SCK		CMOS	SPI clock output.
	SCL(3)		OD	I^2C clock output.
	SDO		CMOS	SPI data output.
	TX		CMOS	EUSART asynchronous TX data out.
	CK		CMOS	EUSART synchronous clock out.
	DT(3)		CMOS	EUSART synchronous data output.
	CLC1OUT		CMOS	Configurable logic cell 1 output.
	CLC2OUT		CMOS	Configurable logic cell 2 output.
	CLC3OUT		CMOS	Configurable logic cell 3 output.
	CLC4OUT		CMOS	Configurable logic cell 4 output.

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TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/ C3IN0-/C4IN0-/C5IN0-/ C6IN0-/C7IN0-/C8IN0-/CLCIN0	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0-	AN	—	Comparator 1 negative input.
	C2IN0-	AN	—	Comparator 2 negative input.
	C3IN0-	AN	—	Comparator 3 negative input.
	C4IN0-	AN	—	Comparator 4 negative input.
	C5IN0-	AN	—	Comparator 5 negative input.
	C6IN0-	AN	—	Comparator 6 negative input.
	C7IN0-	AN	—	Comparator 7 negative input.
	C8IN0-	AN	—	Comparator 8 negative input.
	CLCIN0(1)	TTL/ST	—	CLC input 0.
RA1/AN1/C1IN1-/C2IN1-/ C3IN1-/C4IN1-/PRG1IN0/ PRG2IN1/OPA1OUT/OPA2IN1+/ OPA2IN1-/CLCIN1	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	Channel 1 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	C3IN1-	AN	—	Comparator 3 negative input.
	C4IN1-	AN	—	Comparator 4 negative input.
	PRG1IN0	AN	—	Ramp generator 1 reference voltage input.
	PRG2IN1	AN	—	Ramp generator 2 reference voltage input.
	OPA1OUT	—	AN	Operational amplifier 1 output.
	OPA2IN1+	AN	—	Operational amplifier 2 non-inverting input.
	OPA2IN1-	AN	—	Operational amplifier 2 inverting input.
	CLCIN1(1)	TTL/ST	—	CLC input 0.

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HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA2/AN2/DAC1REF0-/ DAC2REF0-/DAC3REF0-/ DAC4REF0-/DAC5REF0-/ DAC6REF0-/DAC7REF0-/ DAC8REF0-/C1IN0+/C2IN0+/ C3IN0+/C4IN0+/C5IN0+/ C6IN0+/C7IN0+/C8IN0+/ DAC1OUT1	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	DAC1REF0-	AN	—	DAC1 negative reference.
	DAC2REF0-	AN	—	DAC2 negative reference.
	DAC3REF0-	AN	—	DAC3 negative reference.
	DAC4REF0-	AN	—	DAC4 negative reference.
	DAC5REF0-	AN	—	DAC5 negative reference.
	DAC6REF0-	AN	—	DAC6 negative reference.
	DAC7REF0-	AN	—	DAC7 negative reference.
	DAC8REF0-	AN	—	DAC8 negative reference.
	C1IN0+	AN	—	Comparator 1 positive input.
	C2IN0+	AN	—	Comparator 2 positive input.
	C3IN0+	AN	—	Comparator 3 positive input.
	C4IN0+	AN	—	Comparator 4 positive input.
	C5IN0+	AN	—	Comparator 5 positive input.
	C6IN0+	AN	—	Comparator 6 positive input.
	C7IN0+	AN	—	Comparator 7 positive input.
	C8IN0+	AN	—	Comparator 8 positive input.
	DAC1OUT1	—	AN	DAC1 voltage output.
RA3/AN3/DAC1REF0+/ DAC2REF0+/DAC3REF0+/ DAC4REF0+/DAC5REF0+/ DAC6REF0+/DAC7REF0+/ DAC8REF0+/C1IN1+/MD1CL	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC positive reference.
	DAC1REF0+	AN	—	DAC1 positive reference.
	DAC2REF0+	AN	—	DAC2 positive reference.
	DAC3REF0+	AN	—	DAC3 positive reference.
	DAC4REF0+	AN	—	DAC4 positive reference.
	DAC5REF0+	AN	—	DAC5 positive reference.
	DAC6REF0+	AN	—	DAC6 positive reference.
	DAC7REF0+	AN	—	DAC7 positive reference.
	DAC8REF0+	AN	—	DAC8 positive reference.
	C1IN1+	AN	—	Comparator 1 positive input.
	MD1CL(1)	TTL/ST	—	Data signal modulator 1 low carrier input.
RA4/OPA1IN0+/PRG1R/MD1CH	RA4	TTL/ST	CMOS	General purpose I/O.
	OPA1IN0+	AN	—	Operational Amplifier 1 non-inverting input.
	PRG1R(1)	TTL/ST	—	Ramp generator set_rising input.
	MD1CH(1)	TTL/ST	—	Data signal modulator 1 high carrier input.

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Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.