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PIC16(L)F1782/3

28-Pin 8-Bit Advanced Analog Flash Microcontroller

High-Performance RISC CPU:

- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
- Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Memory Features:

- Up to 4 KW Flash Program Memory:
  - Self-programmable under software control
  - Programmable code protection
  - Programmable write protection
- 256 Bytes of Data EEPROM
- Up to 512 Bytes of RAM

High Performance PWM Controller:

- Two Programmable Switch Mode Controller (PSMC) modules:
  - Digital and/or analog feedback control of PWM frequency and pulse begin/end times
  - 16-bit Period, Duty Cycle and Phase
  - 16 ns clock resolution
  - Supports Single PWM, Complementary, Push-Pull and 3-phase modes of operation
  - Dead-band control with 8-bit counter
  - Auto-shutdown and restart
  - Leading and falling edge blanking
  - Burst mode

Extreme Low-Power Management PIC16LF1782/3 with XLP:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Timer1 Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 μA @ 32 kHz, 1.8V, typical
  - 32 μA/MHz @ 1.8V, typical

Analog Peripheral Features:

- Analog-to-Digital Converter (ADC):
  - Fully differential 12-bit converter
  - Up to 75 ksps conversion rate
  - 11 single-ended channels
  - 5 differential channels
  - Positive and negative reference selection
- 8-bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Positive and negative reference selection
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Three High-Speed Comparators:
  - 50 ns response time @ V_{DD} = 5V
  - Rail-to-rail inputs
  - Software selectable hysteresis
  - Internal connection to op amps, FVR and DAC
- Two Operational Amplifiers:
  - Rail-to-rail inputs/outputs
  - High/Low selectable Gain Bandwidth Product
  - Internal connection to DAC and FVR
- Fixed Voltage Reference (FVR):
  - 1.024V, 2.048V and 4.096V output levels
  - Internal connection to ADC, comparators and DAC

I/O Features:

- 25 I/O Pins and 1 Input-only Pin:
- High current sink/source for LED drivers
- Individually programmable interrupt-on-change pins
- Individually programmable weak pull-ups
- Individual input level selection
- Individually programmable slew rate control
- Individually programmable open drain outputs

Digital Peripheral Features:

- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture/Compare/PWM modules (CCP):
  - 16-bit capture, maximum resolution 12.5 ns
  - 16-bit compare, max resolution 31.25 ns
  - 10-bit PWM, max frequency 32 kHz
- Master Synchronous Serial Port (SSP) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-baud detect
  - Auto-wake-up on start

Oscillator Features:

- Operate up to 32 MHz from Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 32.768 kHz Timer1 Oscillator:
  - Available as system clock
  - Low-power RTC
- External Oscillator Block with:
  - 4 crystal/resonator modes up to 32 MHz using 4x PLL
  - 3 external clock modes up to 32 MHz
- 4x Phase-Locked Loop (PLL)
- Fail-Safe Clock Monitor:
  - Detect and recover from external oscillator failure
- Two-Speed Start-up:
  - Minimize latency between code execution and external oscillator start-up

General Microcontroller Features:

- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debug (ICD)
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1782/3)
  - 2.3V to 5.5V (PIC16F1782/3)

PIC16(L)F178X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	Data SRAM (bytes)	I/O's(2)	12-bit ADC (ch)	Comparators	Operational Amplifiers	DAC (8/5-bit)	Timers (8/16-bit)	Programmable Switch Mode Controllers (PSMC)	CCP	EUSART	MSSP (I^2C™/SPI)	Debug(1)	XLP
PIC12(L)F1782	(1)	2048	256	256	25	11	3	2	1/0	2/1	2	2	1	1	I	Y
PIC16(L)F1783	(1)	4096	256	512	25	11	3	2	1/0	2/1	2	2	1	1	I	Y
PIC16(L)F1784	(2)	4096	256	512	36	15	4	3	1/0	2/1	3	3	1	1	I	Y
PIC16(L)F1786	(2)	8192	256	1024	25	11	4	2	1/0	2/1	3	3	1	1	I	Y
PIC16(L)F1787	(2)	8192	256	1024	36	15	4	3	1/0	2/1	3	3	1	1	I	Y
PIC16(L)F1788	(3)	16384	256	2048	25	11	4	2	1/3	2/1	4	3	1	1	I	Y
PIC16(L)F1789	(3)	16384	256	2048	36	15	4	3	1/3	2/1	4	3	1	1	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

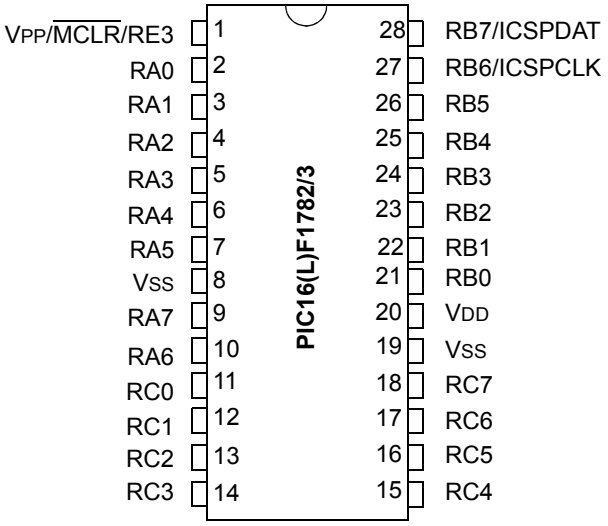
1: DS40001579 PIC16(L)F1782/3 Data Sheet, 28-Pin Flash, 8-bit Advanced Analog MCUs.

2: DS40001637 PIC16(L)F1784/6/7 Data Sheet, 28/40/44-Pin Flash, 8-bit Advanced Analog MCUs.

3: DS40001675 PIC16(L)F1788/9 Data Sheet, 28/40/44-Pin Flash, 8-bit Advanced Analog MCUs.

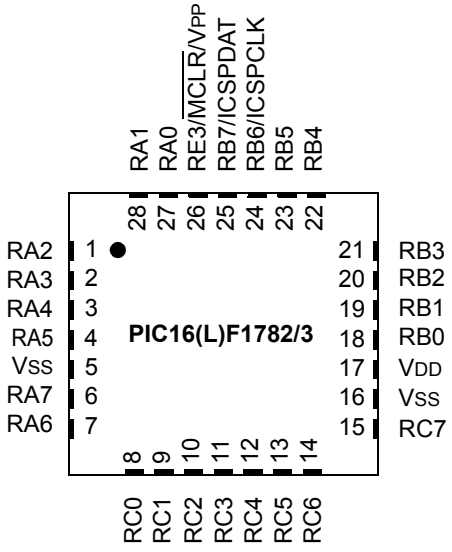
Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

Pin Diagram – 28-Pin SPDIP, SOIC, SSOP



Note: See Table 1 for the location of all peripheral functions.

Pin Diagram – 28-Pin QFN, UQFN



Note: See Table 1 for the location of all peripheral functions.

PIN ALLOCATION TABLE

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1782/3)

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN, UQFN	ADC	ADC Reference	Comparator	Operation Amplifiers	8-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN0	—	C1IN0- C2IN0- C3IN0-	—	—	—	—	—	—	—	IOC	Y	—
RA1	3	28	AN1	—	C1IN1- C2IN1- C3IN1-	OPA1OUT	—	—	—	—	—	—	IOC	Y	—
RA2	4	1	AN2	VREF-	C1IN0+ C2IN0+ C3IN0+	—	DACOUT1 DACVREF-	—	—	—	—	—	IOC	Y	—
RA3	5	2	AN3	VREF+	C1IN1+	—	DACVREF+	—	—	—	—	—	IOC	Y	—
RA4	6	3	—	—	C1OUT	OPA1IN+	—	T0CKI	—	—	—	—	IOC	Y	—
RA5	7	4	AN4	—	C2OUT	OPA1IN-	—	—	—	—	—	$\overline{SS}$	IOC	Y	—
RA6	10	7	—	—	C2OUT(1)	—	—	—	—	—	—	—	IOC	Y	OSC2/ CLKOUT
RA7	9	6	—	—	—	—	—	—	PSMC1CLK PSMC2CLK	—	—	—	IOC	Y	OSC1/ CLKIN
RB0	21	18	AN12	—	C2IN1+	—	—	—	PSMC1IN PSMC2IN	CCP1(1)	—	—	INT/ IOC	Y	—
RB1	22	19	AN10	—	C1IN3- C2IN3- C3IN3-	OPA2OUT	—	—	—	—	—	—	IOC	Y	—
RB2	23	20	AN8	—	—	OPA2IN-	—	—	—	—	—	—	IOC	Y	CLKR
RB3	24	21	AN9	—	C1IN2- C2IN2- C3IN2-	OPA2IN+	—	—	—	CCP2(1)	—	—	IOC	Y	—
RB4	25	22	AN11	—	C3IN1+	—	—	—	—	—	—	—	IOC	Y	—
RB5	26	23	AN13	—	C3OUT	—	—	T1G	—	—	—	SDO(1)	IOC	Y	—
RB6	27	24	—	—	—	—	—	—	—	—	TX(1) CK(1)	SDI(1) SDA(1)	IOC	Y	ICSPCLK
RB7	28	25	—	—	—	—	DACOUT2	—	—	—	RX(1) DT(1)	SCK(1) SCL(1)	IOC	Y	ICSPDAT
RC0	11	8	—	—	—	—	—	T1OSO T1CKI	PSMC1A	—	—	—	IOC	Y	—
RC1	12	9	—	—	—	—	—	T1OSI	PSMC1B	CCP2	—	—	IOC	Y	—
RC2	13	10	—	—	—	—	—	—	PSMC1C	CCP1	—	—	IOC	Y	—
RC3	14	11	—	—	—	—	—	—	PSMC1D	—	—	SCK SCL	IOC	Y	—
RC4	15	12	—	—	—	—	—	—	PSMC1E	—	—	SDI SDA	IOC	Y	—
RC5	16	13	—	—	—	—	—	—	PSMC1F	—	—	SDO	IOC	Y	—
RC6	17	14	—	—	—	—	—	—	PSMC2A	—	TX CK	—	IOC	Y	—
RC7	18	15	—	—	—	—	—	—	PSMC2B	—	RX DT	—	IOC	Y	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$/ VPP
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8, 19	5, 16	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Alternate pin function selected with the APFCON1 (***Register 13-1***) register.

Table of Contents

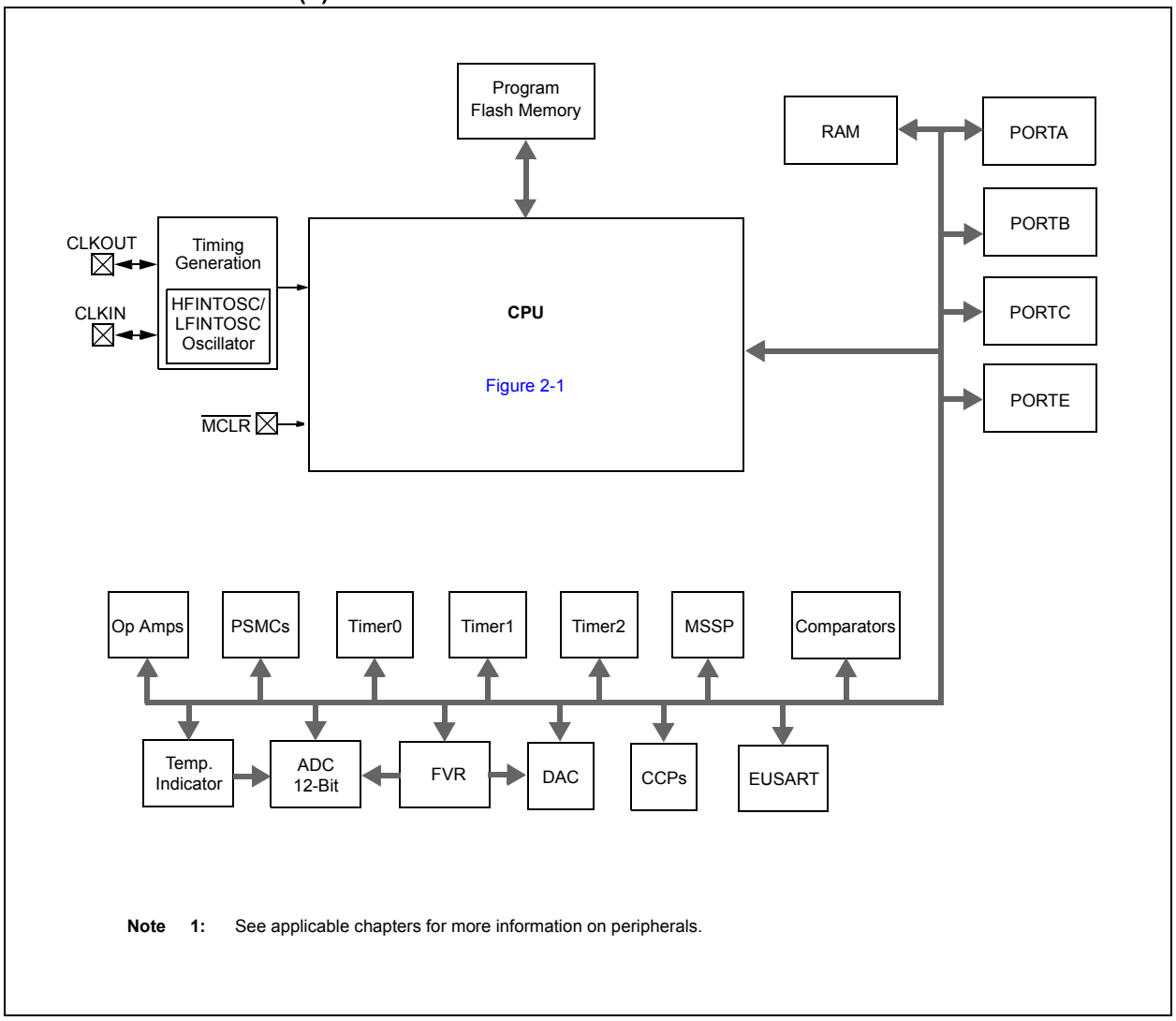
1.0 DEVICE OVERVIEW

The PIC16(L)F1782/3 are described within this data sheet. The block diagram of these devices are shown in Figure 1-1. The available peripherals are shown in Table 1-1, and the pin out descriptions are shown in Table 1-2.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1782	PIC16(L)F1783	PIC16(L)F1784	PIC16(L)F1786	PIC16(L)F1787	PIC16(L)F1788	PIC16(L)F1789
Analog-to-Digital Converter (ADC)		•	•	•	•	•	•	•
Fixed Voltage Reference (FVR)		•	•	•	•	•	•	•
Reference Clock Module		•	•	•	•	•	•	•
Temperature Indicator		•	•	•	•	•	•	•
Capture/Compare/PWM (CCP/ECCP) Modules								
	CCP1	•	•	•	•	•	•	•
	CCP2	•	•	•	•	•	•	•
	CCP3			•	•	•	•	•
Comparators								
	C1	•	•	•	•	•	•	•
	C2	•	•	•	•	•	•	•
	C3	•	•	•	•	•	•	•
	C4			•	•	•	•	•
Digital-to-Analog Converter (DAC)								
	(8-bit DAC) D1	•	•	•	•	•	•	•
	(5-bit DAC) D2							•
	(5-bit DAC) D3							•
	(5-bit DAC) D4							•
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)								
	EUSART	•	•	•	•	•	•	•
Master Synchronous Serial Ports								
	MSSP	•	•	•	•	•	•	•
Op Amp								
	Op Amp 1	•	•	•	•	•	•	•
	Op Amp 2	•	•	•	•	•	•	•
	Op Amp 3			•		•		•
Programmable Switch Mode Controller (PSMC)								
	PSMC1	•	•	•	•	•	•	•
	PSMC2	•	•	•	•	•	•	•
	PSMC3			•	•	•	•	•
	PSMC4						•	•
Timers								
	Timer0	•	•	•	•	•	•	•
	Timer1	•	•	•	•	•	•	•
	Timer2	•	•	•	•	•	•	•

FIGURE 1-1: PIC16(L)F1782/3 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1782/3 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/C3IN0-	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	C3IN0-	AN	—	Comparator C3 negative input.
RA1/AN1/C1IN1-/C2IN1-/ C3IN1-/OPA1OUT	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	C3IN1-	AN	—	Comparator C3 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
RA2/AN2/C1IN0+/C2IN0+/ C3IN0+/DACOUT1/VREF-/ DACVREF-	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	C2IN0+	AN	—	Comparator C2 positive input.
	C3IN0+	AN	—	Comparator C3 positive input.
	DACOUT1	—	AN	Digital-to-Analog Converter output.
	VREF-	AN	—	A/D Negative Voltage Reference input.
	DACVREF-	AN	—	Digital-to-Analog Converter negative reference.
RA3/AN3/VREF+/C1IN1+/ DACVREF+	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	VREF+	AN	—	A/D Voltage Reference input.
	C1IN1+	AN	—	Comparator C1 positive input.
	DACVREF+	AN	—	Digital-to-Analog Converter positive reference.
RA4/C1OUT/OPA1IN+/T0CKI	RA4	TTL/ST	CMOS	General purpose I/O.
	C1OUT	—	CMOS	Comparator C1 output.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	T0CKI	ST	—	Timer0 clock input.
RA5/AN4/C2OUT(1)/OP1INA-/ $\overline{SS}$	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	C2OUT	—	CMOS	Comparator C2 output.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	$\overline{SS}$	ST	—	Slave Select input.
RA6/C2OUT/OSC2/CLKOUT	RA6	TTL/ST	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA7/PSMC1CLK/ PSMC2CLK/OSC1/CLKIN	RA7	TTL/ST	CMOS	General purpose I/O.
	PSMC1CLK	ST	—	PSMC1 clock input.
	PSMC2CLK	ST	—	PSMC2 clock input.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	st	—	External clock input (EC mode).

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have Interrupt-on-Change functionality.

TABLE 1-2: PIC16(L)F1782/3 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB0/AN12/C2IN1+/PSMC1IN/ PSMC2IN/CCP1(1)/INT	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	A/D Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	PSMC1IN	ST	—	PSMC1 Event Trigger input.
	PSMC2IN	ST	—	PSMC2 Event Trigger input.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	INT	ST	—	External interrupt.
RB1/AN10/C1IN3-/C2IN3-/ C3IN3-/OPA2OUT	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	A/D Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	C3IN3-	AN	—	Comparator C3 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
RB2/AN8/OPA2IN-/CLKR	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	A/D Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	CLKR	—	CMOS	Clock output.
RB3/AN9/C1IN2-/C2IN2-/ C3IN2-/OPA2IN+/CCP2(1)	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	A/D Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	C3IN2-	AN	—	Comparator C3 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RB4/AN11/C3IN1+	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	A/D Channel 11 input.
	C3IN1+	AN	—	Comparator C3 positive input.
RB5/AN13/C3OUT/T1G/SDO(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	A/D Channel 13 input.
	C3OUT	—	CMOS	Comparator C3 output.
	T1G	ST	—	Timer1 gate input.
	SDO	—	CMOS	SPI data output.
RB6/TX(1)/CK(1)/SDI(1)/SDA(1)/ ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.
	ICSPCLK	ST	—	Serial Programming Clock.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have Interrupt-on-Change functionality.

TABLE 1-2: PIC16(L)F1782/3 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB7/DACOUT2/RX(1)/DT(1)/ SCK(1)/SCL(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DACOUT2	—	AN	Voltage Reference output.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C™ clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1OSO/T1CKI/PSMC1A	RC0	TTL/ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
	PSMC1A	—	CMOS	PSMC1 output A.
RC1/T1OSI/PSMC1B/CCP2(1)	RC1	TTL/ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	PSMC1B	—	CMOS	PSMC1 output B.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/PSMC1C/CCP1(1)	RC2	TTL/ST	CMOS	General purpose I/O.
	PSMC1C	—	CMOS	PSMC1 output C.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/PSMC1D/SCK(1)/SCL(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	PSMC1D	—	CMOS	PSMC1 output D.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C™ clock.
RC4/PSMC1E/SDI(1)/SDA(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	PSMC1E	—	CMOS	PSMC1 output E.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.
RC5/PSMC1F/SDO(1)	RC5	TTL/ST	CMOS	General purpose I/O.
	PSMC1F	—	CMOS	PSMC1 output F.
	SDO	—	CMOS	SPI data output.
RC6/PSMC2A/TX(1)/CK(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	PSMC2A	—	CMOS	PSMC2 output A.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
RC7/PSMC2B/RX(1)/DT(1)	RC7	TTL/ST	CMOS	General purpose I/O.
	PSMC2B	—	CMOS	PSMC2 output B.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
RE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

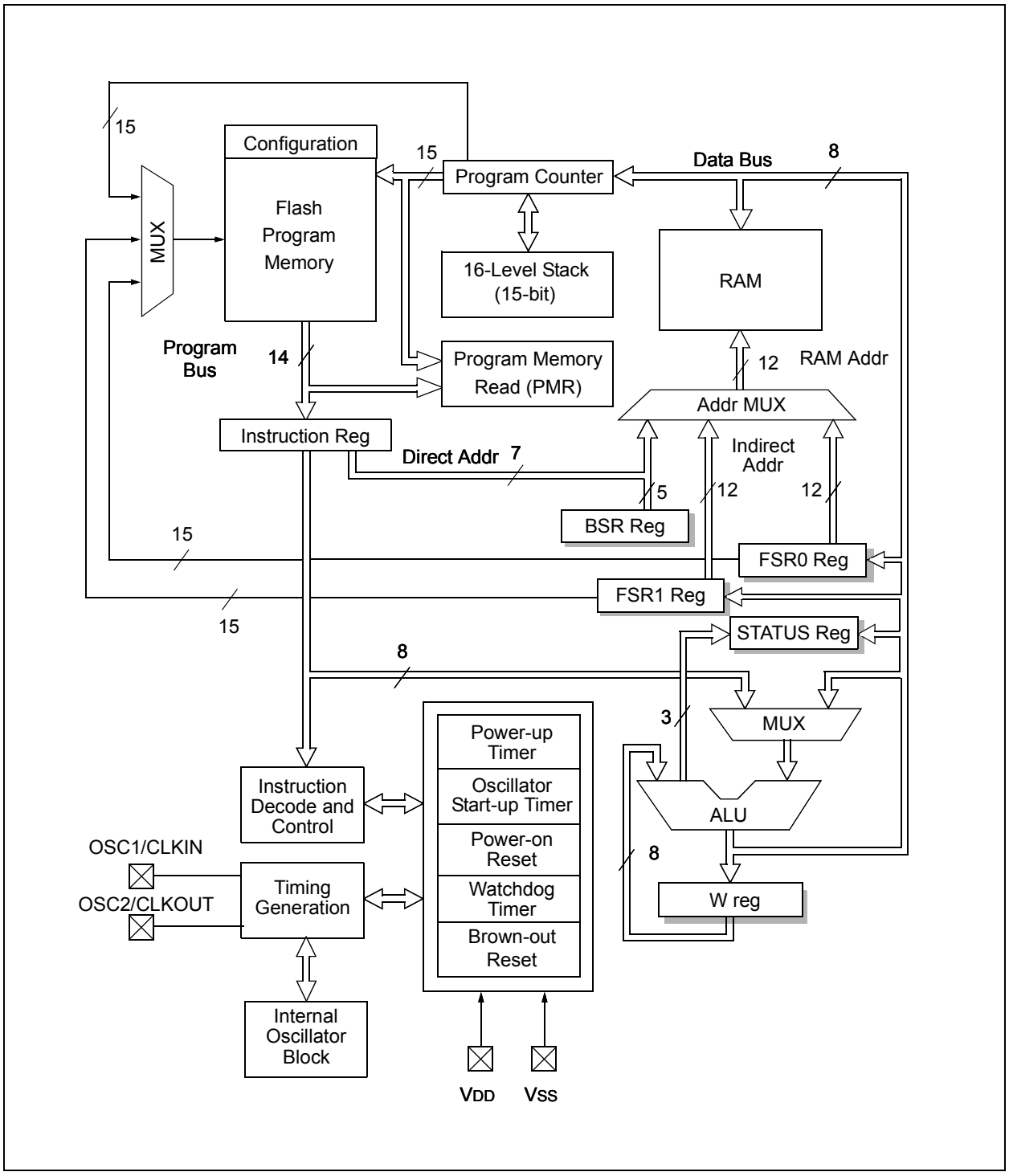
Note 1: Pin functions can be assigned to one of two locations via software. See ***Register 13-1***.
2: All pins have Interrupt-on-Change functionality.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **8.5 "Automatic Context Saving"**, for more information.

2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See **Section 3.5 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.6 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 29.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
- Data EEPROM memory(1)

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in **Section 12.0 "Data EEPROM and Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1782/3 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1 and 3-2).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
PIC16(L)F1782	2,048	07FFh
PIC16(L)F1783	4,096	0FFFh

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1782

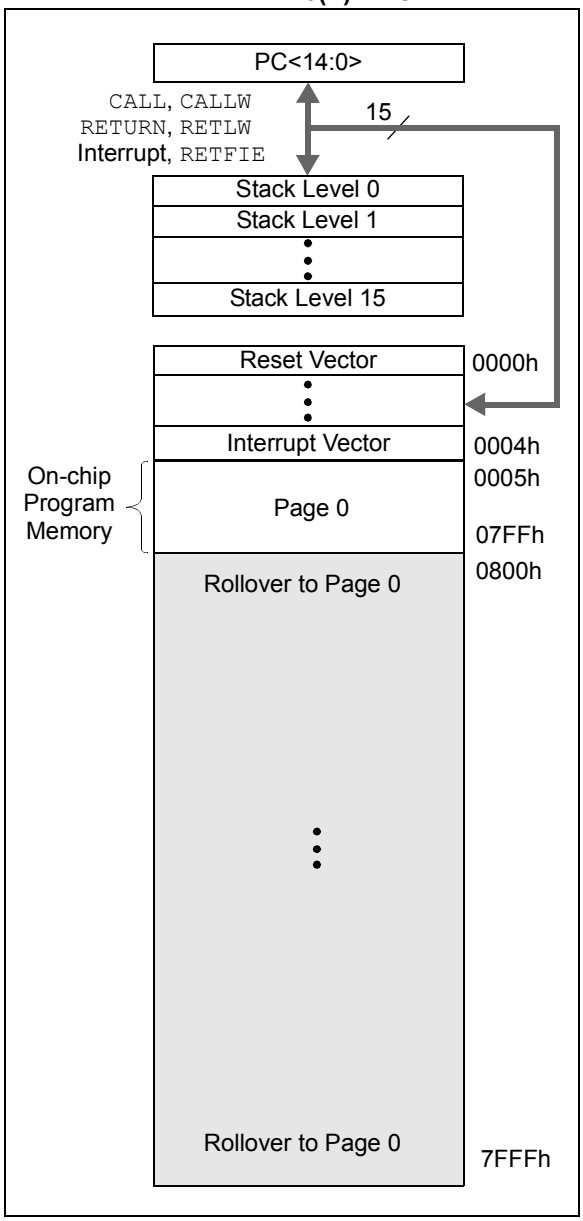
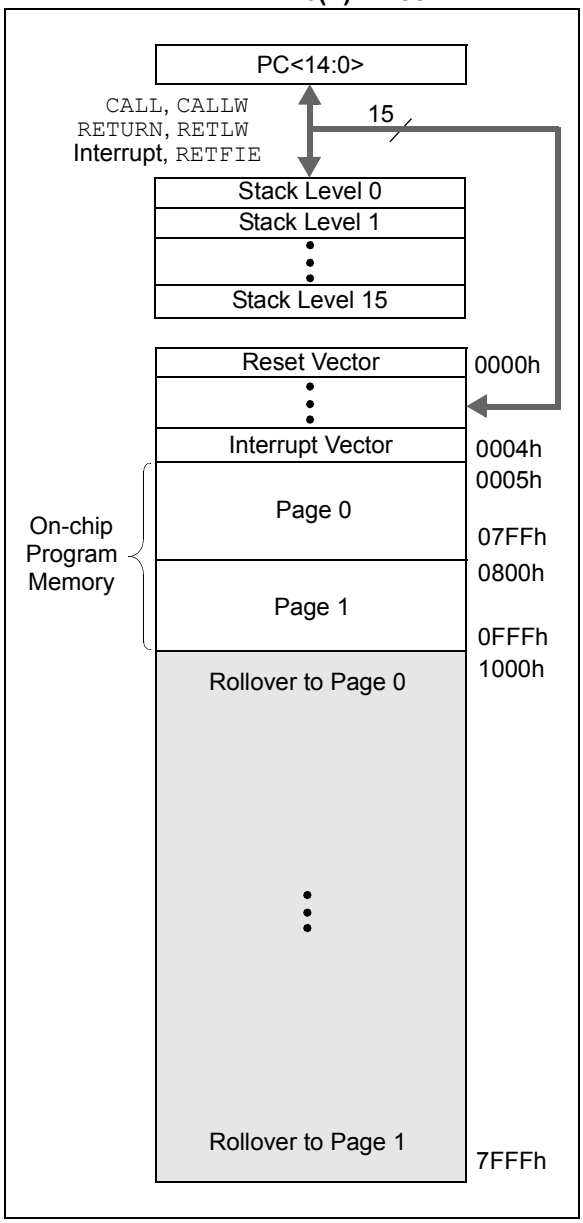


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1783



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The high directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.6 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper 5 bits of the address define the Bank address and the lower 7 bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-7.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 29.0 "Instruction Set Summary"**).

Note:	The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

3.3 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

3.3.1 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.3.2 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

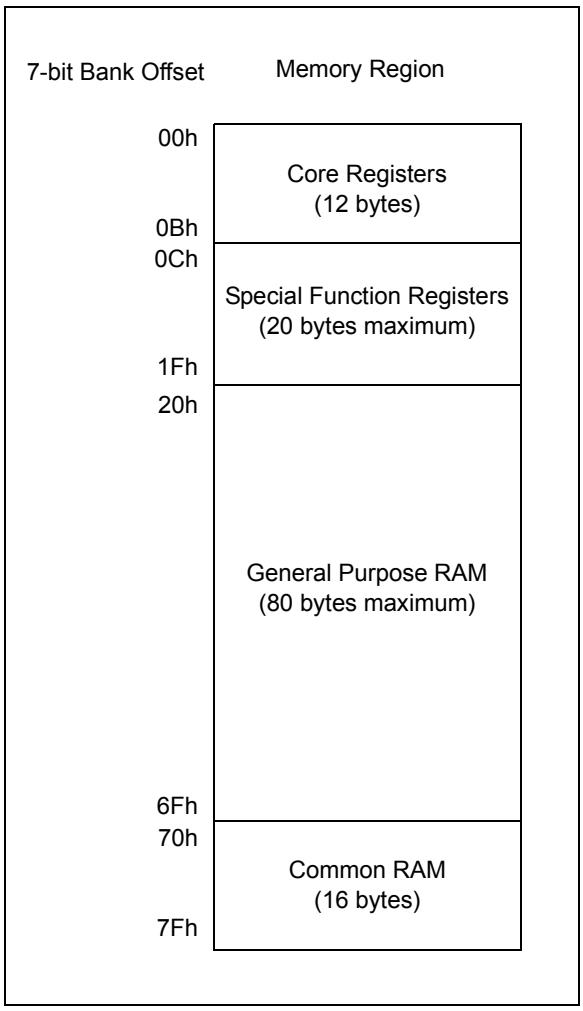
3.3.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.6.2 "Linear Data Memory"** for more information.

3.3.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.3.4 DEVICE MEMORY MAPS

The memory maps for Bank 0 through Bank 31 are shown in the tables in this section.

TABLE 3-3: PIC16(L)F1782/3 MEMORY MAP (BANKS 0-7)

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	—	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	—	190h	—	210h	WPUE	290h	—	310h	—	390h	INLVLE
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	EEADRL	211h	SSP1BUF	291h	CCPR1L	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	EEADRH	212h	SSP1ADD	292h	CCPR1H	312h	—	392h	IOCAN
013h	—	093h	—	113h	CM2CON0	193h	EEDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	PIR4	094h	PIE4	114h	CM2CON1	194h	EEDATH	214h	SSP1STAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	EECON1	215h	SSP1CON1	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	SSP1CON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON(2)	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DACCON0	198h	—	218h	—	298h	CCPR2L	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	RCREG	219h	—	299h	CCPR2H	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TXREG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	—	19Bh	SPBRG	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SPBRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON	19Dh	RCSTA	21Dh	—	29Dh	—	31Dh	—	39Dh	IOCEP
01Eh	—	09Eh	ADCON1	11Eh	CM3CON0	19Eh	TXSTA	21Eh	—	29Eh	—	31Eh	—	39Eh	IOCEN
01Fh	—	09Fh	ADCON2	11Fh	CM3CON1	19Fh	BAUDCON	21Fh	—	29Fh	—	31Fh	—	39Fh	IOCEF
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes(1)	220h	General Purpose Register 80 Bytes(1)	2A0h	General Purpose Register 80 Bytes(1)	320h	General Purpose Register 16 Bytes(1)	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		32Fh		3EFh	
070h	Common RAM 70h – 7Fh	0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	330h	Unimplemented Read as '0'	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		36Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16(L)F1783 only.
2: PIC16F1782/3 only.

TABLE 3-4: PIC16(L)F1782/3 MEMORY MAP (BANKS 8-31)

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	Unimplemented Read as '0'	48Ch	Unimplemented Read as '0'	50Ch	Unimplemented Read as '0'	58Ch	Unimplemented Read as '0'	60Ch	Unimplemented Read as '0'	68Ch	Unimplemented Read as '0'	70Ch	Unimplemented Read as '0'	78Ch	Unimplemented Read as '0'
				510h											
				511h	OPA1CON										
				512h	—										
				513h	OPA2CON										
				514h	Unimplemented Read as '0'										
				519h											
				51Ah	CLKRCON										
				51Bh	Unimplemented Read as '0'										
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
470h	Common RAM (Accesses 70h – 7Fh)	4F0h	Common RAM (Accesses 70h – 7Fh)	570h	Common RAM (Accesses 70h – 7Fh)	5F0h	Common RAM (Accesses 70h – 7Fh)	670h	Common RAM (Accesses 70h – 7Fh)	6F0h	Common RAM (Accesses 70h – 7Fh)	770h	Common RAM (Accesses 70h – 7Fh)	7F0h	Common RAM (Accesses 70h – 7Fh)
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	See Table 3-5	88Ch	Unimplemented Read as '0'	90Ch	Unimplemented Read as '0'	98Ch	Unimplemented Read as '0'	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Common RAM (Accesses 70h – 7Fh)	8F0h	Common RAM (Accesses 70h – 7Fh)	970h	Common RAM (Accesses 70h – 7Fh)	9F0h	Common RAM (Accesses 70h – 7Fh)	A70h	Common RAM (Accesses 70h – 7Fh)	AF0h	Common RAM (Accesses 70h – 7Fh)	B70h	Common RAM (Accesses 70h – 7Fh)	BF0h	Common RAM (Accesses 70h – 7Fh)
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh		F8Bh	
C0Ch	Unimplemented Read as '0'	C8Ch	Unimplemented Read as '0'	D0Ch	Unimplemented Read as '0'	D8Ch	Unimplemented Read as '0'	E0Ch	Unimplemented Read as '0'	E8Ch	Unimplemented Read as '0'	F0Ch	Unimplemented Read as '0'	F8Ch	See Table 3-6
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh		FEFh	
C70h	Common RAM (Accesses 70h – 7Fh)	CF0h	Common RAM (Accesses 70h – 7Fh)	D70h	Common RAM (Accesses 70h – 7Fh)	DF0h	Common RAM (Accesses 70h – 7Fh)	E70h	Common RAM (Accesses 70h – 7Fh)	EF0h	Common RAM (Accesses 70h – 7Fh)	F70h	Common RAM (Accesses 70h – 7Fh)	FF0h	Common RAM (Accesses 70h – 7Fh)
C7Fh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FFFh	

Legend: = Unimplemented data memory locations, read as '0'

TABLE 3-5: PIC16(L)F1782/3 MEMORY MAP (BANK 16 DETAILS)

	BANK 16		BANK 16
811h	PSMC1CON	831h	PSMC2CON
812h	PSMC1MDL	832h	PSMC2MDL
813h	PSMC1SYNC	833h	PSMC2SYNC
814h	PSMC1CLK	834h	PSMC2CLK
815h	PSMC1OEN	835h	PSMC2OEN
816h	PSMC1POL	836h	PSMC2POL
817h	PSMC1BLNK	837h	PSMC2BLNK
818h	PSMC1REBS	838h	PSMC2REBS
819h	PSMC1FEBS	839h	PSMC2FEBS
81Ah	PSMC1PHS	83Ah	PSMC2PHS
81Bh	PSMC1DCS	83Bh	PSMC2DCS
81Ch	PSMC1PRS	83Ch	PSMC2PRS
81Dh	PSMC1ASDC	83Dh	PSMC2ASDC
81Eh	PSMC1ASDD	83Eh	PSMC2ASDD
81Fh	PSMC1ASDS	83Fh	PSMC2ASDS
820h	PSMC1INT	840h	PSMC2INT
821h	PSMC1PHL	841h	PSMC2PHL
822h	PSMC1PHH	842h	PSMC2PHH
823h	PSMC1DCL	843h	PSMC2DCL
824h	PSMC1DCH	844h	PSMC2DCH
825h	PSMC1PRL	845h	PSMC2PRL
826h	PSMC1PRH	846h	PSMC2PRH
827h	PSMC1TMRL	847h	PSMC2TMRL
828h	PSMC1TMRH	848h	PSMC2TMRH
829h	PSMC1DBR	849h	PSMC2DBR
82Ah	PSMC1DBF	84Ah	PSMC2DBF
82Bh	PSMC1BLKR	84Bh	PSMC2BLKR
82Ch	PSMC1BLKF	84Ch	PSMC2BLKF
82Dh	PSMC1FFA	84Dh	PSMC1FFA
82Eh	PSMC1STR0	84Eh	PSMC2STR0
82Fh	PSMC1STR1	84Fh	PSMC2STR1
830h	—	840h	Unimplemented Read as '0'
		86Fh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-6: PIC16(L)F1782/3 MEMORY MAP (BANK 31 DETAILS)

	BANK 31
F8Ch	Unimplemented Read as '0'
FE3h	
FE4h	STATUS_SHAD
FE5h	WREG_SHAD
FE6h	BSR_SHAD
FE7h	PCLATH_SHAD
FE8h	FSR0L_SHAD
FE9h	FSR0H_SHAD
FEAh	FSR1L_SHAD
FEBh	FSR1H_SHAD
FECh	—
FEDh	STKPTR
FEEh	TOSL
FEFh	TOSH

Legend: = Unimplemented data memory locations, read as '0'.

3.3.5 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-7 can be addressed from any Bank.

TABLE 3-7: CORE FUNCTION REGISTERS SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0-31											
x00h or x80h	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x01h or x81h	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x02h or x82h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h or x86h	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h or x88h	BSR	—	—	—	BSR4	BSR3	BSR2	BSR1	BSR0	---0 0000	---0 0000
x09h or x89h	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0											
00Ch	PORTA	PORTA Data Latch when written: PORTA pins when read								xxxx xxxx	uuuu uuuu
00Dh	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
00Eh	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
00Fh	—	Unimplemented								—	—
010h	PORTE	—	—	—	—	RE3	—	—	—	---- x---	---- u---
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
012h	PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	C3IF	CCP2IF	0000 0-00	0000 0-00
013h	—	Unimplemented								—	—
014h	PIR4	—	—	PSMC2TIF	PSMC1TIF	—	—	PSMC2SIF	PSMC1SIF	--00 --00	--00 --00
015h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
016h	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
017h	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
018h	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		0000 0x00	uuuu uxuu
016h	TMR2	Holding Register for the Least Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
017h	PR2	Holding Register for the Most Significant Byte of the 16-bit TMR2 Register								xxxx xxxx	uuuu uuuu
018h	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
01Dh to 01Fh	—	Unimplemented								—	—
Bank 1											
08Ch	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
08Dh	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
08Eh	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
08Fh	—	Unimplemented								—	—
090h	TRISE	—	—	—	—	—(2)	—	—	—	---- 1---	---- 1---
091h	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
092h	PIE2	OSEIE	C2IE	C1IE	EEIE	BCL1IE	—	C3IE	CCP2IE	0000 0-00	0000 0-00
093h	—	Unimplemented								—	—
094h	PIE4	—	—	PSMC2TIE	PSMC1TIE	—	—	PSMC2SIE	PSMC1SIE	--00 --00	--00 --00
095h	OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	00-1 11qq	qq-q qquu
097h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	--01 0110	--01 0110
098h	OSCTUNE	—	—	TUN<5:0>						--00 0000	--00 0000
099h	OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		0011 1-00	0011 1-00
09Ah	OSCSTAT	T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	00q0 --00	qqqq --0q
09Bh	ADRESL	A/D Result Register Low								xxxx xxxx	uuuu uuuu
09Ch	ADRESH	A/D Result Register High								xxxx xxxx	uuuu uuuu
09Dh	ADCON0	ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
09Eh	ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		0000 -000	0000 -000
09Fh	ADCON2	TRIGSEL<3:0>				CHSN<3:0>				000- -000	000- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16F1782/3 only.

TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 2											
10Ch	LATA	PORTA Data Latch								xxxx xxxx	uuuu uuuu
10Dh	LATB	PORTB Data Latch								xxxx xxxx	uuuu uuuu
10Eh	LATC	PORTC Data Latch								xxxx xxxx	uuuu uuuu
10Fh	—	Unimplemented								—	—
110h	—	Unimplemented								—	—
111h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1ZLF	C1SP	C1HYS	C1SYNC	0000 0100	0000 0100
112h	CM1CON1	C1INTP	C1INTN	C1PCH<2:0>			C1NCH<2:0>			0000 0000	0000 0000
113h	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2ZLF	C2SP	C2HYS	C2SYNC	0000 0100	0000 0100
114h	CM2CON1	C2INTP	C2INTN	C2PCH<2:0>			C2NCH<2:0>			0000 0000	0000 0000
115h	CMOUT	—	—	—	—	—	MC3OUT	MC2OUT	MC1OUT	---- -000	---- -000
116h	BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	1x-- ---q	uu-- ---u
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		0q00 0000	0q00 0000
118h	DACCON0	DACEN	—	DACOE1	DACOE2	DACPSS<1:0>		—	DACNSS	0-00 00-0	0-00 00-0
119h	DACCON1	DACR<7:0>								0000 0000	0000 0000
11Ah to 11Ch	—	Unimplemented								—	—
11Dh	APFCON	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	0000 0000	0000 0000
11Eh	CM3CON0	C3ON	C3OUT	C3OE	C3POL	C3ZLF	C3SP	C3HYS	C3SYNC	0000 0100	0000 0100
11Fh	CM3CON1	C3INTP	C3INTN	C3PCH<2:0>			C3NCH<2:0>			0000 0000	0000 0000
Bank 3											
18Ch	ANSELA	ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	1-11 1111	1-11 1111
18Dh	ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	--11 1111
18Eh to 190h	—	Unimplemented								—	—
191h	EEADRL	EEPROM / Program Memory Address Register Low Byte								0000 0000	0000 0000
192h	EEADRH	—(2)	EEPROM / Program Memory Address Register High Byte							1000 0000	1000 0000
193h	EEDATL	EEPROM / Program Memory Read Data Register Low Byte								xxxx xxxx	uuuu uuuu
194h	EEDATH	—	—	EEPROM / Program Memory Read Data Register High Byte						--xx xxxx	--uu uuuu
195h	EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	0000 x000	0000 q000
196h	EECON2	EEPROM / Program Memory Control Register 2								0000 0000	0000 0000
197h	VREGCON(3)	—	—	—	—	—	—	VREGPM	Reserved	---- --01	---- --01
198h	—	Unimplemented								—	—
199h	RCREG	USART Receive Data Register								0000 0000	0000 0000
19Ah	TXREG	USART Transmit Data Register								0000 0000	0000 0000
19Bh	SPBRG	BRG<7:0>								0000 0000	0000 0000
19Ch	SPBRGH	BRG<15:8>								0000 0000	0000 0000
19Dh	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
19Eh	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
19Fh	BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Unimplemented, read as '1'.

3: PIC16F1782/3 only.