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PIC16(L)F18426/46

14/20-Pin Full-Featured, Low Pin Count Microcontrollers with XLP

Description

PIC16(L)F184XX microcontrollers feature Intelligent Analog, Core Independent Peripherals (CIPs) and communication peripherals combined with eXtreme Low-Power (XLP) for a wide range of general purpose and low-power applications. Features such as a 12-bit Analog-to-Digital Converter with Computation (ADC^2), Memory Access Partitioning (MAP), the Device Information Area (DIA), Power-saving operating modes, and Peripheral Pin Select (PPS), offer flexible solutions for a wide variety of custom applications.

Core Features

- C Compiler Optimized RISC Architecture
- Only 50 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - Up to two 24-bit timers
  - Up to four 8-bit timers
  - Up to four 16-bit timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - Configurable in hardware (Configuration Words) and/or software
- Programmable Code Protection

Memory

- Up to 28 KB Program Flash Memory
- Up to 2 KB Data SRAM Memory

- 256B Data EEPROM
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Write-protect
  - Customizable partition
- Device Information Area (DIA)
- Device Configuration Information (DCI)

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF184XX)
  - 2.3V to 5.5V (PIC16F184XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Operation Modes

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Extreme Low-Power mode (XLP)
  - Sleep: 500 nA typical @ 1.8V
  - Sleep and Watchdog Timer: 900 nA typical @ 1.8V

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals

- Configurable Logic Cell (CLC):
  - 4 CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - 2 CWGs

  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules:
  - 4 CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Pulse-Width Modulators (PWM):
  - 2 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock: 0 Hz < f_{NCO} < 32 MHz
  - Resolution: $f_{NCO}/2^{20}$
- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Serial Communications:
  - EUSART
    - 1 EUSART(s)
    - RS-232, RS-485, LIN compatible
    - Auto-Baud Detect, Auto-wake-up on Start.
  - Master Synchronous Serial Port (MSSP)
    - 2 MSSP(s)
    - SPI
    - I^2C, SMBus and PMBus™ compatible
- Data Signal Modulator (DSM)
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms
- Up to 18 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable
- Timer modules:
  - Timer0:
    - 8/16-bit timer/counter
    - Synchronous or asynchronous operation
    - Programmable prescaler/postscaler
    - Time base for capture/compare function
  - Timer1/3/5 with gate control:
    - 16-bit timer/counter
    - Programmable internal or external clock sources
    - Multiple gate sources

        - Multiple gate modes
        - Time base for capture/compare function
    - Timer2/4/6 with Hardware Limit Timer:
        - 8-bit timers
        - Programmable prescaler/postscaler
        - Time base for PWM function
        - Hardware Limit (HLT) and one-shot extensions
        - Selectable clock sources
    - Signal Measurement Timer (SMT)
        - 1 SMT(s)
        - 24-bit timer/counter with programmable prescaler

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC^2):
    - 12-bit with up to 17 external channels
    - Conversion available during Sleep
    - Automated post-processing
    - Automated math functions on input signals:
        - Averaging, filter calculations, oversampling and threshold comparison
    - Integrated charge pump for low-voltage operation
    - CVD support
- Zero-Cross Detect (ZCD):
    - AC high voltage zero-crossing detection for simplifying TRIAC control
    - Synchronized switching control and timing
- Temperature Sensor Circuit
- Comparator:
    - 2 Comparators
    - Fixed Voltage Reference at (non)inverting input(s)
    - Comparator outputs externally accessible
- Digital-to-Analog Converter (DAC):
    - 5-bit resolution, rail-to-rail
    - Positive Reference Selection
    - Unbuffered I/O pin output
    - Internal connections to ADCs and comparators
- Fixed Voltage Reference (FVR) module:
    - 1.024V, 2.048V and 4.096V output levels

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
    - Software-selectable frequency range up to 32 MHz
    - ±2% at calibration (nominal)
- 4x PLL for use with external sources
    - up to 32 MHz (4-8 MHz input)

- 2x PLL for use with the HFINTOSC
  - up to 32 MHz
- Low-Power Internal 31 kHz Oscillator (LFINTOSC)
- External 32.768 kHz Crystal Oscillator (SOCS)
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 32 MHz
  - Fail-Safe Clock Monitor
    - Detects clock source failure
  - Oscillator Start-up Timer (OST)
    - Ensures stability of crystal oscillator sources

PIC16(L)F184XX Family Types

Table 1. Devices Included In This Data Sheet

Device	Program Flash Memory (Words)	Program Flash Memory (Kbytes)	Data Memory (EEPROM) (bytes)	Data SRAM (bytes)	I/O's(2)	12-bit ADC^2 (ch)	5-bit DAC	Comparators	CWG	Clock Ref	Timers (8/16-bit)	CCP	PWM	NCO	EUSART	MSSP (I^2C/SPI)	CLC	DSM	PPS	XLP	PMD	Windowed Watchdog Timer	Memory Access Partition	Device Information Area	Debug(1)
PIC16(L)F18426	16384	28	256	2048	12	11	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18446	16384	28	256	2048	18	17	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I

Note:

1. I - Debugging integrated on-chip.
2. One pin is input-only.

Table 2. Devices Not Included In This Data Sheet

Device	Program Flash Memory (Words)	Program Flash Memory (Kbytes)	Data Memory (EEPROM) (bytes)	Data SRAM (bytes)	I/O's(2)	12-bit ADC2 (ch)	5-bit DAC	Comparators	CWG	Clock Ref	Timers (8/16-bit)	CCP	PWM	NCO	EUSART	MSSP (I2C/SPI)	CLC	DSM	PPS	XLP	PMD	Windowed Watchdog Timer	Memory Access Partition	Device Information Area	Debug(1)
PIC16(L)F18424	4096	7	256	512	12	11	1	2	2	1	4/4	4	2	1	1	1	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18425	8192	14	256	1024	12	11	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18444	4096	7	256	512	18	17	1	2	2	1	4/4	4	2	1	1	1	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18445	8192	14	256	1024	18	17	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18455	8192	14	256	1024	26	24	1	2	2	1	4/4	5	2	1	2	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18456	16384	28	256	2048	26	24	1	2	2	1	4/4	5	2	1	2	2	4	1	Y	Y	Y	Y	Y	Y	I

Data Sheet Index:

1. DS40001985 Data Sheet, 14/20-Pin Full-Featured, Low Pin Count Microcontrollers with XLP
2. DS(TBD) Data Sheet, 14/20-Pin Full-Featured, Low Pin Count Microcontrollers with XLP
3. DS(TBD) Data Sheet, 28-Pin Full-Featured, Low Pin Count Microcontrollers with XLP

Packages

Packages	PDIP	SOIC	SSOP	TSSOP	UQFN (4x4)
PIC16(L)F18426	•	•		•	•
PIC16(L)F18446	•	•	•		•

Note: Pin details are subject to change.

Important: For other small form-factor package availability and marking information, visit www.microchip.com/ packaging or contact your local sales office.

Pin Diagrams

1 14/16-Pin Diagrams

Figure 1. 14-Pin PDIP, SOIC, TSSOP

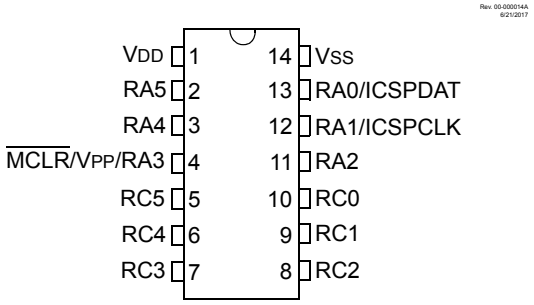
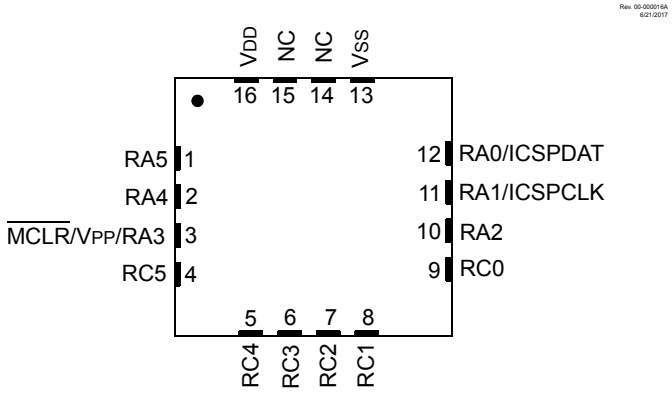


Figure 2. 16-Pin UQFN (4x4)



Note: It is recommended that the exposed bottom pad be connected to V_{SS}.

Related Links

14/16-Pin Allocation Table

2 20-Pin Diagrams

Figure 3. 20-Pin PDIP, SOIC, SSOP

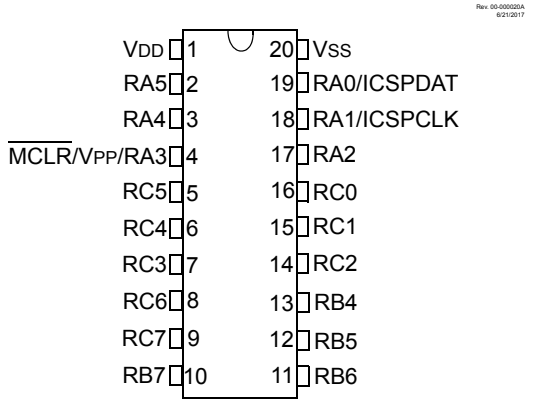
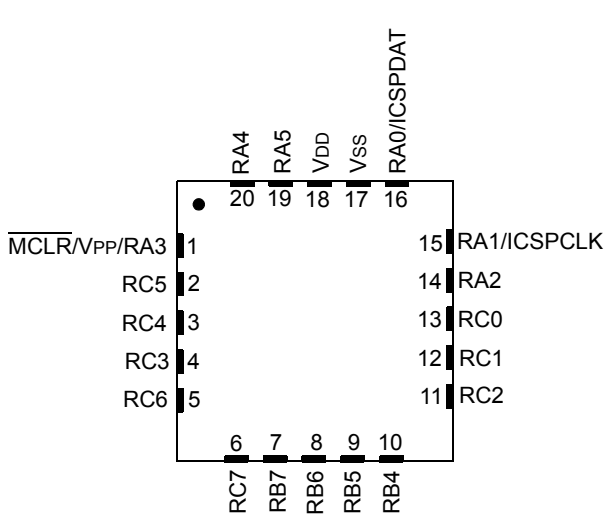


Figure 4. 20-Pin UQFN (4x4)



Note: It is recommended that the exposed bottom pad be connected to V_{SS}.

Related Links

20-Pin Allocation Table

Pin Allocation Tables

1 14/16-Pin Allocation Table

I/O	14-pin PDIP/SOIC/TSSOP	16-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT1	MDSRC(1)	—	—	—	—	SS2(1)	—	—	—	—	IOCA0	Y	ICDDAT ICSPDAT
RA1	12	11	ANA1	ADCVREF+	C1IN0 C2IN0-	—	DAC1VREF+	—	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK ICSPCLK
RA2	11	10	ANA2	ADCVREF-	—	—	DAC1VREF-	—	T0CKI(1)	CCP3IN(1)	—	CWG1IN(1) CWG2IN(1)	—	ZCD1	—	—	—	IOCA2	Y	INT(1)
RA3	4	3	—	—	—	—	—	—	T6IN(1)	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SMT1WIN(1)	—	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT SOSCO OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) T2IN(1) SMT1SIG(1)	—	—	—	—	—	—	CLCIN3(1)	—	IOCA5	Y	CLKIN SOSCI OSC1

I/O	14-pin PDIP/SOIC/TSSOP	16-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI(1)	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	T4IN(1)	CCP4IN(1)	—	—	SDI1(1) SDA1(1,3,4)	—	—	CLCIN2(1)	—	IOCC1	Y	—
RC2	8	7	ANC2 ADACT(1)	—	C1IN2- C2IN2-	—	—	MDCARL(1)	—	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	—	T5G(1)	CCP2IN(1)	—	—	$\overline{SS1}$(1)	—	—	CLCIN0(1)	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	SCK2(1,5) SCL2(1,3,4,5)	—	CK1(1,3)	CLCIN1(1)	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCARH(1)	T3CKI(1)	CCP1IN(1)	—	—	SDI2(1,5) SDA2(1,3,4,5)	—	RX1(1) DT1(1,3)	—	—	IOCC5	Y	—
V_{DD}	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADCGRDA	—	C1OUT	NCO1OUT	—	DSM1OUT	TMR0OUT	CCP1OUT	PWM6OUT	CWG1A CWG2A	SDO1 SDO2	—	DT1(3)	CLC1OUT	CLKR	—	—	—
	—	—	ADCGRDB	—	C2OUT	—	—	—	—	CCP2OUT	PWM7OUT	CWG1B CWG2B	SCK1 SCK2	—	CK1(3)	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3OUT	—	CWG1C CWG2C	SCL1(3) SCL2(3)	—	TX1	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4OUT	—	CWG1D CWG2D	SDA1(3) SDA2(3)	—	—	CLC4OUT	—	—	—	—

Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins may be configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.
5. MSSP2 is not available on the PIC16(L)F18424 or PIC16(L)F18444 devices.

2 20-Pin Allocation Table

I/O	20-pin PDIP/SOIC/TSSOP	20-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	ADCVREF+	C1IN0- C2IN0-	—	DAC1VREF+	MDSRC(1)	—	—	—	—	$\overline{SS2}$(1)	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	ADCVREF-	—	—	DAC1VREF-	—	T0CKI(1)	—	—	CWG1IN(1) CWG2IN(1)	—	ZCD1	—	CLCIN0(1)	—	IOCA2	Y	INT(1)
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ V_{PP}
RA4	3	20	ANA4	—	—	—	—	—	T1G(1) SMT1WIN(1)	CCP4IN(1)	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT SOSCO OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI(1) T2IN(1) SMT1SIG(1)	—	—	—	—	—	—	—	—	IOCA5	Y	CLKIN SOSCI OSC1
RB4	13	10	ANB4	—	—	—	—	—	T5G(1)	—	—	—	SDI1(1) SDA1(1,3,4)	—	—	CLCIN2(1)	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	CCP3IN(1)	—	—	SCK2(1,5) SCL2(1,3,4,5)	—	RX1(1) DT1(1,3)	CLCIN3(1)	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	T6IN(1)	—	—	—	SDI2(1,5) SDA2(1,3,4,5)	—	CK1(1,3)	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	T3CKI(1) T3G(1)	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2-	—	—	MDCARL(1)	T5CKI(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—

I/O	20-pin PDIP/SOIC/TSSOP	20-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
			ADACT(1)		C2IN2-															
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	—	—	CCP2IN(1)	—	—	—	—	—	CLCIN1(1)	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCARH(1)	T4IN(1)	CCP1IN(1)	—	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	$\overline{SS1}$(1)	—	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
V_{DD}	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADCGRDA	—	C1OUT	NCO1OUT	—	DSM1OUT	TMR0OUT	CCP1OUT	PWM6OUT	CWG1A CWG2A	SDO1 SDO2	—	DT1(3)	CLC1OUT	CLKR	—	—	—
	—	—	ADCGRDB	—	C2OUT	—	—	—	—	CCP2OUT	PWM7OUT	CWG1B CWG2B	SCK1 SCK2	—	CK1(3)	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3OUT	—	CWG1C CWG2C	SCL1(3) SCL2(3)	—	TX1	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4OUT	—	CWG1D CWG2D	SDA1(3) SDA2(3)	—	—	CLC4OUT	—	—	—	—

Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins may be configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.
5. MSSP2 is not available on the PIC16(L)F18424 or PIC16(L)F18444 devices.

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1. Device Overview

This document contains device specific information for the following devices:

• PIC16F18426	• PIC16LF18426
• PIC16F18446	• PIC16LF18446

1.1 New Core Features

1.1.1 XLP Technology

All of the devices in the PIC16(L)F184XX family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the secondary oscillator or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Peripheral Module Disable:** Modules that are not being used in the code can be selectively disabled using the PMD module. This further reduces the power consumption.

1.1.2 Multiple Oscillator Options and Features

All of the devices in the PIC16(L)F184XX family offer several different oscillator options. The PIC16(L)F184XX family can be clocked from several different sources:

- HFINTOSC
  - 1-32 MHz precision digitally controlled internal oscillator
- LFINTOSC
  - 31 kHz internal oscillator
- EXTOSC
  - External clock (EC)
  - Low-power oscillator (LP)
  - Medium-power oscillator (XT)
  - High-power oscillator (HS)
- SOSC
  - Secondary oscillator circuit optimized for 32 kHz clock crystals
- A Phase Lock Loop (PLL) frequency multiplier (2x/4x) is available to the External Oscillator modes enabling clock speeds of up to 32 MHz
- Fail-Safe Clock Monitor: This option constantly monitors the main clock source against a reference signal provided by the LFINTOSC. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.

1.2 Other Special Features

- 12-bit A/D Converter with Computation: This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead. It has a new module called ADC^2 with computation features, which provides a digital filter and threshold interrupt functions.
- Memory Endurance: The Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 10K for program memory and 100K for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- Self-programmability: These devices can write to their own program memory spaces under internal software control. By using a boot loader routine located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- Enhanced Peripheral Pin Select: The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections. All analog inputs and outputs remain fixed to their assigned pins.
- Windowed Watchdog Timer (WWDT):
  - Timer monitoring of overflow and underflow events
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software

1.3 Details on Individual Family Members

The devices of the PIC16(L)F184XX family described in the current datasheet are available in 14/20-pin packages. The block diagram for this device is shown in Figure 1-1.

The devices have the following differences:

1. Program Flash Memory
2. Data Memory SRAM
3. Data Memory EEPROM
4. A/D channels
5. I/O ports
6. Enhanced USART
7. Input Voltage Range/Power Consumption

All other features for devices in this family are identical. These are summarized in the following Device Features table.

The pinouts for all devices are listed in the pin summary tables.

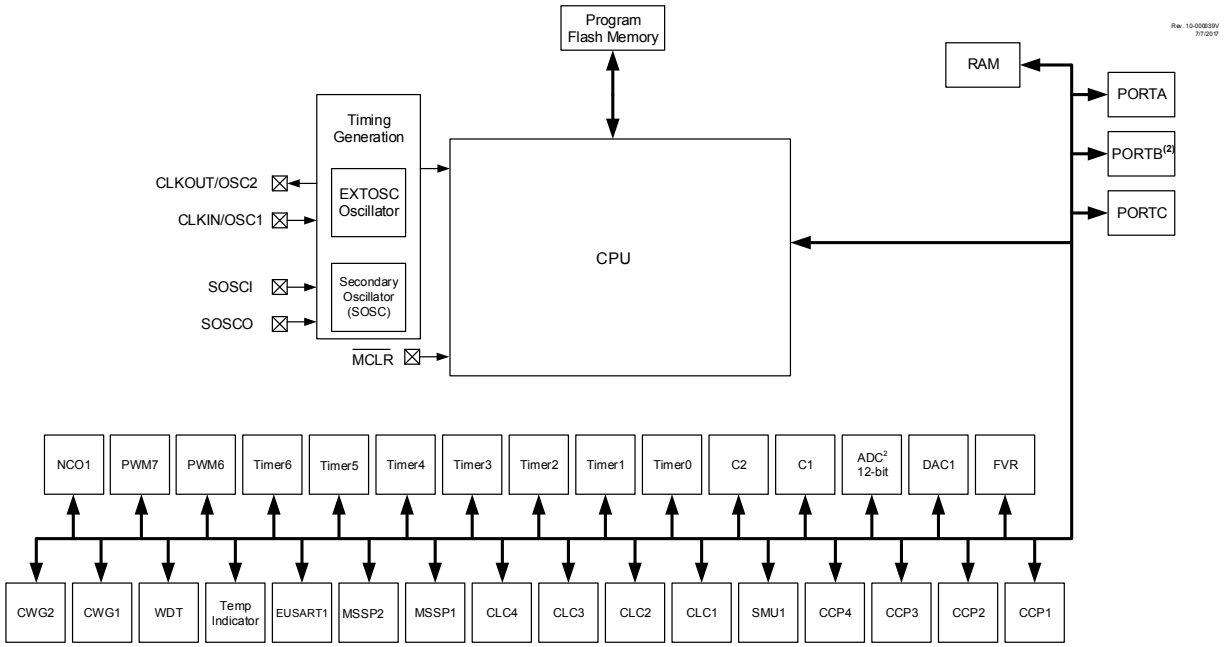
Table 1-1. Device Features

Features	PIC16(L)F18426	PIC16(L)F18446
Program Memory (KBytes)	28	28
Program Memory (Instructions)	16384	16384
Data Memory (Bytes)	2048	2048
Data EEPROM Memory (Bytes)	256	256

Features	PIC16(L)F18426	PIC16(L)F18446
Packages	14 - PDIP 14 - SOIC (3.9 mm) 14 - TSSOP 16 - uQFN (4x4)	20 - PDIP 20 - SOIC (7.5 mm) 20 - SSOP 20 - uQFN (4x4)
I/O Ports	A, C	A, B, C
Capture/Compare/PWM Modules (CCP)	4	4
Configurable Logic Cell (CLC)	4	4
10-Bit Pulse-Width Modulator (PWM)	2	2
12-Bit Analog-to-Digital Module (ADC^2) with Computation Accelerator	11 channels	17 channels
5-Bit Digital-to-Analog Module (DAC)	1	1
Comparators	2	2
Numerical Contolled Oscillator (NCO)	1	1
Interrupt Sources	40	40
Timers (16-/8-bit)	4	4
Serial Communications	2 MSSP 1 EUSART	2 MSSP 1 EUSART
Complementary Waveform Generator (CWG)	2	2
Zero-Cross Detect (ZCD)	1	1
Data Signal Modulator (DSM)	1	1
Reference Clock Output Module	1	1
Peripheral Pin Select (PPS)	YES	YES
Peripheral Module Disable (PMD)	YES	YES
Programmable Brown-out Reset (BOR)	YES	YES
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT
Instruction Set	50 instructions	50 instructions

Features	PIC16(L)F18426	PIC16(L)F18446
	16-levels hardware stack	16-levels hardware stack
Operating Frequency	DC – 32 MHz	DC – 32 MHz

Figure 1-1. PIC16(L)F18426/46 Device Block Diagram



Note:

1. See applicable chapters for more information on peripherals.
2. PORTB available only on 20-pin or higher pin-count devices.

1.4 Register and Bit naming conventions

1.4.1 Register Names

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an ‘x’ in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.4.2 Bit Names

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.4.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is RegisterNamebits.ShortName. For example, the enable bit, EN, in the CM1CON0 register can be set in C programs with the instruction `CM1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.4.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.4.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

COG1CON0bits.MD = 0x5;

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

Example 2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

1.4.3 Register and Bit Naming Exceptions

1.4.3.1 Status, Interrupt, and Mirror Bits

Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.4.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to the following:

- EUSART
- MSSP

1.4.4 Register Legend

The table below describes the conventions for bit types and bit reset values used in the current data sheet.

Table 1-2. Register Legend

Value	Description
RO	Read-only bit
W	Writable bit
U	Unimplemented bit, read as '0'
'1'	Bit is set
'0'	Bit is cleared
x	Bit is unknown
u	Bit is unchanged
-n/n	Value at POR and BOR/Value at all other Resets
q	Reset Value is determined by hardware
f	Reset Value is determined by fuse setting
g	Reset Value at POR for PPS re-mappable signals

2. Guidelines for Getting Started with PIC16(L)F18426/46 Microcontrollers

2.1 Basic Connection Requirements

Getting started with the PIC16(L)F18426/46 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All V_{DD} and V_{SS} pins (see Power Supply Pins)
- $\overline{MCLR}$ pin (see Master Clear (MCLR) Pin)

These pins must also be connected if they are being used in the end application:

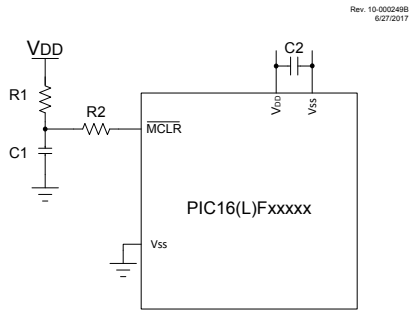
- PGC/PGD pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see In-Circuit Serial Programming™ ICSP™ Pins)
- OSCI and OSCO pins when an external oscillator source is used (see External Oscillator Pins)

Additionally, the following may be required:

- $V_{REF}+/V_{REF}-$ pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in the figure below.

Figure 2-1. Recommended Minimum Connections



Key (all values are recommendations):
C1: 10 nF, 16V ceramic
C2: 0.1 uF, 16V ceramic
R1: 10 kΩ
R2: 100Ω to 470Ω

2.2 Power Supply Pins

2.2.1 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins (V_{DD} and V_{SS}) is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1 µF (100 nF), 10-25V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.

- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 µF in parallel with 0.001 µF).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 Tank Capacitors

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

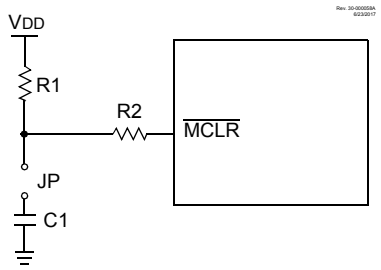
2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to V_{DD} may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

Figure 2-2. Example of $\overline{MCLR}$ Pin Connections



Note:

1. R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.
2. R2 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the extended capacitor, C1, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.

2.4 In-Circuit Serial Programming™ ICSP™ Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they can interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

For device emulation, ensure that the “Communication Channel Select” (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to the *“Development Support”* section.

Related Links

Development Support

2.5 External Oscillator Pins

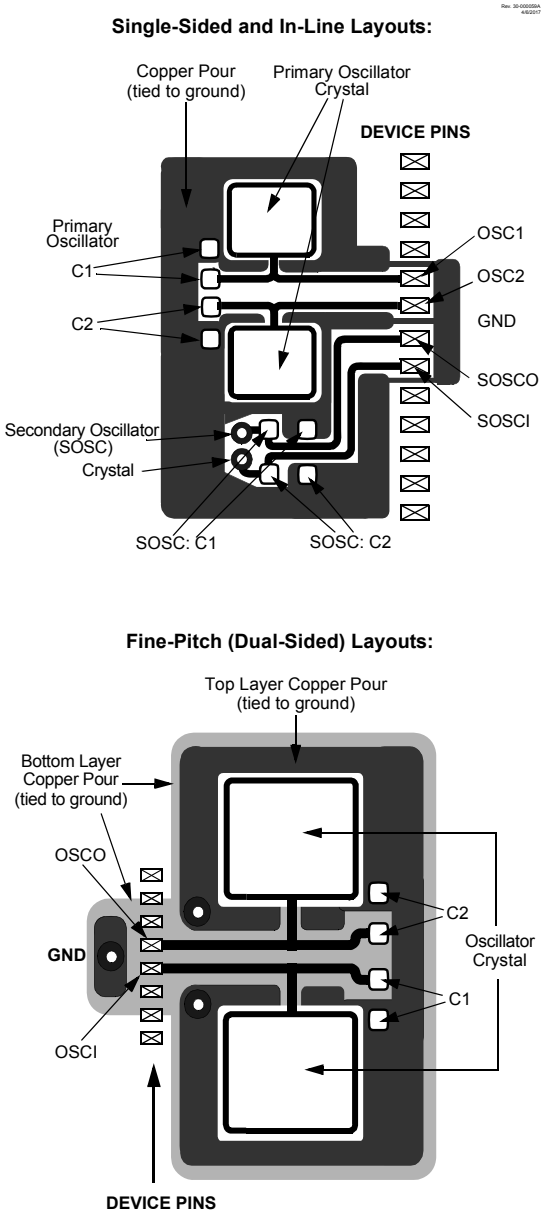
Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator.

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in the following figure. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

Figure 2-3. Suggested Placement of the Oscillator Circuit



In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

For additional information and design guidance on oscillator circuits, refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- AN826, *"Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- AN849, *"Basic PICmicro® Oscillator Design"*
- AN943, *"Practical PICmicro® Oscillator Analysis and Design"*
- AN949, *"Making Your Oscillator Work"*

Related Links

Oscillator Module (with Fail-Safe Clock Monitor)

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1kΩ to 10 kΩ resistor to V_{SS} on unused pins to drive the output to logic low.