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PIC16(L)F1938/9

28/40/44-Pin Flash-Based, 8-Bit CMOS Microcontrollers with LCD Driver

High-Performance RISC CPU:

- Only 49 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 32 MHz oscillator/clock input
  - DC – 125 ns instruction cycle
- Up to 16K x 14 Words of Flash Program Memory
- Up to 1024 Bytes of Data Memory (RAM)
- Interrupt Capability with automatic context saving
- 16-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes
- Processor Read Access to Program Memory
- Pinout Compatible to other 28/40-pin PIC16CXXX and PIC16FXXX Microcontrollers

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 32 MHz to 31 kHz
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR):
  - Selectable between two trip points
  - Disable in Sleep option
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- Wide Operating Voltage Range:
  - 1.8V-5.5V (PIC16F193X)
  - 1.8V-3.6V (PIC16LF193X)

PIC16LF193X Low-Power Features:

- Standby Current:
  - 60 nA @ 1.8V, typical
- Operating Current:
  - 43 μA/MHz @ 1.8V, typical
- Timer1 Oscillator Current:
  - 600 nA @ 32 kHz, 1.8V, typical
- Low-Power Watchdog Timer Current:
  - 500 nA @ 1.8V, typical

Peripheral Features:

- Up to 35 I/O Pins and 1 Input-only pin:
  - High-current source/sink for direct LED drive
  - Individually programmable Interrupt-on-pin change pins
  - Individually programmable weak pull-ups
- Integrated LCD Controller:
  - Up to 96 segments
  - Variable clock input
  - Contrast control
  - Internal voltage reference selections
- Capacitive Sensing module (mTouch™):
  - Up to 16 selectable channels
- A/D Converter:
  - 10-bit resolution and up to 14 channels
  - Selectable 1.024/2.048/4.096V voltage reference
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - Dedicated low-power 32 kHz oscillator driver
  - 16-bit timer/counter with prescaler
  - External Gate Input mode with toggle and single-shot modes
  - Interrupt-on-gate completion
- Timer2, 4, 6: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture, Compare, PWM Modules (CCP):
  - 16-bit Capture, max. resolution 125 ns
  - 16-bit Compare, max. resolution 125 ns
  - 10-bit PWM, max. frequency 31.25 kHz
- Three Enhanced Capture, Compare, PWM modules (ECCP):
  - 3 PWM time-base options
  - Auto-shutdown and auto-restart
  - PWM steering
  - Programmable Dead-band Delay

Peripheral Features (Continued):

- Master Synchronous Serial Port (MSSP) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
  - Auto-wake-up on start
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
- SR Latch (555 Timer):
  - Multiple Set/Reset input options
  - Emulates 555 Timer applications
- 2 Comparators:
  - Rail-to-rail inputs/outputs
  - Power mode control
  - Software enable hysteresis
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

PIC16(L)F193X/194X FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	Data SRAM (bytes)	I/O's(2)	10-bit ADC (ch)	Cap Sense (ch)	Comparators	Timers (8/16-bit)	EUSART	MSSP (I^2C™/SPI)	ECCP	CCP	LCD (Com/Seg/Total)	Debug(1)	XLP
PIC16(L)F1933	(1)	4096	256	256	25	11	8	2	4/1	1	1	3	2	4/16/60(3)	I/H/E	Y
PIC16(L)F1934	(2)	4096	256	256	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H/E	Y
PIC16(L)F1936	(2)	8192	256	512	25	11	8	2	4/1	1	1	3	2	4/16/60(3)	I/H/E	Y
PIC16(L)F1937	(2)	8192	256	512	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H/E	Y
PIC16(L)F1938	(3)	16384	256	1024	25	11	8	2	4/1	1	1	3	2	4/16/60(3)	I/H/E	Y
PIC16(L)F1939	(3)	16384	256	1024	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H/E	Y
PIC16(L)F1946	(4)	8192	256	512	54	17	17	3	4/1	2	2	3	2	4/46/184	I	Y
PIC16(L)F1947	(4)	16384	256	1024	54	17	17	3	4/1	2	2	3	2	4/46/184	I	Y

Note 1: Debugging Methods: (I) – Integrated On-Chip; (H) – using Debug Header; (E) – using Emulation Header.

2: One pin is input-only.

3: COM3 and SEG15 share the same physical pin, therefore SEG15 is not available when using 1/4 multiplex displays.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS41575 PIC16(L)F1933 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.

2: DS41364 PIC16(L)F1934/6/7 Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers.

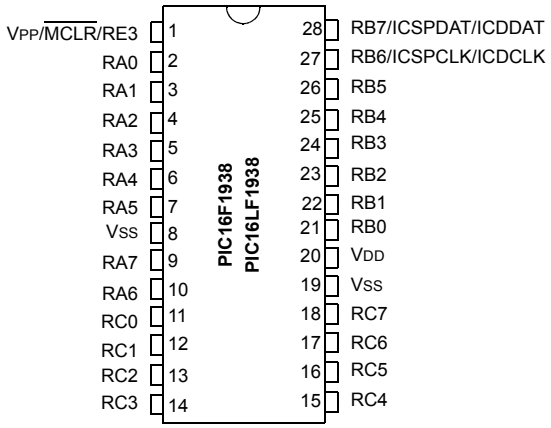
3: DS41574 PIC16(L)F1938/9 Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers.

4: DS41414 PIC16(L)F1946/1947 Data Sheet, 64-Pin Flash, 8-bit Microcontrollers.

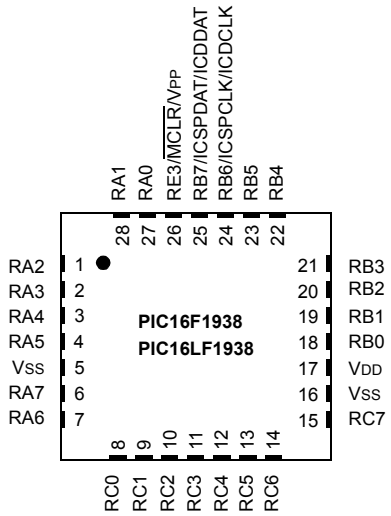
Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

PIN DIAGRAMS

Pin Diagram – 28-Pin SPDIP/SOIC/SSOP

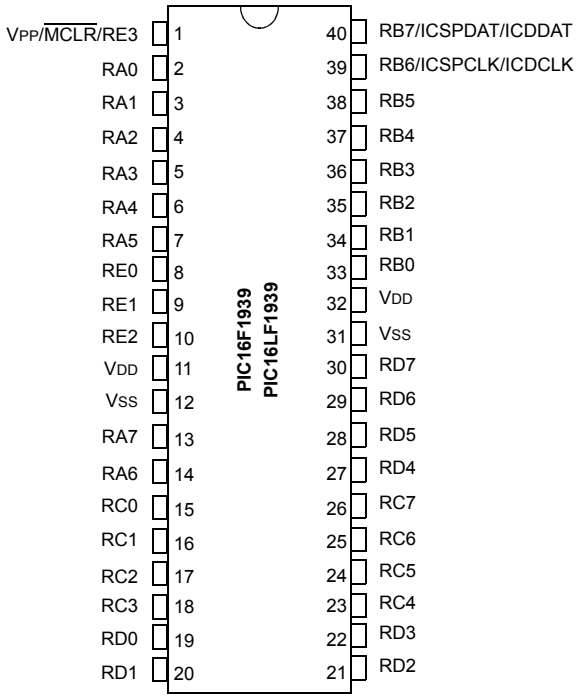


Pin Diagram – 28-Pin QFN/UQFN

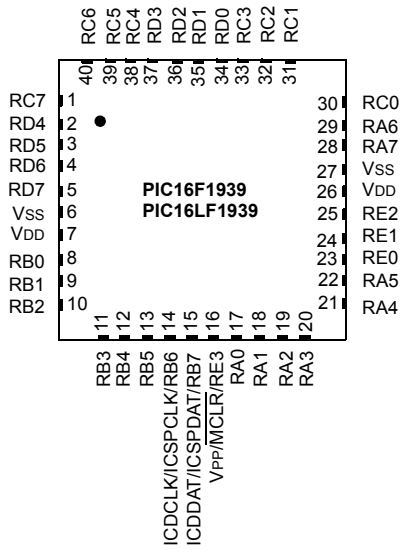


Note: It is recommended that the exposed bottom pad be connected to VSS.

Pin Diagram – 40-Pin PDIP

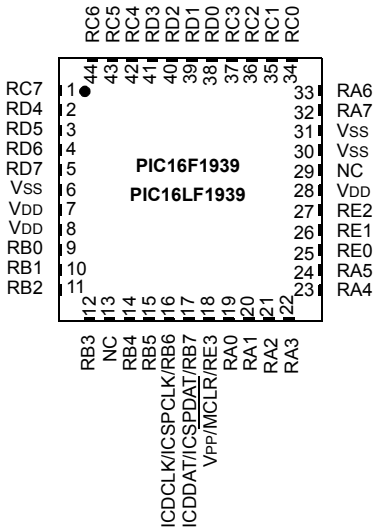


Pin Diagram – 40-Pin UQFN 5x5



Note: It is recommended that the exposed bottom pad be connected to VSS.

Pin Diagram – 44-Pin QFN 8x8



Note: It is recommended that the exposed bottom pad be connected to VSS.

Pin Diagram – 44-Pin TQFP

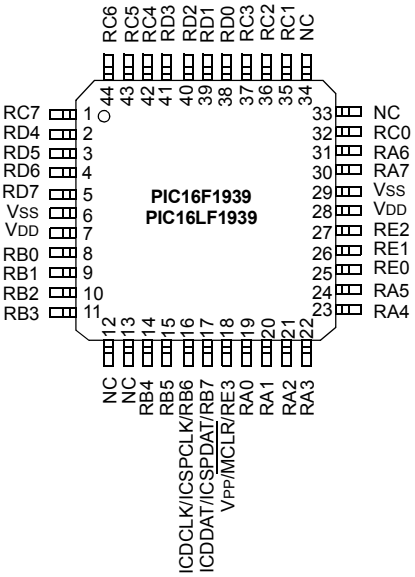


TABLE 1: 28-PIN SUMMARY (PIC16F1938, PIC16LF1938)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin QFN/UQFN	ANSEL	A/D	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	MSSP	LCD	Interrupt	Pull-up	Basic
RA0	2	27	Y	AN0	—	C12IN0-/ C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG12	—	—	VCAP(2)
RA1	3	28	Y	AN1	—	C12IN1-	—	—	—	—	—	SEG7	—	—	—
RA2	4	1	Y	AN2/ VREF-	—	C2IN+/ DACOUT	—	—	—	—	—	COM2	—	—	—
RA3	5	2	Y	AN3/ VREF+	—	C1IN+	—	—	—	—	—	SEG15/ COM3	—	—	—
RA4	6	3	Y	—	CPS6	C1OUT	SRQ	T0CKI	CCP5	—	—	SEG4	—	—	—
RA5	7	4	Y	AN4	CPS7	C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG5	—	—	VCAP(2)
RA6	10	7	—	—	—	—	—	—	—	—	—	SEG1	—	—	OSC2/ CLKOUT VCAP(2)
RA7	9	6	—	—	—	—	—	—	—	—	—	SEG2	—	—	OSC1/ CLKIN
RB0	21	18	Y	AN12	CPS0	—	SRI	—	CCP4	—	—	SEG0	INT/ IOC	Y	—
RB1	22	19	Y	AN10	CPS1	C12IN3-	—	—	P1C	—	—	VLCD1	IOC	Y	—
RB2	23	20	Y	AN8	CPS2	—	—	—	P1B	—	—	VLCD2	IOC	Y	—
RB3	24	21	Y	AN9	CPS3	C12IN2-	—	—	CCP2(1)/ P2A(1)	—	—	VLCD3	IOC	Y	—
RB4	25	22	Y	AN11	CPS4	—	—	—	P1D	—	—	COM0	IOC	Y	—
RB5	26	23	Y	AN13	CPS5	—	—	T1G(1)	P2B(1) CCP3(1)/ P3A(1)	—	—	COM1	IOC	Y	—
RB6	27	24	—	—	—	—	—	—	—	—	—	SEG14	IOC	Y	ICSPCLK/ ICDCLK
RB7	28	25	—	—	—	—	—	—	—	—	—	SEG13	IOC	Y	ICSPDAT/ ICDDAT
RC0	11	8	—	—	—	—	—	T1OSO/ T1CKI	P2B(1)	—	—	—	—	—	—
RC1	12	9	—	—	—	—	—	T1OSI	CCP2(1)/ P2A(1)	—	—	—	—	—	—
RC2	13	10	—	—	—	—	—	—	CCP1/ P1A	—	—	SEG3	—	—	—
RC3	14	11	—	—	—	—	—	—	—	—	SCK/SCL	SEG6	—	—	—
RC4	15	12	—	—	—	—	—	T1G(1)	—	—	SDI/SDA	SEG11	—	—	—
RC5	16	13	—	—	—	—	—	—	—	—	SDO	SEG10	—	—	—
RC6	17	14	—	—	—	—	—	—	CCP3(1) P3A(1)	TX/CK	—	SEG9	—	—	—
RC7	18	15	—	—	—	—	—	—	P3B	RX/DT	—	SEG8	—	—	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{MCLR}$/VPP
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	VDD
Vss	8, 19	5, 16	—	—	—	—	—	—	—	—	—	—	—	—	Vss

Note 1: Pin functions can be moved using the APFCON register.
2: PIC16F1938 devices only.

TABLE 2: 40/44-PIN SUMMARY (PIC16F1939, PIC16LF1939)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ANSEL	A/D	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	MSSP	LCD	Interrupt	Pull-up	Basic
RA0	2	17	19	19	Y	AN0	—	C12IN0-/ C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG12	—	—	VCAP
RA1	3	18	20	20	Y	AN1	—	C12IN1-	—	—	—	—	—	SEG7	—	—	—
RA2	4	19	21	21	Y	AN2/ VREF-	—	C2IN+/ DACOUT	—	—	—	—	—	COM2	—	—	—
RA3	5	20	22	22	Y	AN3/ VREF+	—	C1IN+	—	—	—	—	—	SEG15	—	—	—
RA4	6	21	23	23	Y	—	CPS6	C1OUT	SRQ	T0CKI		—	—	SEG4	—	—	—
RA5	7	22	24	24	Y	AN4	CPS7	C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG5	—	—	VCAP
RA6	14	29	31	33	—	—	—	—	—	—	—	—	—	SEG1	—	—	OSC2/ CLKOUT VCAP
RA7	13	28	30	32	—	—	—	—	—	—	—	—	—	SEG2	—	—	OSC1/ CLKIN
RB0	33	8	8	9	Y	AN12	CPS0	—	SRI	—	—	—	—	SEG0	INT/ IOC	Y	—
RB1	34	9	9	10	Y	AN10	CPS1	C12IN3-	—	—	—	—	—	VLCD1	IOC	Y	—
RB2	35	10	10	11	Y	AN8	CPS2	—	—	—	—	—	—	VLCD2	IOC	Y	—
RB3	36	11	11	12	Y	AN9	CPS3	C12IN2-	—	—	CCP2(1)/ P2A(1)	—	—	VLCD3	IOC	Y	—
RB4	37	12	14	14	Y	AN11	CPS4	—	—	—	—	—	—	COM0	IOC	Y	—
RB5	38	13	15	15	Y	AN13	CPS5	—	—	T1G(1)	CCP3(1)/ P3A(1)	—	—	COM1	IOC	Y	—
RB6	39	14	16	16	—	—	—	—	—	—	—	—	—	SEG14	IOC	Y	ICSPCLK/ ICDCLK
RB7	40	15	17	17	—	—	—	—	—	—	—	—	—	SEG13	IOC	Y	ICSPDAT/ ICDDAT
RC0	15	30	32	34	—	—	—	—	—	T1OSO/ T1CKI	P2B(1)	—	—	—	—	—	—
RC1	16	31	35	35	—	—	—	—	—	T1OSI	CCP2(1)/ P2A(1)	—	—	—	—	—	—
RC2	17	32	36	36	—	—	—	—	—	—	CCP1/ P1A	—	—	SEG3	—	—	—
RC3	18	37	37	37	—	—	—	—	—	—	—	—	SCK/SCL	SEG6	—	—	—
RC4	23	38	42	42	—	—	—	—	—	T1G(1)	—	—	SDI/SDA	SEG11	—	—	—
RC5	24	39	43	43	—	—	—	—	—	—	—	—	SDO	SEG10	—	—	—
RC6	25	40	44	44	—	—	—	—	—	—	—	TX/CK	—	SEG9	—	—	—
RC7	26	1	1	1	—	—	—	—	—	—	—	RX/DT	—	SEG8	—	—	—
RD0	19	34	38	38	Y	—	CPS8	—	—	—	—	—	—	COM3	—	—	—
RD1	20	35	39	39	Y	—	CPS9	—	—	—	CCP4	—	—	—	—	—	—
RD2	21	36	40	40	Y	—	CPS10	—	—	—	P2B(1)	—	—	—	—	—	—
RD3	22	37	41	41	Y	—	CPS11	—	—	—	P2C	—	—	SEG16	—	—	—
RD4	27	2	2	2	Y	—	CPS12	—	—	—	P2D	—	—	SEG17	—	—	—
RD5	28	3	3	3	Y	—	CPS13	—	—	—	P1B	—	—	SEG18	—	—	—
RD6	29	4	4	4	Y	—	CPS14	—	—	—	P1C	—	—	SEG19	—	—	—
RD7	30	5	5	5	Y	—	CPS15	—	—	—	P1D	—	—	SEG20	—	—	—
RE0	8	23	25	25	Y	AN5	—	—	—	—	CCP3(1) P3A(1)	—	—	SEG21	—	—	—
RE1	9	24	26	26	Y	AN6	—	—	—	—	P3B	—	—	SEG22	—	—	—
RE2	10	25	27	27	Y	AN7	—	—	—	—	CCP5	—	—	SEG23	—	—	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{MCLR}$/VPP
VDD	11, 32	7, 26	7, 28	7,8, 28	—	—	—	—	—	—	—	—	—	—	—	—	VDD
Vss	12, 31	6, 27	6, 29	6,30, 31	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pin functions can be moved using the APFCON register.

TABLE OF CONTENTS

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NOTES:

1.0 DEVICE OVERVIEW

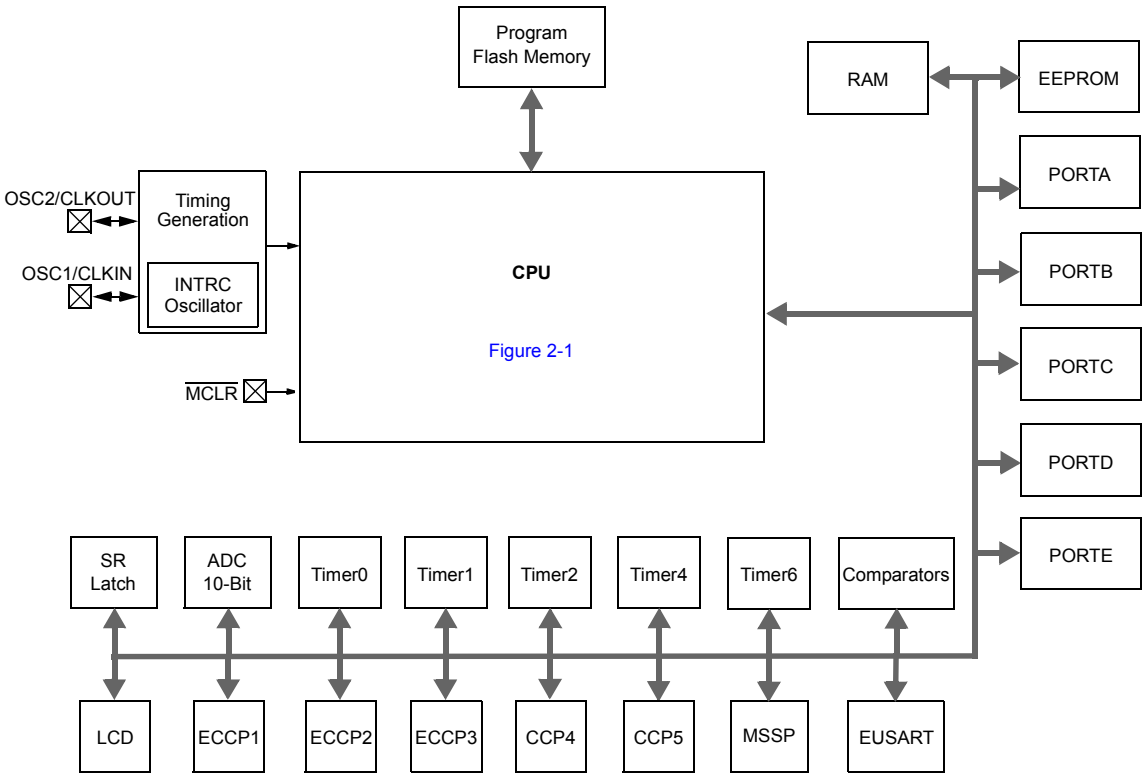
The PIC16(L)F1938/9 are described within this data sheet. They are available in 28/40/44-pin packages. Figure 1-1 shows a block diagram of the PIC16(L)F1938/9 devices. Table 1-2 shows the pin out descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16F1938/9	PIC16LF1938/9
ADC		•	•
Capacitive Sensing Module		•	•
Digital-to-Analog Converter (DAC)		•	•
EUSART		•	•
Fixed Voltage Reference (FVR)		•	•
LCD		•	•
SR Latch		•	•
Temperature Indicator		•	•
Capture/Compare/PWM Modules			
	ECCP1	•	•
	ECCP2	•	•
	ECCP3	•	•
	CCP4	•	•
	CCP5	•	•
Comparators			
	C1	•	•
	C2	•	•
Master Synchronous Serial Ports			
	MSSP1	•	•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	•	•
	Timer4	•	•
	Timer6	•	•

FIGURE 1-1: PIC16(L)F1938/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1938/9 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C12IN0-/C2OUT(1)/ SRNQ(1)/$\overline{SS}$(1)/VCAP(2)/SEG12	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	C2OUT	—	CMOS	Comparator C2 output.
	SRNQ	—	CMOS	SR Latch inverting output.
	$\overline{SS}$	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1938/9 only).
	SEG12	—	AN	LCD Analog output.
RA1/AN1/C12IN1-/SEG7	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
	SEG7	—	AN	LCD Analog output.
RA2/AN2/C2IN+/VREF-/ DACOUT/COM2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	C2IN+	AN	—	Comparator C2 positive input.
	VREF-	AN	—	A/D Negative Voltage Reference input.
	DACOUT	—	AN	Voltage Reference output.
	COM2	—	AN	LCD Analog output.
RA3/AN3/C1IN+/VREF+/ COM3(3)/SEG15	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF+	AN	—	A/D Voltage Reference input.
	COM3(3)	—	AN	LCD Analog output.
	SEG15	—	AN	LCD Analog output.
RA4/C1OUT/CPS6/T0CKI/SRQ/ CCP5/SEG4	RA4	TTL	CMOS	General purpose I/O.
	C1OUT	—	CMOS	Comparator C1 output.
	CPS6	AN	—	Capacitive sensing input 6.
	T0CKI	ST	—	Timer0 clock input.
	SRQ	—	CMOS	SR Latch non-inverting output.
	CCP5	ST	CMOS	Capture/Compare/PWM5.
	SEG4	—	AN	LCD Analog output.
RA5/AN4/C2OUT(1)/CPS7/ SRNQ(1)/$\overline{SS}$(1)/VCAP(2)/SEG5	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	C2OUT	—	CMOS	Comparator C2 output.
	CPS7	AN	—	Capacitive sensing input 7.
	SRNQ	—	CMOS	SR Latch inverting output.
	$\overline{SS}$	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1938/9 only).
	SEG5	—	AN	LCD Analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels XTAL = Crystal
HV = High Voltage I^2C™ = Schmitt Trigger input with I^2C levels

Note 1: Pin function is selectable via the APFCON register.
2: PIC16F1938/9 devices only.
3: PIC16(L)F1938 devices only.
4: PORTD is available on PIC16(L)F1939 devices only.
5: RE<2:0> are available on PIC16(L)F1939 devices only.

TABLE 1-2: PIC16(L)F1938/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA6/OSC2/CLKOUT/VCAP(2)/ SEG1	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1938/9 only).
	SEG1	—	AN	LCD Analog output.
RA7/OSC1/CLKIN/SEG2	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	SEG2	—	AN	LCD Analog output.
RB0/AN12/CPS0/CCP4/SRI/INT/ SEG0	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12 input.
	CPS0	AN	—	Capacitive sensing input 0.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
	SRI	—	ST	SR Latch input.
	INT	ST	—	External interrupt.
	SEG0	—	AN	LCD analog output.
RB1/AN10/C12IN3-/CPS1/P1C/ VLCD1	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	CPS1	AN	—	Capacitive sensing input 1.
	P1C	—	CMOS	PWM output.
	VLCD1	AN	—	LCD analog input.
RB2/AN8/CPS2/P1B/VLCD2	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8 input.
	CPS2	AN	—	Capacitive sensing input 2.
	P1B	—	CMOS	PWM output.
	VLCD2	AN	—	LCD analog input.
RB3/AN9/C12IN2-/CPS3/ CCP2(1)/P2A(1)/VLCD3	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9 input.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	CPS3	AN	—	Capacitive sensing input 3.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P2A	—	CMOS	PWM output.
	VLCD3	AN	—	LCD analog input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels XTAL = Crystal
HV = High Voltage I^2C™ = Schmitt Trigger input with I^2C levels

Note 1: Pin function is selectable via the APFCON register.
2: PIC16F1938/9 devices only.
3: PIC16(L)F1938 devices only.
4: PORTD is available on PIC16(L)F1939 devices only.
5: RE<2:0> are available on PIC16(L)F1939 devices only.

TABLE 1-2: PIC16(L)F1938/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB4/AN11/CPS4/P1D/COM0	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN11	AN	—	A/D Channel 11 input.
	CPS4	AN	—	Capacitive sensing input 4.
	P1D	—	CMOS	PWM output.
	COM0	—	AN	LCD Analog output.
RB5/AN13/CPS5/P2B/CCP3(1)/P3A(1)/T1G(1)/COM1	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN13	AN	—	A/D Channel 13 input.
	CPS5	AN	—	Capacitive sensing input 5.
	P2B	—	CMOS	PWM output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	P3A	—	CMOS	PWM output.
	T1G	ST	—	Timer1 Gate input.
	COM1	—	AN	LCD Analog output.
RB6/ICSPCLK/ICDCLK/SEG14	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
	SEG14	—	AN	LCD Analog output.
RB7/ICSPDAT/ICDDAT/SEG13	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
	SEG13	—	AN	LCD Analog output.
RC0/T1OSO/T1CKI/P2B(1)	RC0	ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
	P2B	—	CMOS	PWM output.
RC1/T1OSI/CCP2(1)/P2A(1)	RC1	ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P2A	—	CMOS	PWM output.
RC2/CCP1/P1A/SEG3	RC2	ST	CMOS	General purpose I/O.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	P1A	—	CMOS	PWM output.
	SEG3	—	AN	LCD Analog output.
RC3/SCK/SCL/SEG6	RC3	ST	CMOS	General purpose I/O.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C™ clock.
	SEG6	—	AN	LCD Analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels XTAL = Crystal
HV = High Voltage I^2C™ = Schmitt Trigger input with I^2C levels

Note 1: Pin function is selectable via the APFCON register.
2: PIC16F1938/9 devices only.
3: PIC16(L)F1938 devices only.
4: PORTD is available on PIC16(L)F1939 devices only.
5: RE<2:0> are available on PIC16(L)F1939 devices only.

TABLE 1-2: PIC16(L)F1938/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/SDI/SDA/T1G(1)/SEG11	RC4	ST	CMOS	General purpose I/O.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.
	T1G	ST	—	Timer1 Gate input.
	SEG11	—	AN	LCD Analog output.
RC5/SDO/SEG10	RC5	ST	CMOS	General purpose I/O.
	SDO	—	CMOS	SPI data output.
	SEG10	—	AN	LCD Analog output.
RC6/TX/CK/CCP3/P3A/SEG9	RC6	ST	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	P3A	—	CMOS	PWM output.
	SEG9	—	AN	LCD Analog output.
RC7/RX/DT/P3B/SEG8	RC7	ST	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	P3B	—	CMOS	PWM output.
	SEG8	—	AN	LCD Analog output.
RD0(4)/CPS8/COM3	RD0	ST	CMOS	General purpose I/O.
	CPS8	AN	—	Capacitive sensing input 8.
	COM3	—	AN	LCD analog output.
RD1(4)/CPS9/CCP4	RD1	ST	CMOS	General purpose I/O.
	CPS9	AN	—	Capacitive sensing input 9.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
RD2(4)/CPS10/P2B	RD2	ST	CMOS	General purpose I/O.
	CPS10	AN	—	Capacitive sensing input 10.
	P2B	—	CMOS	PWM output.
RD3(4)/CPS11/P2C/SEG16	RD3	ST	CMOS	General purpose I/O.
	CPS11	AN	—	Capacitive sensing input 11.
	P2C	—	CMOS	PWM output.
	SEG16	—	AN	LCD analog output.
RD4(4)/CPS12/P2D/SEG17	RD4	ST	CMOS	General purpose I/O.
	CPS12	AN	—	Capacitive sensing input 12.
	P2D	—	CMOS	PWM output.
	SEG17	—	AN	LCD analog output.
RD5(4)/CPS13/P1B/SEG18	RD5	ST	CMOS	General purpose I/O.
	CPS13	AN	—	Capacitive sensing input 13.
	P1D	—	CMOS	PWM output.
	SEG18	—	AN	LCD analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels XTAL = Crystal
HV = High Voltage I^2C™ = Schmitt Trigger input with I^2C levels

Note 1: Pin function is selectable via the APFCON register.
2: PIC16F1938/9 devices only.
3: PIC16(L)F1938 devices only.
4: PORTD is available on PIC16(L)F1939 devices only.
5: RE<2:0> are available on PIC16(L)F1939 devices only.

TABLE 1-2: PIC16(L)F1938/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD6(4)/CPS14/P1C/SEG19	RD6	ST	CMOS	General purpose I/O.
	CPS14	AN	—	Capacitive sensing input 14.
	P1C	—	CMOS	PWM output.
	SEG19	—	AN	LCD analog output.
RD7(4)/CPS15/P1D/SEG20	RD7	ST	CMOS	General purpose I/O.
	CPS15	AN	—	Capacitive sensing input 15.
	P1D	—	CMOS	PWM output.
	SEG20	—	AN	LCD analog output.
RE0(5)/AN5/P3A(1)/CCP3(1)/ SEG21	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	P3A	—	CMOS	PWM output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SEG21	—	AN	LCD analog output.
RE1(5)/AN6/P3B/SEG22	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	P3B	—	CMOS	PWM output.
	SEG22	—	AN	LCD analog output.
RE2(5)/AN7/CCP5/SEG23	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	CCP5	ST	CMOS	Capture/Compare/PWM5.
	SEG23	—	AN	LCD analog output.
RE3/$\overline{\text{MCLR}}$/VPP	RE3	TTL	—	General purpose input.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels XTAL = Crystal
HV = High Voltage I^2C™ = Schmitt Trigger input with I^2C levels

Note 1: Pin function is selectable via the APFCON register.
2: PIC16F1938/9 devices only.
3: PIC16(L)F1938 devices only.
4: PORTD is available on PIC16(L)F1939 devices only.
5: RE<2:0> are available on PIC16(L)F1939 devices only.

NOTES:

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See section **Section 3.5 "Stack"** for more details.

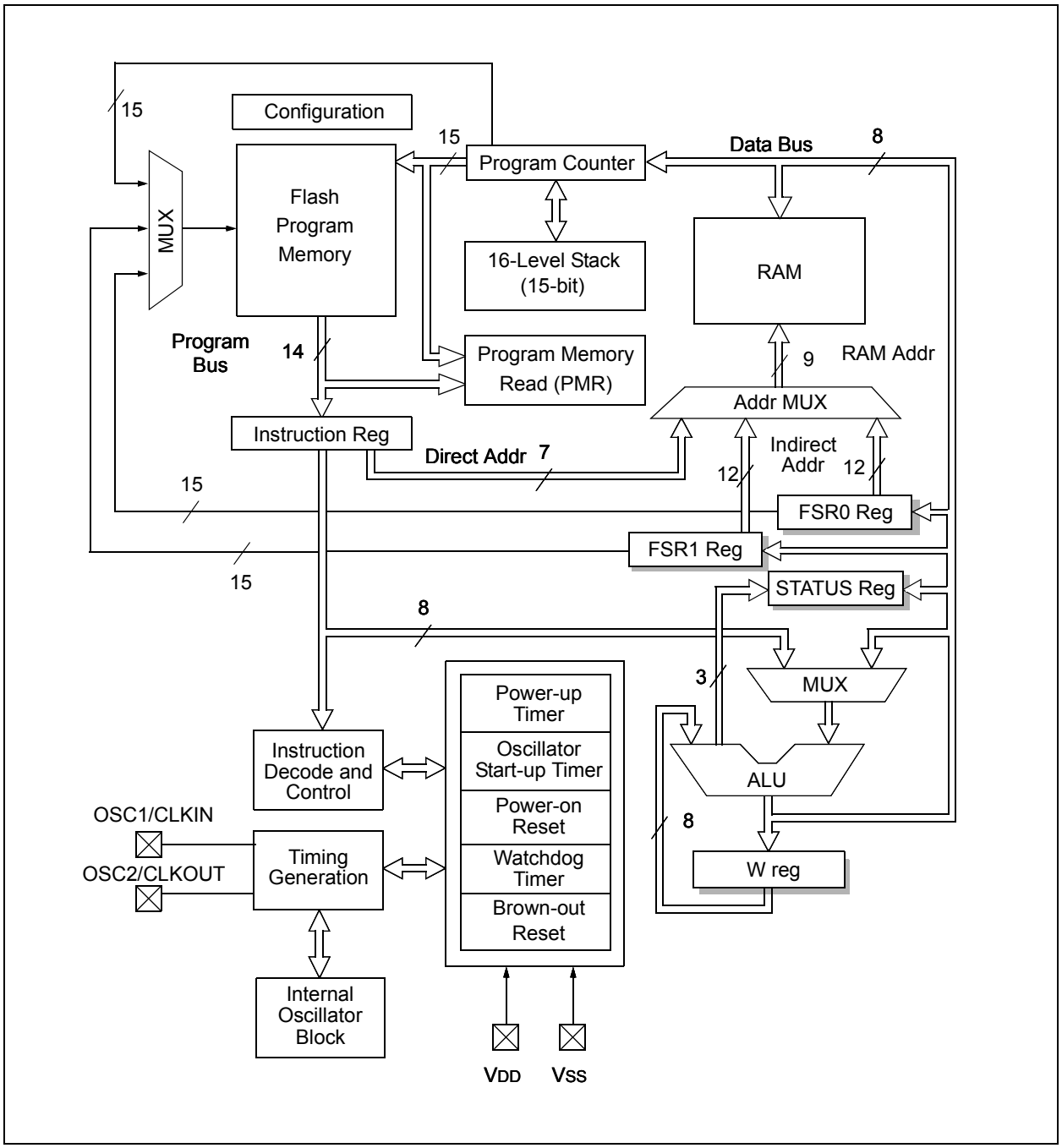
2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.6 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 29.0 "Instruction Set Summary"** for more details.

FIGURE 2-1: CORE BLOCK DIAGRAM



3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
- Data EEPROM memory(1)

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in **Section 11.0 "Data EEPROM and Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

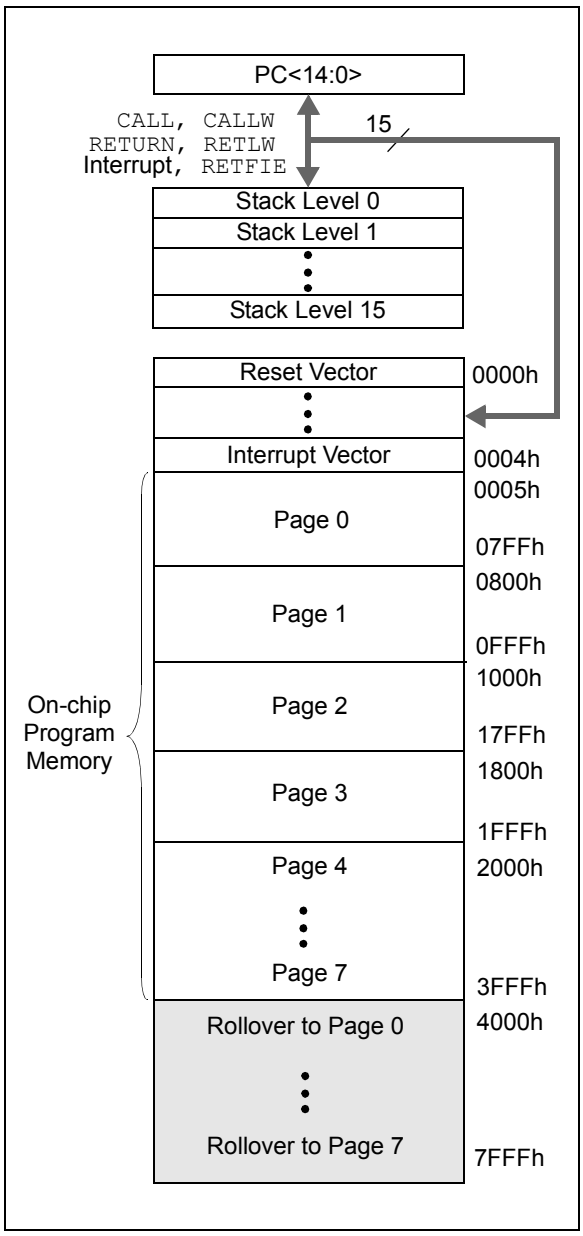
3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1938/9 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
PIC16F1938/PIC16LF1938	16,384	3FFFh
PIC16F1939/PIC16LF1939	16,384	3FFFh

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR 16 KW PARTS



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of `RETLW` instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 `RETLW` Instruction

The `RETLW` instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: `RETLW` INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The `BRW` instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the `BRW` instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-2):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.6 "Indirect Addressing"** for more information.

Data Memory uses a 12-bit address. The upper seven bits of the address define the Bank address and the lower five bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation of the PIC16(L)F1938/9. These registers are listed below:

- INDF0
- INDF1
- PCL
- STATUS
- FSR0 Low
- FSR0 High
- FSR1 Low
- FSR1 High
- BSR
- WREG
- PCLATH
- INTCON

Note:	The core registers are the first 12 addresses of every data memory bank.

3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 29.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

3.3 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

3.3.1 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.3.2 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank.

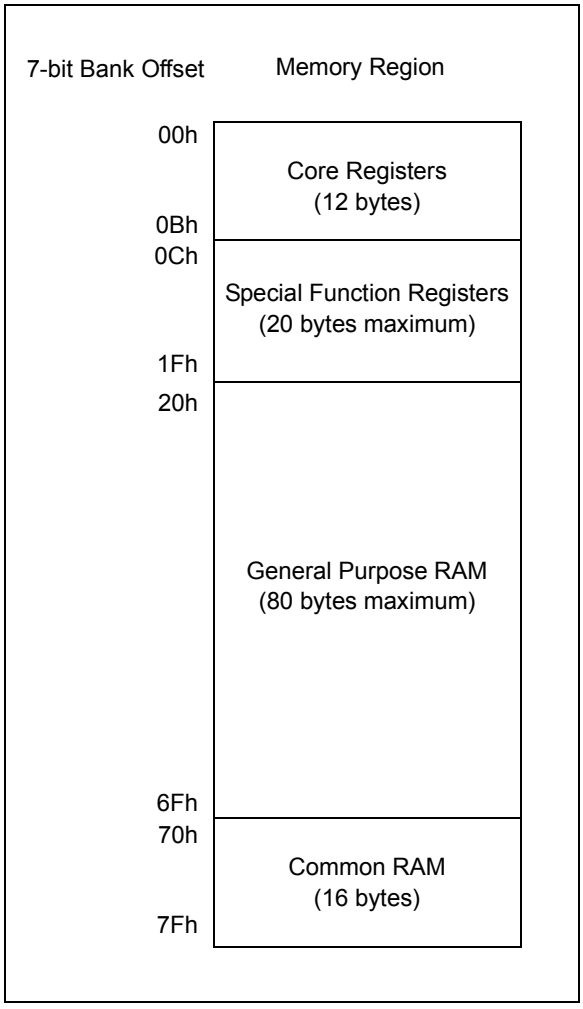
3.3.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.6.2 "Linear Data Memory"** for more information.

3.3.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-2: BANKED MEMORY PARTITIONING



3.3.4 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Table 3-2.

TABLE 3-2: MEMORY MAP TABLES

Device	Banks	Table No.
PIC16F1938 PIC16LF1938	0-7	Table 3-3
	8-15	Table 3-4, Table 3-7
	16-23	Table 3-5
	23-31	Table 3-6, Table 3-9
PIC16F1939 PIC16LF1939	0-7	Table 3-3
	8-15	Table 3-4, Table 3-8
	16-23	Table 3-5
	23-31	Table 3-6, Table 3-9