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# PIC18C601/801

## High-Performance ROM-less Microcontrollers with External Memory Bus

### High Performance RISC CPU:

- C compiler optimized architecture instruction set
- Linear program memory addressing up to 2 Mbytes
- Linear data memory addressing to 4 Kbytes

| Device | External Program Memory | | On-Chip RAM (bytes) |
|---|---|---|---|
| | On-Chip | | |
| | Maximum Addressing (bytes) | Maximum Single Word Instructions | |
| PIC18C601 | 256K | 128K | 1.5K |
| PIC18C801 | 2M | 1M | 1.5K |

- Up to 160 ns instruction cycle:
  - DC - 25 MHz clock input
  - 4 MHz - 6 MHz clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 8 x 8 Single Cycle Hardware Multiplier

### Peripheral Features:

- High current sink/source 25 mA/25 mA
- Up to 47 I/O pins with individual direction control
- Three external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter with 8-bit programmable prescaler
- Timer1 module: 16-bit timer/counter (time-base for CCP)
- Timer2 module: 8-bit timer/counter with 8-bit period register
- Timer3 module: 16-bit timer/counter
- Secondary oscillator clock option - Timer1/Timer3
- Two Capture/Compare/PWM (CCP) modules CCP pins can be configured as:
  - Capture input: 16-bit, max. resolution 10 ns
  - Compare is 16-bit, max. resolution 160 ns ($T_{CY}$)
  - PWM output: PWM resolution is 1- to 10-bit Max. PWM freq. @:
    8-bit resolution = 99 kHz
    10-bit resolution = 24.4 kHz
- Master Synchronous Serial Port (MSSP) with two modes of operation:
  - 3-wire SPI™ (Supports all 4 SPI modes)
  - $I^2C$™ Master and Slave mode
- Addressable USART module: Supports Interrupt on Address bit

### Advanced Analog Features:

- 10-bit Analog-to-Digital Converter module (A/D) with:
  - Fast sampling rate
  - Conversion available during SLEEP
  - DNL = ±1 LSb, INL = ±1 LSb
  - Up to 12 channels available
- Programmable Low Voltage Detection (LVD) module
  - Supports interrupt on Low Voltage Detection

### Special Microcontroller Features:

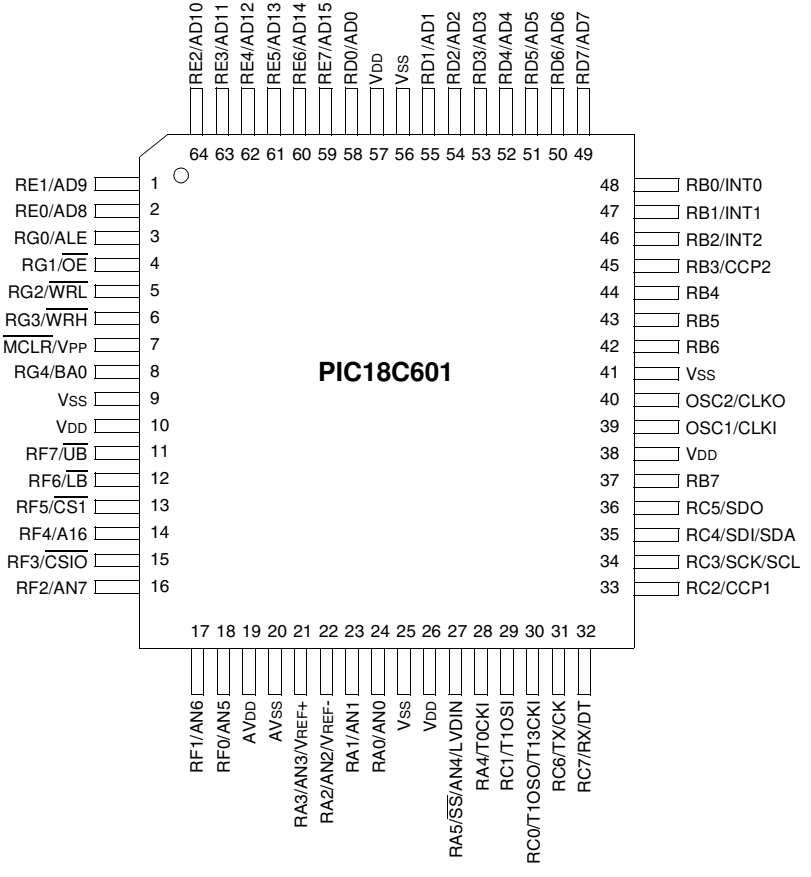
- Power-on Reset (POR), Power-up Timer (PWRT), and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator
- On-chip Boot RAM for boot loader application
- 8-bit or 16-bit external memory interface modes
- Up to two software programmable chip select signals ($\overline{CS1}$ and $\overline{CS2}$)
- One programmable chip I/O select signal ($\overline{CSIO}$) for memory mapped I/O expansion
- Power saving SLEEP mode
- Different oscillator options, including:
  - 4X Phase Lock Loop (of primary oscillator)
  - Secondary Oscillator (32 kHz) clock input

### CMOS Technology:

- Low power, high speed CMOS technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Industrial and Extended temperature ranges
- Low power consumption

**Pin Diagrams**

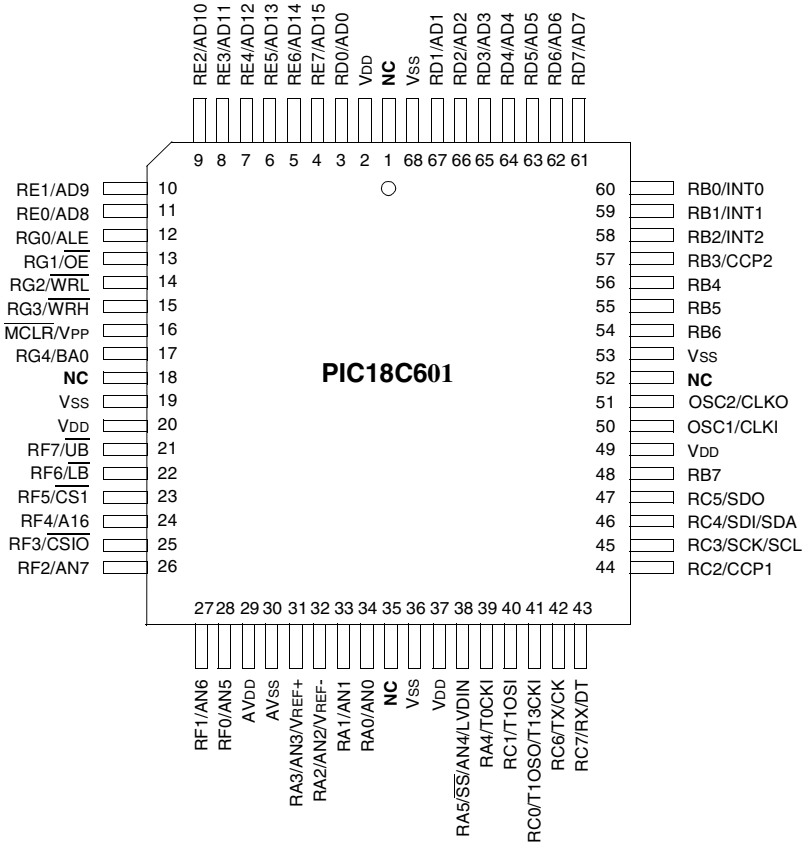
**64-Pin TQFP**



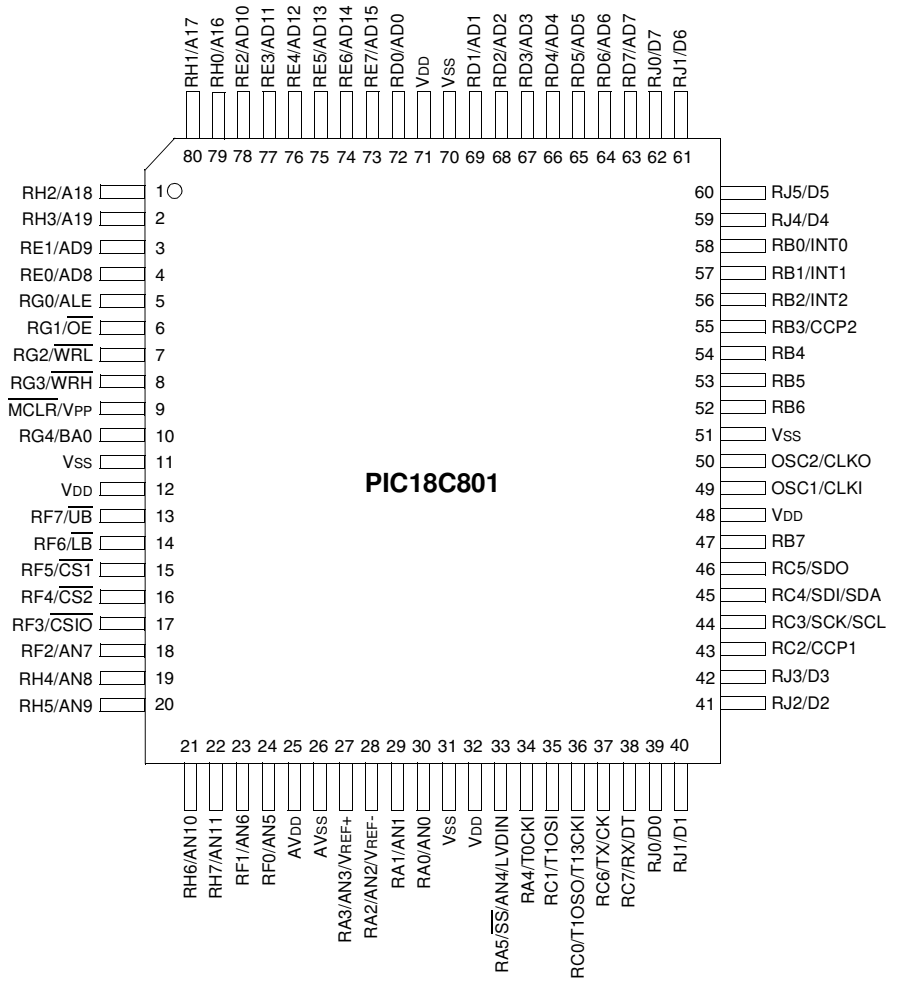
**Pin Diagrams (Cont.'d)**

**68-Pin PLCC**



**Pin Diagrams (Cont.'d)**

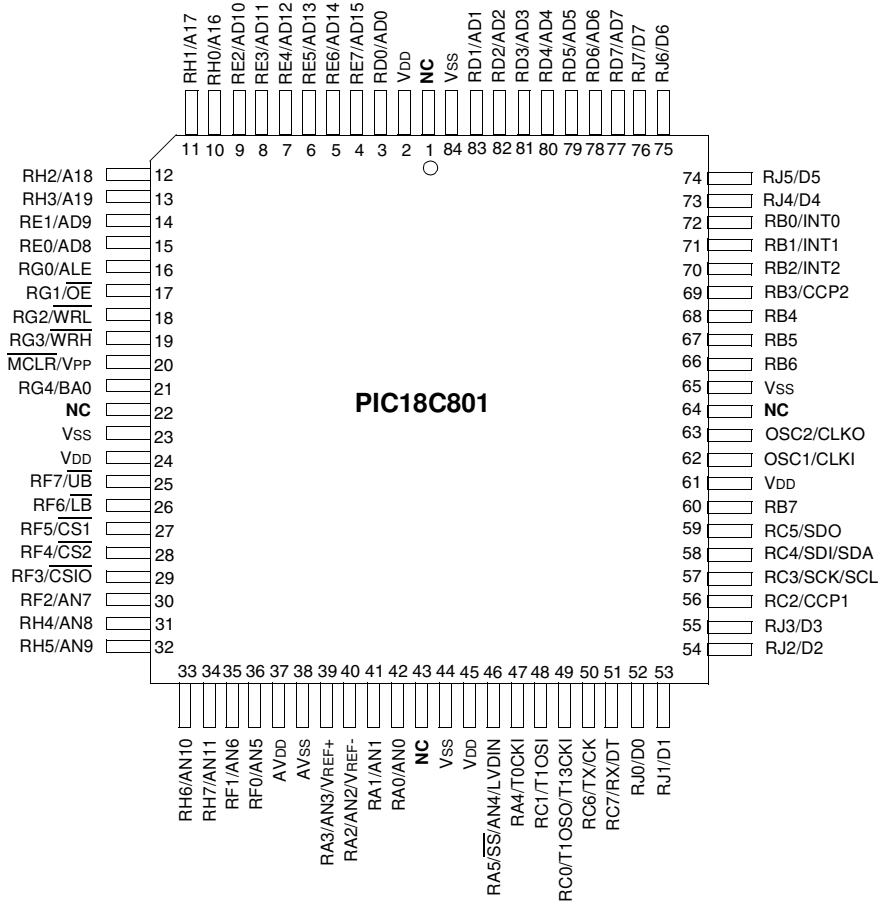
**80-Pin TQFP**



**Pin Diagrams (Cont.'d)**

**84-Pin PLCC**



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**NOTES:**

## 1.0 DEVICE OVERVIEW

This document contains device specific information for the following two devices:

1. PIC18C601
2. PIC18C801

The PIC18C601 is available in 64-pin TQFP and 68-pin PLCC packages. The PIC18C801 is available in 80-pin TQFP and 84-pin PLCC packages.

An overview of features is shown in Table 1-1.

Device block diagrams are provided in Figure 1-1 for the 64/68-pin configuration, and Figure 1-2 for the 80/84-pin configuration. The pinouts for both packages are listed in Table 1-2.

**TABLE 1-1: DEVICE FEATURES**

| Features | | PIC18C601 | PIC18C801 |
|---|---|---|---|
| Operating Frequency | | DC - 25 MHz | DC - 25 MHz |
| External Program Memory | Bytes | 256K | 2M |
| | Max. # of Single Word Instructions | 128K | 1M |
| Data Memory (Bytes) | | 1536 | 1536 |
| Interrupt Sources | | 15 | 15 |
| I/O Ports | | Ports A - G | Ports A - H, J |
| Timers | | 4 | 4 |
| Capture/Compare/PWM modules | | 2 | 2 |
| Serial Communications | | MSSP, Addressable USART | MSSP, Addressable USART |
| 10-bit Analog-to-Digital Module | | 8 input channels | 12 input channels |
| RESETS (and Delays) | | POR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST) | POR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST) |
| Programmable Low Voltage Detect | | Yes | Yes |
| 8-bit External Memory Interface | | Yes | Yes |
| 8-bit De-multiplexed External Memory Interface | | No | Yes |
| 16-bit External Memory Interfaces | | Yes | Yes |
| On-chip Chip Select Signals | | $\overline{CS1}$ | $\overline{CS1}$, $\overline{CS2}$ |
| On-chip I/O Chip Select Signal | | Yes | Yes |
| Instruction Set | | 75 Instructions | 75 Instructions |
| Packages | | 64-pin TQFP 68-pin PLCC | 80-pin TQFP 84-pin PLCC |

**FIGURE 1-1: PIC18C601 BLOCK DIAGRAM**

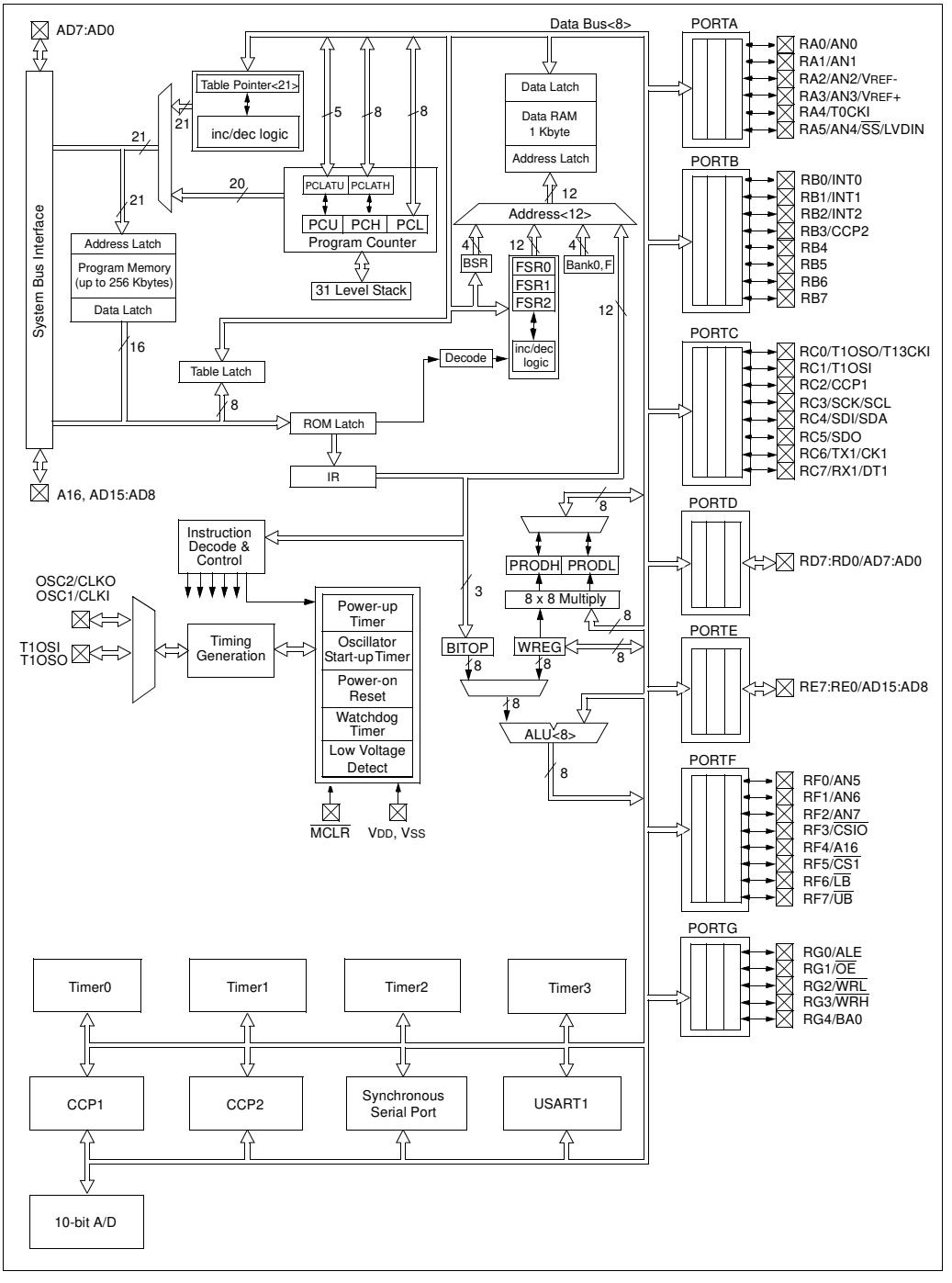


**FIGURE 1-2: PIC18C801 BLOCK DIAGRAM**

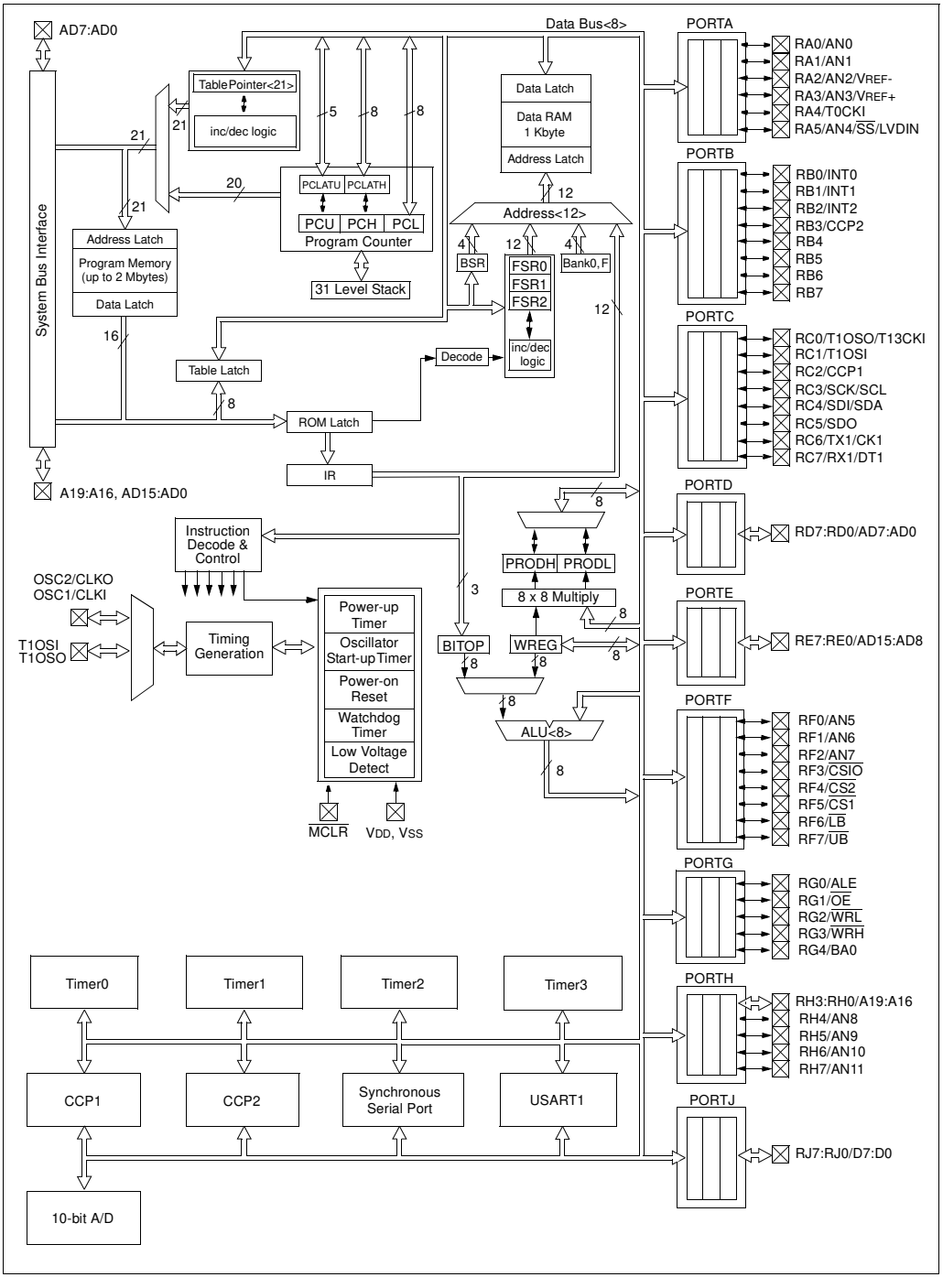


**TABLE 1-2: PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| $\overline{MCLR}$/VPP | 7 | 16 | 9 | 20 | | | |
| $\overline{MCLR}$ | | | | | I | ST | Master clear (RESET) input. This pin is an active low RESET to the device. |
| VPP | | | | | P | | Programming voltage input. |
| NC | — | 1, 18, 35, 52 | — | 1, 22, 43, 64 | — | — | These pins should be left unconnected. |
| OSC1/CLKI | 39 | 50 | 49 | 62 | | | |
| OSC1 | | | | | I | CMOS/ST | Oscillator crystal input or external clock source input. ST buffer when in RC mode. Otherwise CMOS. |
| CLKI | | | | | I | CMOS | External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins). |
| OSC2/CLKO | 40 | 51 | 50 | 63 | | | |
| OSC2 | | | | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | | | | O | — | In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTA is a bi-directional I/O port. |
| RA0/AN0 | 24 | 34 | 30 | 42 | | | |
| RA0 | | | | | I/O | TTL | Digital I/O. |
| AN0 | | | | | I | Analog | Analog input 0. |
| RA1/AN1 | 23 | 33 | 29 | 41 | | | |
| RA1 | | | | | I/O | TTL | Digital I/O. |
| AN1 | | | | | I | Analog | Analog input 1. |
| RA2/AN2/VREF- | 22 | 32 | 28 | 40 | | | |
| RA2 | | | | | I/O | TTL | Digital I/O. |
| AN2 | | | | | I | Analog | Analog input 2. |
| VREF- | | | | | I | Analog | A/D reference voltage (Low) input. |
| RA3/AN3/VREF+ | 21 | 31 | 27 | 39 | | | |
| RA3 | | | | | I/O | TTL | Digital I/O. |
| AN3 | | | | | I | Analog | Analog input 3. |
| VREF+ | | | | | I | Analog | A/D reference voltage (High) input. |
| RA4/T0CKI | 28 | 39 | 34 | 47 | | | |
| RA4 | | | | | I/O | ST/OD | Digital I/O – Open drain when configured as output. |
| T0CKI | | | | | I | ST | Timer0 external clock input. |
| RA5/AN4/$\overline{SS}$/LVDIN | 27 | 38 | 33 | 46 | | | |
| RA5 | | | | | I/O | TTL | Digital I/O. |
| AN4 | | | | | I | Analog | Analog input 4. |
| $\overline{SS}$ | | | | | I | ST | SPI slave select input. |
| LVDIN | | | | | I | Analog | Low voltage detect input. |

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0 | 48 | 60 | 58 | 72 | | | |
| RB0 | | | | | I/O | TTL | Digital I/O. |
| INT0 | | | | | I | ST | External interrupt 0. |
| RB1/INT1 | 47 | 59 | 57 | 71 | | | |
| RB1 | | | | | I/O | TTL | Digital I/O. |
| INT1 | | | | | I | ST | External interrupt 1. |
| RB2/INT2 | 46 | 58 | 56 | 70 | | | |
| RB2 | | | | | I/O | TTL | Digital I/O. |
| INT2 | | | | | I | ST | External interrupt 2. |
| RB3/CCP2 | 45 | 57 | 55 | 69 | | | |
| RB3 | | | | | I/O | TTL | Digital I/O. |
| CCP2 | | | | | I/O | ST | Capture2 input, Compare2 output, PWM2 output. |
| RB4 | 44 | 56 | 54 | 68 | I/O | TTL | Digital I/O, Interrupt-on-change pin. |
| RB5 | 43 | 55 | 53 | 67 | I/O | TTL | Digital I/O, Interrupt-on-change pin. |
| RB6 | 42 | 54 | 52 | 66 | I/O | TTL | Digital I/O, Interrupt-on-change pin. |
| | | | | | I | ST | ICSP programming clock. |
| RB7 | 37 | 48 | 47 | 60 | I/O | TTL | Digital I/O, Interrupt-on-change pin. |
| | | | | | I/O | ST | ICSP programming data. |

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
Analog = Analog input
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to $V_{DD}$)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTC is a bi-directional I/O port. |
| RC0/T1OSO/T13CKI | 30 | 41 | 36 | 49 | | | |
| RC0 | | | | | I/O | ST | Digital I/O. |
| T1OSO | | | | | O | — | Timer1 oscillator output. |
| T13CKI | | | | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI | 29 | 40 | 35 | 48 | | | |
| RC1 | | | | | I/O | ST | Digital I/O. |
| T1OSI | | | | | I | CMOS | Timer1 oscillator input. |
| RC2/CCP1 | 33 | 44 | 43 | 56 | | | |
| RC2 | | | | | I/O | ST | Digital I/O. |
| CCP1 | | | | | I/O | ST | Capture1 input/Compare1 output/PWM1 output. |
| RC3/SCK/SCL | 34 | 45 | 44 | 57 | | | |
| RC3 | | | | | I/O | ST | Digital I/O. |
| SCK | | | | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL | | | | | I/O | ST | Synchronous serial clock input/output for $I^2C$ mode. |
| RC4/SDI/SDA | 35 | 46 | 45 | 58 | | | |
| RC4 | | | | | I/O | ST | Digital I/O. |
| SDI | | | | | I | ST | SPI data in. |
| SDA | | | | | I/O | ST | $I^2C$ data I/O. |
| RC5/SDO | 36 | 47 | 46 | 59 | | | |
| RC5 | | | | | I/O | ST | Digital I/O. |
| SDO | | | | | O | — | SPI data out. |
| RC6/TX/CK | 31 | 42 | 37 | 50 | | | |
| RC6 | | | | | I/O | ST | Digital I/O. |
| TX | | | | | O | — | USART asynchronous transmit. |
| CK | | | | | I/O | ST | USART synchronous clock. |
| RC7/RX/DT | 32 | 43 | 38 | 51 | | | |
| RC7 | | | | | I/O | ST | Digital I/O. |
| RX | | | | | I | ST | USART asynchronous receive. |
| DT | | | | | I/O | ST | USART synchronous data. |

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to $V_{DD}$)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTD is a bi-directional I/O port. These pins have TTL input buffers when external memory is enabled. |
| RD0/AD0 | 58 | 3 | 72 | 3 | | | |
| RD0 | | | | | I/O | ST | Digital I/O. |
| AD0 | | | | | I/O | TTL | External memory address/data 0. |
| RD1/AD1 | 55 | 67 | 69 | 83 | | | |
| RD1 | | | | | I/O | ST | Digital I/O. |
| AD1 | | | | | I/O | TTL | External memory address/data 1. |
| RD2/AD2 | 54 | 66 | 68 | 82 | | | |
| RD2 | | | | | I/O | ST | Digital I/O. |
| AD2 | | | | | I/O | TTL | External memory address/data 2. |
| RD3/AD3 | 53 | 65 | 67 | 81 | | | |
| RD3 | | | | | I/O | ST | Digital I/O. |
| AD3 | | | | | I/O | TTL | External memory address/data 3. |
| RD4/AD4 | 52 | 64 | 66 | 80 | | | |
| RD4 | | | | | I/O | ST | Digital I/O. |
| AD4 | | | | | I/O | TTL | External memory address/data 4. |
| RD5/AD5 | 51 | 63 | 65 | 79 | | | |
| RD5 | | | | | I/O | ST | Digital I/O. |
| AD5 | | | | | I/O | TTL | External memory address/data 5. |
| RD6/AD6 | 50 | 62 | 64 | 78 | | | |
| RD6 | | | | | I/O | ST | Digital I/O. |
| AD6 | | | | | I/O | TTL | External memory address/data 6. |
| RD7/AD7 | 49 | 61 | 63 | 77 | | | |
| RD7 | | | | | I/O | ST | Digital I/O. |
| AD7 | | | | | I/O | TTL | External memory address/data 7. |

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTE is a bi-directional I/O port. |
| RE0/AD8 | 2 | 11 | 4 | 15 | | | |
| RE0 | | | | | I/O | ST | Digital I/O. |
| AD8 | | | | | I/O | TTL | External memory address/data 8. |
| RE1/AD9 | 1 | 10 | 3 | 14 | | | |
| RE1 | | | | | I/O | ST | Digital I/O. |
| AD9 | | | | | I/O | TTL | External memory address/data 9. |
| RE2/AD10 | 64 | 9 | 78 | 9 | | | |
| RE2 | | | | | I/O | ST | Digital I/O. |
| AD10 | | | | | I/O | TTL | External memory address/data 10. |
| RE3/AD11 | 63 | 8 | 77 | 8 | | | |
| RE3 | | | | | I/O | ST | Digital I/O. |
| AD11 | | | | | I/O | TTL | External memory address/data 11. |
| RE4/AD12 | 62 | 7 | 76 | 7 | | | |
| RE4 | | | | | I/O | ST | Digital I/O. |
| AD12 | | | | | I/O | TTL | External memory address/data 12. |
| RE5/AD13 | 61 | 6 | 75 | 6 | | | |
| RE5 | | | | | I/O | ST | Digital I/O. |
| AD13 | | | | | I/O | TTL | External memory address/data 13. |
| RE6/AD14 | 60 | 5 | 74 | 5 | | | |
| RE6 | | | | | I/O | ST | Digital I/O. |
| AD14 | | | | | I/O | TTL | External memory address/data 14. |
| RE7/AD15 | 59 | 4 | 73 | 4 | | | |
| RE7 | | | | | I/O | ST | Digital I/O. |
| AD15 | | | | | I/O | ST | External memory address/data 15. |

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
Analog = Analog input
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to $V_{DD}$)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTF is a bi-directional I/O port. |
| RF0/AN5 | 18 | 28 | 24 | 36 | | | |
| RF0 | | | | | I/O | ST | Digital I/O. |
| AN5 | | | | | I | Analog | Analog input 5. |
| RF1/AN6 | 17 | 27 | 23 | 35 | | | |
| RF1 | | | | | I/O | ST | Digital I/O. |
| AN6 | | | | | I | Analog | Analog input 6. |
| RF2/AN7 | 16 | 26 | 18 | 30 | | | |
| RF2 | | | | | I/O | ST | Digital I/O. |
| AN7 | | | | | I | Analog | Analog input 7. |
| RF3/$\overline{\text{CSIO}}$ | 15 | 25 | 17 | 29 | | | |
| RF3 | | | | | I/O | ST | Digital I/O. |
| $\overline{\text{CSIO}}$ | | | | | I/O | ST | System bus chip select I/O. |
| RF4/A16 | 14 | 24 | — | — | | | |
| RF4/$\overline{\text{CS2}}$ | — | — | 16 | 28 | | | |
| RF4 | | | | | I/O | ST | Digital I/O. |
| A16 | | | | | I/O | TTL | External memory address 16. |
| $\overline{\text{CS2}}$ | | | | | O | TTL | Chip select 2. |
| RF5/$\overline{\text{CS1}}$ | 13 | 23 | 15 | 27 | | | |
| RF5 | | | | | I/O | ST | Digital I/O. |
| $\overline{\text{CS1}}$ | | | | | O | TTL | Chip select 1. |
| RF6/$\overline{\text{LB}}$ | 12 | 22 | 14 | 26 | | | |
| RF6 | | | | | I/O | ST | Digital I/O. |
| $\overline{\text{LB}}$ | | | | | O | TTL | Low byte select signal for external memory interface. |
| RF7/$\overline{\text{UB}}$ | 11 | 21 | 13 | 25 | | | |
| RF7 | | | | | I/O | ST | Digital I/O. |
| $\overline{\text{UB}}$ | | | | | O | TTL | High byte select signal for external memory interface. |

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
Analog = Analog input
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to $V_{DD}$)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTG is a bi-directional I/O port. |
| RG0/ALE | 3 | 12 | 5 | 16 | | | |
| RG0 | | | | | I/O | ST | Digital I/O. |
| ALE | | | | | O | TTL | Address Latch Enable. |
| RG1/$\overline{OE}$ | 4 | 13 | 6 | 17 | | | |
| RG1 | | | | | I/O | ST | Digital I/O. |
| $\overline{OE}$ | | | | | O | TTL | Output Enable. |
| RG2/$\overline{WRL}$ | 5 | 14 | 7 | 18 | | | |
| RG2 | | | | | I/O | ST | Digital I/O. |
| $\overline{WRL}$ | | | | | O | TTL | Write Low control. |
| RG3/$\overline{WRH}$ | 6 | 15 | 8 | 19 | | | |
| RG3 | | | | | I/O | ST | Digital I/O. |
| $\overline{WRH}$ | | | | | O | TTL | Write High control. |
| RG4/BA0 | 8 | 17 | 10 | 21 | | | |
| RG4 | | | | | I/O | ST | Digital I/O. |
| BA0 | | | | | O | TTL | System bus byte address 0. |
| | | | | | | | PORTH is a bi-directional I/O port. |
| RH0/A16 | — | — | 79 | 10 | | | |
| RH0 | | | | | I/O | ST | Digital I/O. |
| A16 | | | | | O | TTL | External memory address 16. |
| RH1/A17 | — | — | 80 | 11 | | | |
| RH1 | | | | | I/O | ST | Digital I/O. |
| A17 | | | | | O | — | External memory address 17. |
| RH2/A18 | — | — | 1 | 12 | | | |
| RH2 | | | | | I/O | ST | Digital I/O. |
| A18 | | | | | O | — | External memory address 18. |
| RH3/A19 | — | — | 2 | 13 | | | |
| RH3 | | | | | I/O | ST | Digital I/O. |
| A19 | | | | | O | — | External memory address 19. |
| RH4/AN8 | — | — | 19 | 31 | | | |
| RH4 | | | | | I/O | ST | Digital I/O. |
| AN8 | | | | | I | Analog | Analog input 8. |
| RH5/AN9 | — | — | 20 | 32 | | | |
| RH5 | | | | | I/O | ST | Digital I/O. |
| AN9 | | | | | I | Analog | Analog input 9. |
| RH6/AN10 | — | — | 21 | 33 | | | |
| RH6 | | | | | I/O | ST | Digital I/O. |
| AN10 | | | | | I | Analog | Analog input 10. |
| RH7/AN11 | — | — | 22 | 34 | | | |
| RH7 | | | | | I/O | ST | Digital I/O. |
| AN11 | | | | | I | Analog | Analog input 11. |

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
Analog = Analog input
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to VDD)

**TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | PIC18C601 | | PIC18C801 | | | | |
| | TQFP | PLCC | TQFP | PLCC | | | |
| | | | | | | | PORTJ is a bi-directional I/O port. |
| RJ0/D0 | — | — | 39 | 52 | | | |
| RJ0 | | | | | I/O | ST | Digital I/O. |
| D0 | | | | | I/O | TTL | System bus data bit 0. |
| RJ1/D1 | — | — | 40 | 53 | | | |
| RJ1 | | | | | I/O | ST | Digital I/O. |
| D1 | | | | | I/O | TTL | System bus data bit 1. |
| RJ2/D2 | — | — | 41 | 54 | | | |
| RJ2 | | | | | I/O | ST | Digital I/O. |
| D2 | | | | | I/O | TTL | System bus data bit 2. |
| RJ3/D3 | — | — | 42 | 55 | | | |
| RJ3 | | | | | I/O | ST | Digital I/O. |
| D3 | | | | | I/O | TTL | System bus data bit 3. |
| RJ4/D4 | — | — | 59 | 73 | | | |
| RJ4 | | | | | I/O | ST | Digital I/O. |
| D4 | | | | | I/O | TTL | System bus data bit 4. |
| RJ5/D5 | — | — | 60 | 74 | | | |
| RJ5 | | | | | I/O | ST | Digital I/O. |
| D5 | | | | | I/O | TTL | System bus data bit 5. |
| RJ6/D6 | — | — | 61 | 75 | | | |
| RJ6 | | | | | I/O | ST | Digital I/O. |
| D6 | | | | | I/O | TTL | System bus data bit 6. |
| RJ7/D7 | — | — | 62 | 76 | | | |
| RJ7 | | | | | I/O | ST | Digital I/O. |
| D7 | | | | | I/O | TTL | System bus data bit 7. |
| VSS | 9, 25, 41, 56 | 19, 36, 53, 68 | 11,31, 51, 70 | 23, 44, 65, 84 | P | — | Ground reference for logic and I/O pins. |
| VDD | 10,26, 38, 57 | 2, 20, 37, 49 | 12,32, 48, 71 | 2, 24, 45, 61 | P | — | Positive supply for logic and I/O pins. |
| AVSS | 20 | 30 | 26 | 38 | P | — | Ground reference for analog modules. |
| AVDD | 19 | 29 | 25 | 37 | P | — | Positive supply for analog modules. |

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

# 2.0 OSCILLATOR CONFIGURATIONS

## 2.1 Oscillator Types

PIC18C601/801 can be operated in one of four oscillator modes, programmable by configuration bits FOSC1:FOSC0 in CONFIG1H register:

1. LP Low Power Crystal
2. HS High Speed Crystal/Resonator
3. RC External Resistor/Capacitor
4. EC External Clock

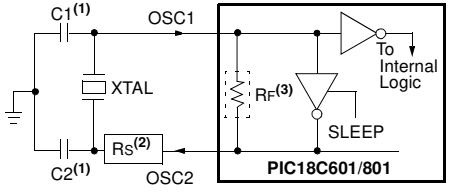
## 2.2 Crystal Oscillator/Ceramic Resonators

In LP or HS oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-1 shows the pin connections. An external clock source may also be connected to the OSC1 pin, as shown in Figure 2-3 and Figure 2-4.

PIC18C601/801 oscillator design requires the use of a parallel cut crystal.

| **Note:** | Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications. |
|---|---|

**FIGURE 2-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS OR LP OSC CONFIGURATION)**




**Note 1:** See Table 2-1 and Table 2-2 for recommended values of C1 and C2.

**2:** A series resistor (RS) may be required for AT strip cut crystals.

**3:** RF varies with the crystal chosen.

**TABLE 2-1: CERAMIC RESONATORS**

| Ranges Tested: | | | |
|---|---|---|---|
| **Mode** | **Freq.** | **OSC1** | **OSC2** |
| HS | 8.0 MHz | 10 - 68 pF | 10 - 68 pF |
| | 16.0 MHz | 10 - 22 pF | 10 - 22 pF |
| | 20.0 MHz | TBD | TBD |
| | 25.0 MHz | TBD | TBD |
| HS+PLL | 4.0 MHz | TBD | TBD |
| **These values are for design guidance only.** See notes on this page. | | | |
| **Resonators Used:** | | | |
| 4.0 MHz | Murata Erie CSA4.00MG | | ± 0.5% |
| 8.0 MHz | Murata Erie CSA8.00MT | | ± 0.5% |
| 16.0 MHz | Murata Erie CSA16.00MX | | ± 0.5% |
| All resonators used did not have built-in capacitors. | | | |

**TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR**

| Osc Type | Crystal Freq. | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32.0 kHz | 33 pF | 33 pF |
| | 200 kHz | 15 pF | 15 pF |
| HS | 4.0 MHz | 15 pF | 15 pF |
| | 8.0 MHz | 15-33 pF | 15-33 pF |
| | 20.0 MHz | 15-33 pF | 15-33 pF |
| | 25.0 MHz | TBD | TBD |
| HS+PLL | 4.0 MHz | 15 pF | 15 pF |
| **These values are for design guidance only.** See notes on this page. | | | |
| **Crystals Used** | | | |
| 32.0 kHz | Epson C-001R32.768K-A | | ± 20 PPM |
| 200 kHz | STD XTL 200.000kHz | | ± 20 PPM |
| 1.0 MHz | ECS ECS-10-13-1 | | ± 50 PPM |
| 4.0 MHz | ECS ECS-40-20-1 | | ± 50 PPM |
| 8.0 MHz | EPSON CA-301 8.000M-C | | ± 30 PPM |
| 20.0 MHz | EPSON CA-301 20.000M-C | | ± 30 PPM |



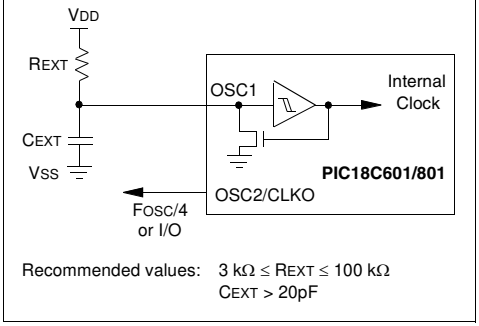
**Note 1:** Recommended values of C1 and C2 are identical to the ranges tested (Table 2-1).
**2:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
**3:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
**4:** Rs may be required in HS mode to avoid overdriving crystals with low drive level specification.

## 2.3 RC Oscillator

For timing insensitive applications, the "RC" oscillator mode offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 2-2 shows how the RC combination is connected.

In the RC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic.

**FIGURE 2-2: RC OSCILLATOR MODE**



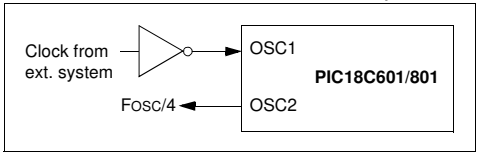

 

## 2.4 External Clock Input

The EC oscillator mode requires an external clock source to be connected to the OSC1 pin. The feedback device between OSC1 and OSC2 is turned off in these modes to save current. There is no oscillator start-up time required after a Power-on Reset or after a recovery from SLEEP mode.

In the EC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-3 shows the pin connections for the EC oscillator mode.

**FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (EC OSC CONFIGURATION)**



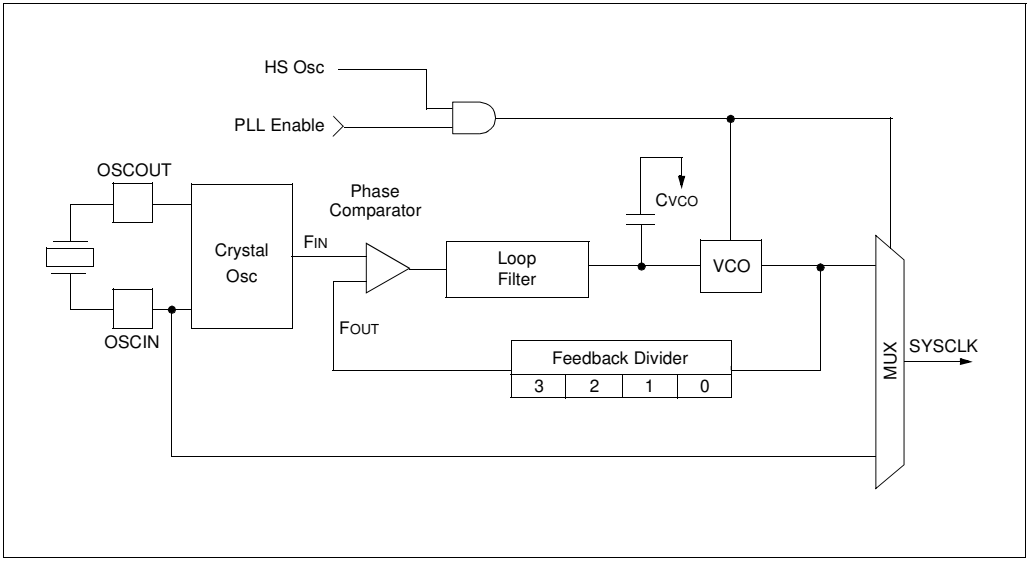

## 2.5 HS4 (PLL)

A Phase Lock Loop (PLL) circuit is provided as a software programmable option for users that want to multiply the frequency of the incoming crystal oscillator signal by 4. For an input clock frequency of 6 MHz, the internal clock frequency will be multiplied to 24 MHz. This is useful for customers who are concerned with EMI due to high frequency crystals.

The PLL is enabled by configuring HS oscillator mode and setting the PLLEN bit in the OSCON register. If HS oscillator mode is not selected, or PLLEN bit in OSCCON register is clear, the PLL is not enabled and the system clock will come directly from OSC1. HS oscillator mode is the default for PIC18C601/801. In all other modes, the PLLEN bit and the SCS1 bit are forced to '0'.

A PLL lock timer is used to ensure that the PLL has locked before device execution starts. The PLL lock timer has a time-out, referred to as TPLL.

**FIGURE 2-4: PLL BLOCK DIAGRAM**



## 2.6 Oscillator Switching Feature

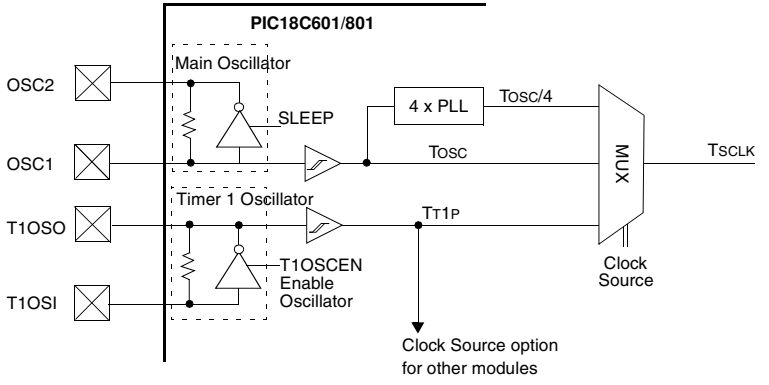
PIC18C601/801 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low frequency clock source. For PIC18C601/801 devices, this alternate clock source is the Timer1 oscillator. If a low frequency crystal (32 kHz, for example) has been attached to the Timer1 oscillator pins and the Timer1 oscillator has been enabled, the device can switch to a low power execution mode. Figure 2-5 shows a block diagram of the system clock sources.

### 2.6.1 SYSTEM CLOCK SWITCH BIT

The system clock source switching is performed under software control. The system clock switch bit, SCS0 (OSCCON register), controls the clock switching. When the SCS0 bit is '0', the system clock source comes from the main oscillator, selected by the FOSC2:FOSC0 configuration bits in CONFIG1H register. When the SCS0 bit is set, the system clock source will come from the Timer1 oscillator. The SCS0 bit is cleared on all forms of RESET.

| **Note:** | The Timer1 oscillator must be enabled to switch the system clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 control register (T1CON). If the Timer1 oscillator is not enabled, any write to the SCS0 bit will be ignored (SCS0 bit forced cleared) and the main oscillator will continue to be the system clock source. |
|---|---|

**FIGURE 2-5: DEVICE CLOCK SOURCES**




**Note:** I/O pins have diode protection to VDD and VSS.

**REGISTER 2-1: OSCCON REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LOCK | PLLEN | SCS1 | SCS0 |
| bit 7 | | | | | | | bit 0 |

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **LOCK:** Phase Lock Loop Lock Status bit
1 = Phase Lock Loop output is stable as system clock
0 = Phase Lock Loop output is not stable and cannot be used as system clock

bit 2 **PLLEN:** Phase Lock Loop Enable bit
1 = Enable Phase Lock Loop output as system clock
0 = Disable Phase Lock Loop

bit 1 **SCS1:** System Clock Switch bit 1
When PLLEN and LOCK bit are set:
1 = Use PLL output
0 = Use primary oscillator/clock input pin
When PLLEN bit or LOCK bit is cleared:
Bit is forced clear

bit 0 **SCS0:** System Clock Switch bit 0
When T1OSCEN bit is set:
1 = Switch to Timer1 oscillator/clock pin
0 = Use primary oscillator/clock input pin
When T1OSCEN is cleared:
Bit is forced clear

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 2.6.2 OSCILLATOR TRANSITIONS

PIC18C601/801 devices contain circuitry to prevent "glitches" when switching between oscillator sources. Essentially, the circuitry waits for eight rising edges of the clock source that the processor is switching to. This ensures that the new clock source is stable and that its pulse width will not be less than the shortest pulse width of the two clock sources.

A timing diagram indicating the transition from the main oscillator to the Timer1 oscillator is shown in Figure 2-6. The Timer1 oscillator is assumed to be running all the time. After the SCS0 bit is set, the processor is frozen at the next occurring Q1 cycle. After eight synchronization cycles are counted from the Timer1 oscillator, operation resumes. No additional delays are required after the synchronization cycles.

The sequence of events that takes place when switching from the Timer1 oscillator to the main oscillator will depend on the mode of the main oscillator. In addition to eight clock cycles of the main oscillator, additional delays may take place.

If the main oscillator is configured for an external crystal (HS, LP), the transition will take place after an oscillator start-up time (TOST) has occurred. A timing diagram indicating the transition from the Timer1 oscillator to the main oscillator for HS and LP modes is shown in Figure 2-7.