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PIC18(L)F1XK22

20-Pin Flash Microcontrollers with XLP Technology

High-Performance RISC CPU

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 256 bytes Data EEPROM
- Up to 16 Kbytes Linear Program Memory Addressing
- Up to 512 bytes Linear Data Memory Addressing
- Up to 16 MIPS Operation
- 16-bit Wide Instructions, 8-bit Wide Data Path
- Priority Levels for Interrupts
- 31-Level, Software Accessible Hardware Stack
- 8 x 8 Single-Cycle Hardware Multiplier

Flexible Oscillator Structure

- Precision 16 MHz Internal Oscillator Block:
  - Factory calibrated to ± 1%
  - Software selectable frequencies range of 31 kHz to 16 MHz
  - 64 MHz performance available using PLL – no external components required
- Four Crystal modes up to 64 MHz
- Two External Clock modes up to 64 MHz
- 4X Phase Lock Loop (PLL)
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up

Special Microcontroller Features

- 2.3V - 5.5V Operation – PIC18F1XK22
- 1.8V-3.6V Operation – PIC18LF1XK22
- Self-reprogrammable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug via Two Pins

Extreme Low-Power Management PIC18LF1XK22 with XLP Technology

- Sleep mode: 34 nA
- Watchdog Timer: 460 nA
- Timer1 Oscillator: 650 nA @ 32 kHz

Analog Features

- Analog-to-Digital Converter (ADC) module
  - 10-bit resolution, 12 channels
  - Auto-acquisition capability
  - Conversion available during Sleep
- Analog Comparator module:
  - Two rail-to-rail analog comparators
  - Independent input multiplexing
  - Inputs and outputs externally accessible
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive Digital-to-Analog Converter (DAC) with positive and negative reference selection

Peripheral Highlights

- 17 I/O Pins and 1 Input-only Pin:
  - High current sink/source 25 mA/25 mA
  - Programmable weak pull-ups
  - Programmable interrupt-on- change
  - Three external interrupt pins
- Four Timer modules:
  - Three 16-bit timers/counters with prescaler
  - One 8-bit timer/counter with 8-bit period register, prescaler and postscaler
  - Dedicated, low-power Timer1 oscillator
- Enhanced Capture/Compare/PWM (ECCP) module:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and Auto-restart
  - PWM output steering control
- Master Synchronous Serial Port (MSSP) module
  - 3-wire SPI (supports all four SPI modes)
  - I^2C Master and Slave modes (Slave mode address masking)
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter module (EUSART)
  - Supports RS-232, RS-485 and LIN 2.0
  - Auto-Baud Detect
  - Auto Wake-up on Break
- SR Latch (555 Timer) module with:
  - Configurable inputs and outputs
  - Supports mTouch® capacitive sensing applications

PIC18(L)F1XK22 Family Types

Device	Data Sheet Index	Program Memory		Data Memory		Pins	I/O(1)	10-bit A/D Channels	Comparators	Timers 8-bit/16-bit	ECCP	MSSP	EUSART	SR Latch
		Bytes	Words	SRAM (bytes)	Data EEPROM (bytes)									
PIC18(L)F13K22	(1)	8K	4K	256	256	20	18	12-ch	2	1 / 3	1	1	1	Yes
PIC18(L)F14K22	(1)	16K	8K	512	256	20	18	12-ch	2	1 / 3	1	1	1	Yes

Note 1: One pin is input-only.

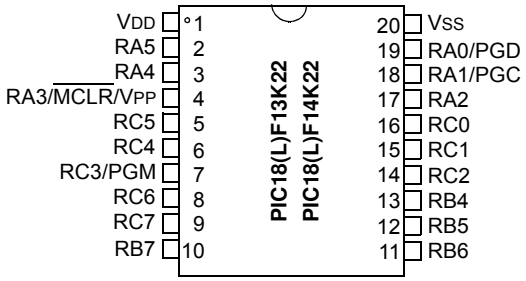
Data Sheet Index: (Unshaded devices are described in this document)

1. DS40001365 PIC18(L)F1XK22 20-Pin Flash Microcontrollers with XLP Technology

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

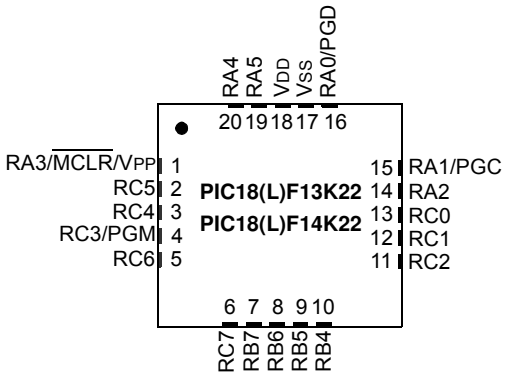
Pin Diagrams

FIGURE 1: 20-PIN PDIP, SSOP, SOIC



Note: See Table 1 for location of all peripheral functions.

FIGURE 2: 20-PIN QFN (4x4)



Note: See Table 1 for location of all peripheral functions.

TABLE 1: 20-PIN ALLOCATION TABLE (PIC18(L)F1XK22)

I/O	20-Pin PDIP/SSOP/SOIC	20-Pin QFN	Analog	Comparator	Reference	ECCP	EUSART	MSSP	SR Latch	Timers	Interrupts	Pull-up	Basic
RA0	19	16	AN0	C1IN+	VREF-/ CVREF(DAC1OUT)	—	—	—	—	—	IOC/INT0	Y	PGD
RA1	18	15	AN1	C12IN0-	VREF+	—	—	—	—	—	IOC/INT1	Y	PGC
RA2	17	14	AN2	C1OUT	—	—	—	—	SRQ	T0CKI	IOC/INT2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$/VPP
RA4	3	20	AN3	—	—	—	—	—	—	—	IOC	Y	OSC2/CLKOUT
RA5	2	19	—	—	—	—	—	—	—	T13CKI	IOC	Y	OSC1/CLKIN
RB4	13	10	AN10	—	—	—	—	SDI/SDA	—	—	IOC	Y	—
RB5	12	9	AN11	—	—	—	RX/DT	—	—	—	IOC	Y	—
RB6	11	8	—	—	—	—	—	SCL/SCK	—	—	IOC	Y	—
RB7	10	7	—	—	—	—	TX/CK	—	—	—	IOC	Y	—
RC0	16	13	AN4	C2IN+	—	—	—	—	—	—	—	—	—
RC1	15	12	AN5	C12IN1-	—	—	—	—	—	—	—	—	—
RC2	14	11	AN6	C12IN2-	—	P1D	—	—	—	—	—	—	—
RC3	7	4	AN7	C12IN3-	—	P1C	—	—	—	—	—	—	PGM
RC4	6	3	—	C2OUT	—	P1B	—	—	SRNQ	—	—	—	—
RC5	5	2	—	—	—	CCP1/P1A	—	—	—	—	—	—	—
RC6	8	5	AN8	—	—	—	—	$\overline{SS}$	—	—	—	—	—
RC7	9	6	AN9	—	—	—	—	SDO	—	—	—	—	—
—	1	18	—	—	—	—	—	—	—	—	—	—	VDD
—	20	17	—	—	—	—	—	—	—	—	—	—	VSS

Table of Contents

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1.0 DEVICE OVERVIEW

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance with the addition of high-endurance, Flash program memory. On top of these features, the PIC18(L)F1XK22 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 XLP TECHNOLOGY

All of the devices in the PIC18(L)F1XK22 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 26.0 "Electrical Specifications"** for values.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18(L)F1XK22 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators
- External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O)
- External RC Oscillator modes with the same pin options as the External Clock modes
- An internal oscillator block which contains a 16 MHz HFINTOSC oscillator and a 31 kHz LFINTOSC oscillator which together provide eight user selectable clock frequencies, from 31 kHz to 16 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the high-speed crystal and internal oscillator modes, which allows clock speeds of up to 64 MHz. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 64 MHz – all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the LFINTOSC. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.2 Other Special Features

- **Memory Endurance:** The Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 10K for program memory and 100K for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-programmability:** These devices can write to their own program memory spaces under internal software control. Using a bootloader routine located in the code protected Boot Block, it is possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18(L)F1XK22 family introduces an optional extension to the PIC18 instruction set, which adds eight new instructions and an Indexed Addressing mode. This extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- **Enhanced CCP module:** In PWM mode, this module provides one, two or four modulated outputs for controlling half-bridge and full-bridge drivers. Other features include:
  - Auto-Shutdown, for disabling PWM outputs on interrupt or other select conditions
  - Auto-Restart, to reactivate outputs once the condition has cleared
  - Output steering to selectively enable one or more of four outputs to provide the PWM signal.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution.
- **10-bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit postscaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 26.0 "Electrical Specifications"** for time-out periods.

1.3 Details on Individual Family Members

Devices in the PIC18(L)F1XK22 family are available in 20-pin packages. Block diagrams for the two groups are shown in Figure 1-1.

The devices are differentiated from each other in the following ways:

1. Flash program memory:
   - 8 Kbytes for PIC18(L)F13K22
   - 16 Kbytes for PIC18(L)F14K22

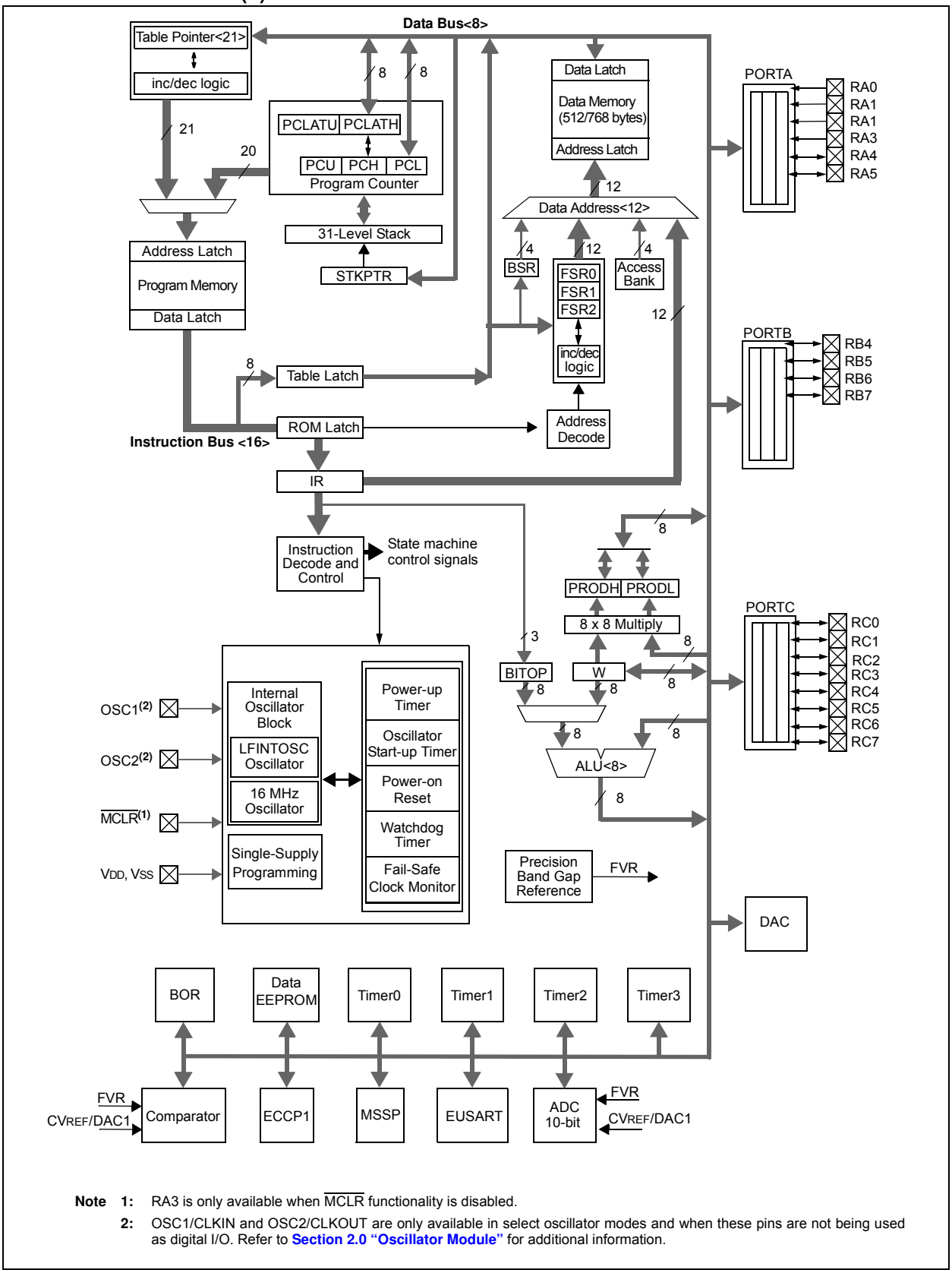
All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1 and I/O description are in Table 1-2.

TABLE 1-1: DEVICE FEATURES FOR THE PIC18(L)F1XK22 (20-PIN DEVICES)

Features	PIC18F13K22	PIC18LF13K22	PIC18F14K22	PIC18LF14K22
Voltage Range (1.8 - 5.5V)	2.3-5.5V	1.8V-3.6V	2.3-5.5V	1.8V-3.6V
Program Memory (Bytes)	8K		16K	
Program Memory (Instructions)	4096		8192	
Data Memory (Bytes)	256		512	
Operating Frequency	DC – 64 MHz			
Interrupt Sources	30			
I/O Ports	Ports A, B, C			
Timers	4			
Enhanced Capture/ Compare/PWM Modules	1			
Serial Communications	MSSP, Enhanced USART			
10-Bit Analog-to-Digital Module	12 Input Channels			
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)			
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled			
Packages	20-Pin PDIP, SSOP, SOIC QFN (4x4x0.9mm)			

FIGURE 1-1: PIC18(L)F1XK22 BLOCK DIAGRAM



Note 1: RA3 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

2: OSC1/CLKIN and OSC2/CLKOUT are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Module"** for additional information.

TABLE 1-2: PIC18(L)F1XK22 PIN SUMMARY

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP/SSOP/SOIC	QFN			
RA0/AN0/CVREF/VREF-/C1IN+/INT0/PGD	19	16			
RA0			I/O	TTL	Digital I/O
AN0			I	Analog	ADC channel 0
CVREF/DAC1OUT			O	Analog	DAC reference voltage output
VREF-			I	Analog	ADC and DAC reference voltage (low) input
C1IN+			I	Analog	Comparator C1 noninverting input
INT0			I	ST	External interrupt 0
PGD			I/O	ST	ICSP™ programming data pin
RA1/AN1/C12IN0-/VREF+/INT1/PGC	18	15			
RA1			I/O	TTL	Digital I/O
AN1			I	Analog	ADC channel 1
C12IN0-			1	Analog	Comparator C1 and C2 inverting input
VREF+			I	Analog	ADC and DAC reference voltage (high) input
INT1			I	ST	External interrupt 1
PGC			I/O	ST	ICSP programming clock pin
RA2/AN2/C1OUT/T0CKI/INT2/SRQ	17	14			
RA2			I/O	ST	Digital I/O
AN2			I	Analog	ADC channel 2
C1OUT			—	CMOS	Comparator C1 output
T0CKI			I	ST	Timer0 external clock input
INT2			I	ST	External interrupt 2
SRQ			O	CMOS	SR latch output
RA3/$\overline{\text{MCLR}}$/VPP	4	1			
RA3			I	ST	Digital input
$\overline{\text{MCLR}}$			I	ST	Active-low Master Clear with internal pull-up
VPP			P	—	High voltage programming input
RA4/AN3/OSC2/CLKOUT	3	20			
RA4			I/O	TTL	Digital I/O
AN3			I	Analog	ADC channel 3
OSC2			O	XTAL	Oscillator crystal output. Connect to crystal or resonator in Crystal Oscillator mode
CLKOUT			O	CMOS	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate
RA5/OSC1/CLKIN/T13CKI	2	19			
RA5			I/O	TTL	Digital I/O
OSC1			I	XTAL	Oscillator crystal input or external clock input ST buffer when configured in RC mode; analog other wise
CLKIN			I	CMOS	External clock source input. Always associated with the pin function OSC1 (See related OSC1/CLKIN, OSC2, CLKOUT pins
T13CKI			I	ST	Timer0 and Timer3 external clock input
RB4/AN10/SDI/SDA	13	10			
RB4			I/O	TTL	Digital I/O
AN10			I	Analog	ADC channel 10
SDI			I	ST	SPI data in
SDA			I/O	ST	I^2C data I/O

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input
O = Output
XTAL = Crystal Oscillator
CMOS = CMOS compatible input or output
I = Input
P = Power

TABLE 1-2: PIC18(L)F1XK22 PIN SUMMARY (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP/SSOP/SOIC	QFN			
RB5/AN11/RX/DT	12	9			
RB5			I/O	TLL	Digital I/O
AN11			I	Analog	ADC channel 11
RX			I	ST	EUSART asynchronous receive
DT			I/O	ST	EUSART synchronous data (see related RX/TX)
RB6/SCK/SCL	11	8			
RB6			I/O	TLL	Digital I/O
SCK			I/O	ST	Synchronous serial clock input/output for SPI mode
SCL			I/O	ST	Synchronous serial clock input/output for I^2C mode
RB7/TX/CK	10	7			
RB7			I/O	TLL	Digital I/O
TX			O	CMOS	EUSART asynchronous transmit
CK			I/O	ST	EUSART synchronous clock (see related RX/DT)
RC0/AN4/C2IN+	16	13			
RC0			I/O	ST	Digital I/O
AN4			I	Analog	ADC channel 4
C2IN+			I	Analog	Comparator C2 noninverting input
RC1/AN5/C12IN-	15	12			
RC1			I/O	ST	Digital I/O
AN5			I	Analog	ADC channel 5
C12IN-			I	Analog	Comparator C1 and C2 inverting input
RC2/AN6/C12IN2-/P1D	14	11			
RC2			I/O	ST	Digital I/O
AN6			I	Analog	ADC channel 6
C12IN2-			I	Analog	Comparator C1 and C2 inverting input
P1D			O	CMOS	Enhanced CCP1 PWM output
RC3/AN7/C12IN3-/P1C/PGM	7	4			
RC3			I/O	ST	Digital I/O
AN7			I	Analog	ADC channel 7
C12IN3-			I	Analog	Comparator C1 and C2 inverting input
P1C			O	CMOS	Enhanced CCP1 PWM output
PGM			I/O	ST	Low-Voltage ICSP Programming enable pin
RC4/C2OUT/P1B/SRNQ	6	3			
RC4			I/O	ST	Digital I/O
C2OUT			O	CMOS	Comparator C2 output
P1B			O	CMOS	Enhanced CCP1 PWM output
SRNQ			O	CMOS	SR latch inverted output
RC5/CCP1/P1A	5	2			
RC5			I/O	ST	Digital I/O
CCP1			I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output
P1A			O	CMOS	Enhanced CCP1 PWM output
RC6/AN8/$\overline{SS}$	8	5			
RC6			I/O	ST	Digital I/O
AN8			I	Analog	ADC channel 8
$\overline{SS}$			I	TTL	SPI slave select input
RC7/AN9/SDO	9	6			
RC7			I/O	ST	Digital I/O
AN9			I	Analog	ADC channel 9
SDO			O	CMOS	SPI data out
VSS	20	17	P	—	Ground reference for logic and I/O pins
VDD	1	18	P	—	Positive supply for logic and I/O pins

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input
O = Output
XTAL = Crystal Oscillator
CMOS = CMOS compatible input or output
I = Input
P = Power

2.0 OSCILLATOR MODULE

2.1 Overview

The oscillator module has a variety of clock sources and features that allow it to be used in a wide range of applications, maximizing performance and minimizing power consumption. Figure 2-1 illustrates a block diagram of the oscillator module.

Key features of the oscillator module include:

- System Clocks
- System Clock Selection
  - Primary External Oscillator
  - Secondary External Oscillator
  - Internal Oscillator
- Oscillator Start-up Timer
- System Clock Selection
- Clock Switching
- 4x Phase Lock Loop Frequency Multiplier
- CPU Clock Divider
- Two-Speed Start-up Mode
- Fail-Safe Clock Monitoring

2.2 System Clocks

The PIC18(L)F1XK22 can be operated in 13 different oscillator modes. The user can program these using the available Configuration bits. In addition, clock support functions such as Fail-Safe and two Start-up can also be configured.

The available Primary oscillator options include:

- External Clock, low power (ECL)
- External Clock, medium power (ECM)
- External Clock, high power (ECH)
- External Clock, low power, CLKOUT function on RA4/OSC2 (ECCLKOUTL)
- External Clock, medium power, CLKOUT function on RA4/OSC2 (ECCLKOUTM)
- External Clock, high power, CLKOUT function on RA4/OSC2 (ECCLKOUTH)
- External Crystal (XT)
- High-speed Crystal (HS)
- Low-power crystal (LP)
- External Resistor/Capacitor (EXTRC)
- External RC, CLKOUT function on RA4/OSC2
- 31.25 kHz – 16 MHz internal oscillator (INTOSC)
- 31.25 kHz – 16 MHz internal oscillator, CLKOUT function on RA4/OSC2

Additionally, the 4x PLL may be enabled in hardware or software (under certain conditions) for increased oscillator speed.

2.3 System Clock Selection

The SCS bits of the OSCCON register select between the following clock sources:

- Primary External Oscillator
- Secondary External Oscillator
- Internal Oscillator

Note: The frequency of the system clock will be referred to as FOSC throughout this document.

TABLE 2-1: SYSTEM CLOCK SELECTION

Configuration	Selection
SCS <1:0>	System Clock
1x	Internal Oscillator
01	Secondary External Oscillator
00 (Default after Reset)	Oscillator defined by FOSC<3:0>

The default state of the SCS bits sets the system clock to be the oscillator defined by the FOSC bits of the CONFIG1H Configuration register. The system clock will always be defined by the FOSC bits until the SCS bits are modified in software.

When the Internal Oscillator is selected as the system clock, the IRCF bits of the OSCCON register and the INTSRC bit of the OSCTUNE register will select either the LFINTOSC or the HFINTOSC. The LFINTOSC is selected when the IRCF<2:0> = 000 and the INTSRC bit is clear. All other combinations of the IRCF bits and the INTSRC bit will select the HFINTOSC as the system clock.

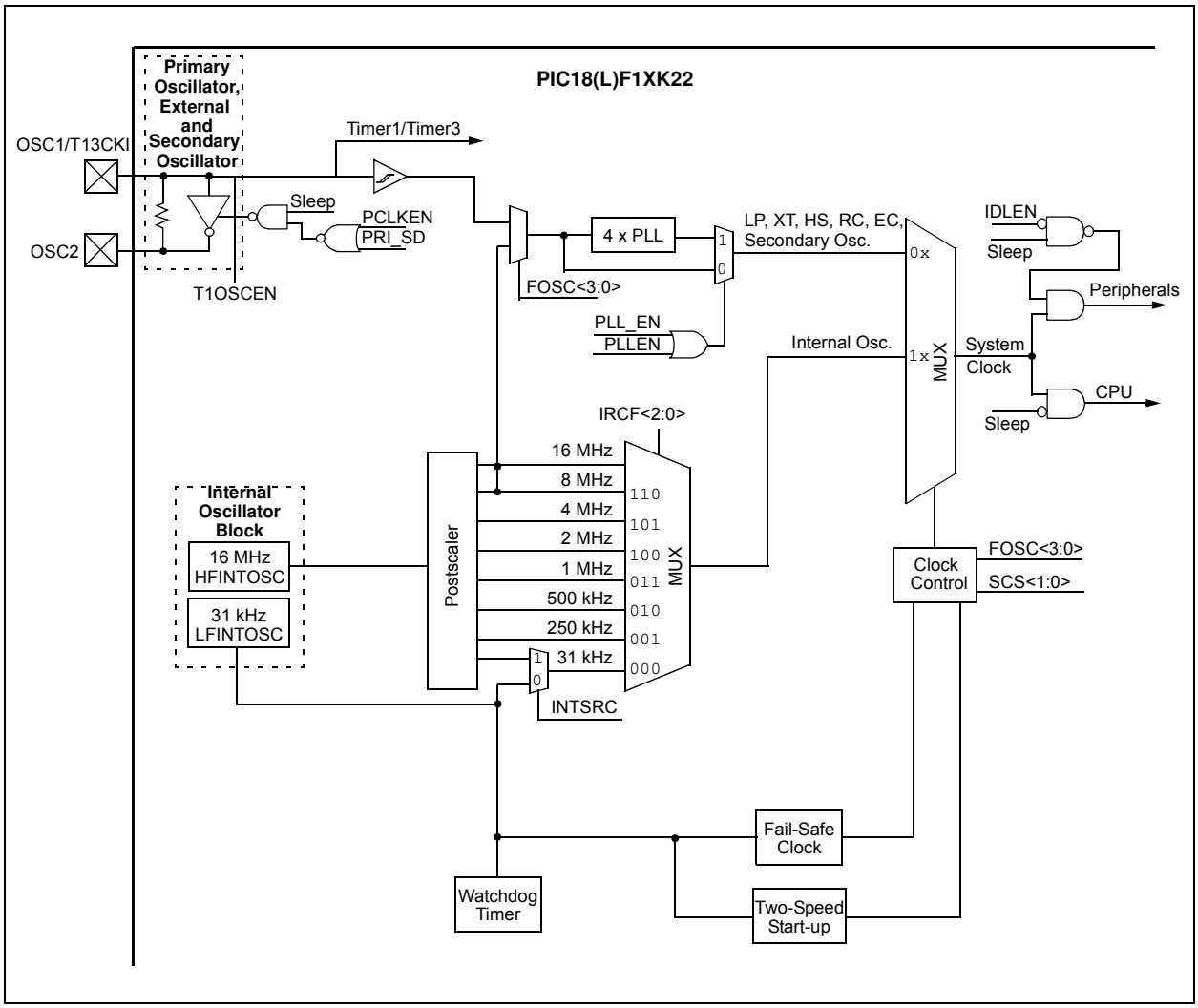
2.4 Primary External Oscillator

The Primary External Oscillator's mode of operation is selected by setting the FOSC<3:0> bits of the CONFIG1H Configuration register. The oscillator can be set to the following modes:

- LP: Low-Power Crystal
- XT: Crystal/Ceramic Resonator
- HS: High-Speed Crystal Resonator
- RC: External RC Oscillator
- EC: External Clock

Additionally, the Primary External Oscillator may be shut down under firmware control to save power.

FIGURE 2-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



Note:	If using a low-frequency external oscillator and want to multiple it by 4 via PLL, the ideal input frequency is from 4 MHz to 16 MHz.

2.4.1 PRIMARY EXTERNAL OSCILLATOR SHUTDOWN

The Primary External Oscillator can be enabled or disabled via software. To enable software control of the Primary External Oscillator, the PCLKEN bit of the CONFIG1H Configuration register must be set. With the PCLKEN bit set, the Primary External Oscillator is controlled by the PRI_SD bit of the OSCCON2 register. The Primary External Oscillator will be enabled when the PRI_SD bit is set, and disabled when the PRI_SD bit is clear.

Note:	The Primary External Oscillator cannot be shut down when it is selected as the System Clock. To shut down the oscillator, the system clock source must be either the Secondary Oscillator or the Internal Oscillator.

2.4.2 LP, XT AND HS OSCILLATOR MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 2-2). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

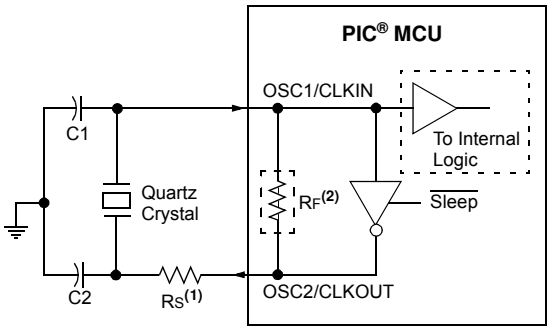
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 2-2 and Figure 2-3 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 2-2: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)

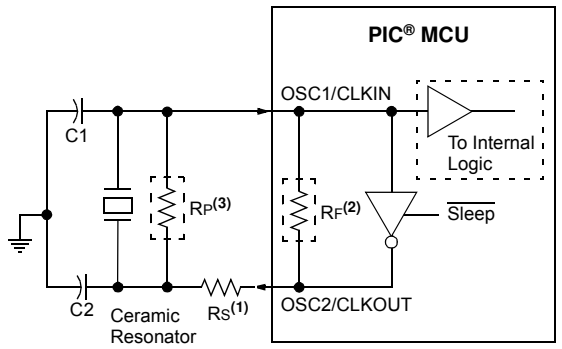


Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Note 1:	Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
2:	Always verify oscillator performance over the VDD and temperature range that is expected for the application.
3:	For oscillator design assistance, reference the following Microchip Applications Notes: • *AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC® and PICmicro® Devices* (DS00826) • *AN849, Basic PICmicro® Oscillator Design* (DS00849) • *AN943, Practical PICmicro® Oscillator Analysis and Design* (DS00943) • *AN949, Making Your Oscillator Work* (DS00949)

FIGURE 2-3: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

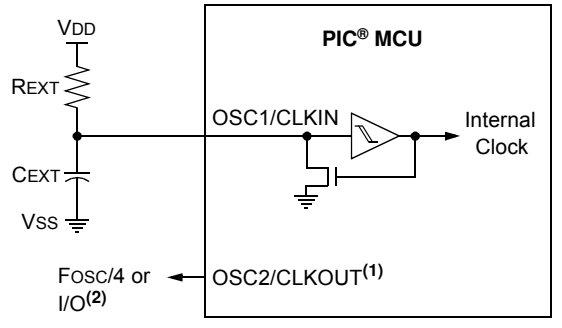
2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

2.4.3 EXTERNAL RC

The External Resistor-Capacitor (RC) mode supports the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. In RC mode, the RC circuit connects to OSC1, allowing OSC2 to be configured as an I/O or as CLKOUT. The CLKOUT function is selected by the FOSC bits of the CONFIG1H Configuration register. When OSC2 is configured as CLKOUT, the frequency at the pin is the frequency of the RC oscillator divided by 4. Figure 2-4 shows the external RC mode connections.

FIGURE 2-4: EXTERNAL RC MODES



Recommended values: 10 kΩ ≤ REXT ≤ 100 kΩ
CEXT > 20 pF

Note 1: Alternate pin functions are listed in **Section 1.0 "Device Overview"**.

2: Output depends upon RC or RCIO clock mode.

The RC oscillator frequency is a function of the supply voltage, the resistor REXT, the capacitor CEXT and the operating temperature. Other factors affecting the oscillator frequency are:

- Input threshold voltage variation
- Component tolerances
- Variation in capacitance due to packaging

2.4.4 EXTERNAL CLOCK

The External Clock (EC) mode allows an externally generated logic level clock to be used as the system's clock source. When operating in this mode, the external clock source is connected to the OSC1 allowing OSC2 to be configured as an I/O or as CLKOUT. The CLKOUT function is selected by the FOSC bits of the CONFIG1H Configuration register. When OSC2 is configured as CLKOUT, the frequency at the pin is the frequency of the EC oscillator divided by 4.

Three different power settings are available for EC mode. The power settings allow for a reduced IDD of the device, if the EC clock is known to be in a specific range. If there is an expected range of frequencies for the EC clock, select the power mode for the highest frequency.

EC	Low power	0 – 250 kHz
EC	Medium power	250 kHz – 4 MHz
EC	High power	4 – 64 MHz

2.5 Secondary External Oscillator

The Secondary External Oscillator is designed to drive an external 32.768 kHz crystal. This oscillator is enabled or disabled by the T1OSCEN bit of the T1CON register. See **Section 10.0 "Timer1 Module"** for more information.

2.6 Internal Oscillator

The internal oscillator module contains two independent oscillators which are:

- LFINTOSC: Low-Frequency Internal Oscillator
- HFINTOSC: High-Frequency Internal Oscillator

When operating with either oscillator, OSC1 will be an I/O and OSC2 will be either an I/O or CLKOUT. The CLKOUT function is selected by the FOSC bits of the CONFIG1H Configuration register. When OSC2 is configured as CLKOUT, the frequency at the pin is the frequency of the Internal Oscillator divided by 4.

2.6.1 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is a 31 kHz internal clock source. The LFINTOSC oscillator is the clock source for:

- Power-up Timer
- Watchdog Timer
- Fail-Safe Clock Monitor

The LFINTOSC is enabled when any of the following conditions are true:

- Power-up Timer is enabled (PWRTEN = 0)
- Watchdog Timer is enabled (WDTEN = 1)
- Watchdog Timer is enabled by software (WDTEN = 0 and SWDTEN = 1)
- Fail-Safe Clock Monitor is enabled (FCMEM = 1)
- SCS1 = 1 and IRCF<2:0> = 000 and INTSRC = 0
- FOSC<3:0> selects the internal oscillator as the primary clock and IRCF<2:0> = 000 and INTSRC = 0
- IESO = 1 (Two-Speed Start-up) and IRCF<2:0> = 000 and INTSRC = 0

2.6.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a precision oscillator that is factory-calibrated to operate at 16 MHz. The output of the HFINTOSC connects to a postscaler and a multiplexer (see Figure 2-1). One of eight frequencies can be selected using the IRCF<2:0> bits of the OSCCON register. The following frequencies are available from the HFINTOSC:

- 16 MHZ
- 8 MHZ
- 4 MHZ
- 2 MHZ
- 1 MHZ (Default after Reset)
- 500 kHz
- 250 kHz
- 31 kHz

The HFIOFS bit of the OSCCON register indicates whether the HFINTOSC is stable.

Note 1: Selecting 31 kHz from the HFINTOSC oscillator requires IRCF<2:0> = 000 and the INTSRC bit of the OSCTUNE register to be set. If the INTSRC bit is clear, the system clock will come from the LFINTOSC.

2: Additional adjustments to the frequency of the HFINTOSC can made via the OSCTUNE registers. See Register 2-3 for more details.

The HFINTOSC is enabled if any of the following conditions are true:

- SCS1 = 1 and IRCF<2:0> ≠ 000
- SCS1 = 1 and IRCF<2:0> = 000 and INTSRC = 1
- FOSC<3:0> selects the internal oscillator as the primary clock and
  - IRCF<2:0> ≠ 000 or
  - IRCF<2:0> = 000 and INTSRC = 1
- IESO = 1 (Two-Speed Start-up) and
  - IRCF<2:0> ≠ 000 or
  - IRCF<2:0> = 000 and INTSRC = 1
- FCMEM = 1 (Fail-Safe Clock Monitoring) and
  - IRCF<2:0> ≠ 000 or
  - IRCF<2:0> = 000 and INTSRC = 1

2.7 Oscillator Control

The Oscillator Control (OSCCON) (Register 2-1) and the Oscillator Control 2 (OSCCON2) (Register 2-2) registers control the system clock and frequency selection options.

REGISTER 2-1: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R-q	R-0	R/W-0	R/W-0
IDLEN	IRCF2	IRCF1	IRCF0	OSTS(1)	HFIOFS	SCS1	SCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	q = depends on condition
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IDLEN:** Idle Enable bit
1 = Device enters Idle mode on SLEEP instruction
0 = Device enters Sleep mode on SLEEP instruction

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits
111 = 16 MHz
110 = 8 MHz
101 = 4 MHz
100 = 2 MHz
011 = 1 MHz(3)
010 = 500 kHz
001 = 250 kHz
000 = 31 kHz(2)

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit(1)
1 = Device is running from the clock defined by FOSC<2:0> of the CONFIG1 register
0 = Device is running from the internal oscillator (HFINTOSC or LFINTOSC)

bit 2 **HFIOFS:** HFINTOSC Frequency Stable bit
1 = HFINTOSC frequency is stable
0 = HFINTOSC frequency is not stable

bit 1-0 **SCS<1:0>:** System Clock Select bits
1x = Internal oscillator block
01 = Secondary (Timer1) oscillator
00 = Primary clock (determined by CONFIG1H[FOSC<3:0>]).

Note 1: Reset state depends on state of the IESO Configuration bit.
2: Source selected by the INTSRC bit of the OSCTUNE register, see text.
3: Default output frequency of HFINTOSC on Reset.

REGISTER 2-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R-x
—	—	—	—	—	PRI_SD	HFIOFL	LFIOFS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	q = depends on condition
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **PRI_SD:** Primary Oscillator Drive Circuit shutdown bit
1 = Oscillator drive circuit on
0 = Oscillator drive circuit off (zero power)

bit 1 **HFIOFL:** HFINTOSC Frequency Locked bit
1 = HFINTOSC is in lock
0 = HFINTOSC has not yet locked

bit 0 **LFIOFS:** LFINTOSC Frequency Stable bit
1 = LFINTOSC is stable
0 = LFINTOSC is not stable

2.7.1 OSCTUNE REGISTER

The HFINTOSC is factory-calibrated, but can be adjusted in software by writing to the TUN<5:0> bits of the OSCTUNE register (Register 2-3).

The default value of the TUN<5:0> is '000000'. The value is a 6-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift, while giving no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. The operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

The OSCTUNE register also implements the INTSRC and PLLEN bits, which control certain features of the internal oscillator block.

The INTSRC bit allows users to select which internal oscillator provides the clock source when the 31 kHz frequency option is selected. This is covered in greater detail in **Section 2.6.1 "LFINTOSC"**.

The PLLEN bit controls the operation of the frequency multiplier. For more details about the function of the PLLEN bit see **Section 2.10 "4x Phase Lock Loop Frequency Multiplier"**.

REGISTER 2-3: OSCTUNE: OSCILLATOR TUNING REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTSRC	PLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **INTSRC:** Internal Oscillator Low-Frequency Source Select bit
1 = 31.25 kHz device clock derived from 16 MHz HFINTOSC source (divide-by-512 enabled)
0 = 31 kHz device clock derived directly from LFINTOSC internal oscillator

bit 6 **PLLEN:** Frequency Multiplier PLL bit
1 = PLL enabled (for HFINTOSC 8 MHz and 16 MHz only)
0 = PLL disabled

bit 5-0 **TUN<5:0>:** Frequency Tuning bits
011111 = Maximum frequency
011110 =
• • •
000001 =
000000 = Oscillator module is running at the factory-calibrated frequency.
111111 =
• • •
100000 = Minimum frequency

2.8 Oscillator Start-up Timer

The Primary External Oscillator, when configured for LP, XT or HS modes, incorporates an Oscillator Start-up Timer (OST). The OST ensures that the oscillator starts and provides a stable clock to the oscillator module. The OST times out when 1024 oscillations on OSC1 have occurred. During the OST period, with the system clock set to the Primary External Oscillator, the program counter does not increment suspending program execution. The OST period will occur following:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Wake-up from Sleep
- Oscillator being enabled
- Expiration of Power-up Timer (PWRT)

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Start-up mode can be selected. See **Section 2.11 "Two-Speed Start-up Mode"** for more information.

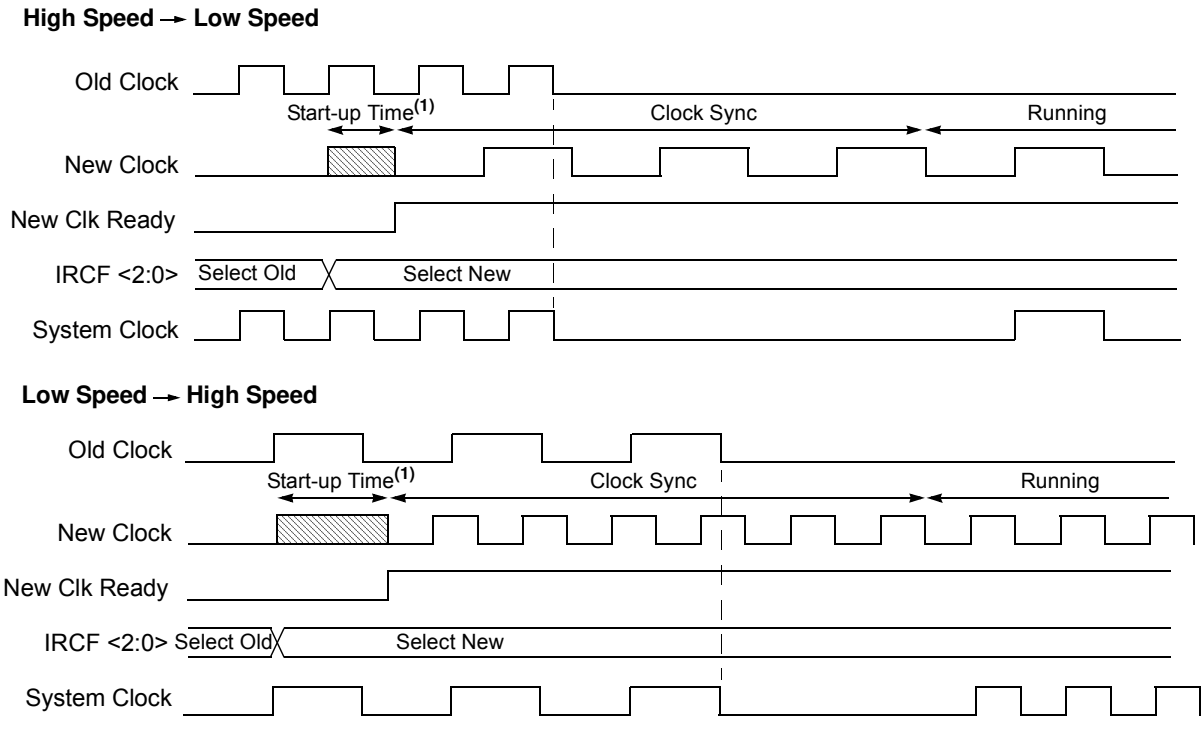
2.9 Clock Switching

The device contains circuitry to prevent clock "glitches" due to a change of the system clock source. To accomplish this, a short pause in the system clock occurs during the clock switch. If the new clock source is not stable (e.g., OST is active), the device will continue to execute from the old clock source until the new clock source becomes stable. The timing of a clock switch is as follows:

1. SCS<1:0> bits of the OSCCON register are modified.
2. The system clock will continue to operate from the old clock until the new clock is ready.
3. Clock switch circuitry waits for two consecutive rising edges of the old clock after the new clock is ready.
4. The system clock is held low, starting at the next falling edge of the old clock.
5. Clock switch circuitry waits for an additional two rising edges of the new clock.
6. On the next falling edge of the new clock, the low hold on the system clock is release and the new clock is switched in as the system clock.
7. Clock switch is complete.

Refer to Figure 2-5 for more details.

FIGURE 2-5: CLOCK SWITCH TIMING



Note 1: Start-up time includes TOST (1024 TOSC) for external clocks, plus TPLL (approx. 2 ms) for HSPLL mode.

TABLE 2-2: EXAMPLES OF DELAYS DUE TO CLOCK SWITCHING

Switch From	Switch To	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	Oscillator Warm-up Delay (TWARM)
Sleep/POR	LP, XT, HS	1024 clock cycles
Sleep/POR	EC, RC	8 Clock Cycles

2.10 4x Phase Lock Loop Frequency Multiplier

A Phase Locked Loop (PLL) circuit is provided as an option for users who wish to use a lower-frequency external oscillator or to operate at 32 MHz or 64 MHz with the HFINTOSC. The PLL is designed for an input frequency from 4 MHz to 16 MHz. The PLL multiplies its input frequency by a factor of four when the PLL is enabled. This may be useful for customers who are concerned with EMI, due to high-frequency crystals.

Two bits control the PLL: the PLL_EN bit of the CONFIG1H Configuration register and the PLLEN bit of the OSCTUNE register. The PLL is enabled when the PLL_EN bit is set and it is under software control when the PLL_EN bit is cleared. Refer to Table 2-3 and Table 2-4 for more information.

TABLE 2-3: PLL CONFIGURATION

PLL_EN	PLLEN	PLL Status
1	x	PLL enabled
0	1	PLL enabled
0	0	PLL disabled

TABLE 2-4: PLL CONFIG1H/SOFTWARE ENABLE CLOCK SOURCE RESTRICTIONS

Mode	PLL CONFIG1H Enable (PLL_EN)	PLL Software Enable (PLLEN)
LP	Yes	No
XT	Yes	No
HS	Yes	No
EC	Yes	No
EXTRC	Yes	No
LF INTOSC	No	No
HF INTOSC	8/16 MHz	8/16 MHz

2.11 Two-Speed Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external Oscillator Start-up Timer (OST) and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the OST period, which can reduce the overall power consumption of the device.

Two-Speed Start-up mode is enabled by setting the IESO bit of the CONFIG1H Configuration register. With Two-Speed Start-up enabled, the device will execute instructions using the internal oscillator during the Primary External Oscillator OST period.

When the system clock is set to the Primary External Oscillator and the oscillator is configured for LP, XT or HS modes, the device will not execute code during the OST period. The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator while the OST is active. The system clock will switch back to the Primary External Oscillator after the OST period has expired.

Two-speed Start-up will become active after:

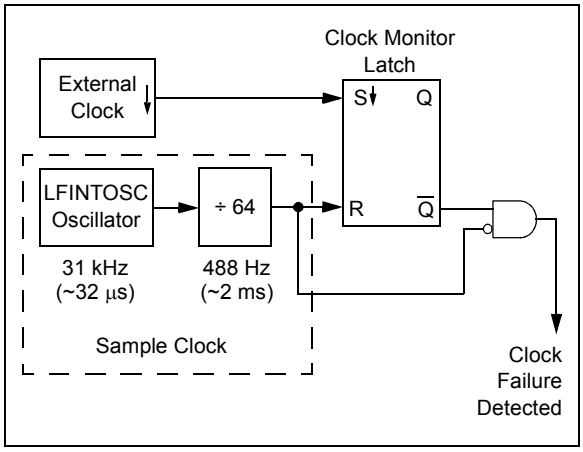
- Power-on Reset (POR)
- Power-up Timer (PWRT), if enabled
- Wake-up from Sleep

The OSTS bit of the OSCCON register reports which oscillator the device is currently using for operation. The device is running from the oscillator defined by the FOSC bits of the CONFIG1H Configuration register when the OSTS bit is set. The device is running from the internal oscillator when the OSTS bit is clear.

2.12 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the CONFIG1H Configuration register. The FSCM is applicable to all external oscillator modes (LP, XT, HS, EC and RC).

FIGURE 2-6: FSCM BLOCK DIAGRAM



2.12.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 2-6. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the primary clock goes low.

2.12.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSCFIF of the PIR2 register. The OSCFIF flag will generate an interrupt if the OSCFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation. An automatic transition back to the failed clock source will not occur.

The internal clock source chosen by the FSCM is determined by the IRCF<2:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

2.12.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared by either one of the following:

- Any Reset
- By toggling the SCS1 bit of the OSCCON register

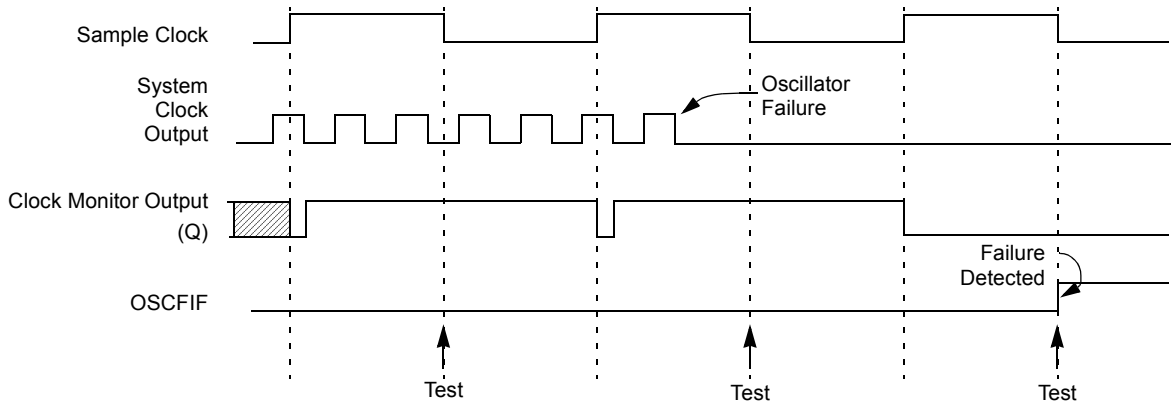
Both of these conditions restart the OST. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared and the device automatically switches over to the external clock source. The Fail-Safe condition need not be cleared before the OSCFIF flag is cleared.

2.12.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note:	Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit of the OSCCON register to verify the oscillator start-up and that the system clock switchover has successfully completed.

FIGURE 2-7: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

TABLE 2-5: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
CONFIG1H	IESO	FCMEN	PCLKEN	PLL_EN	FOSC3	FOSC2	FOSC1	FOSC0	251
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	245
OSCCON	IDLEN	IRCF2	IRCF1	IRCF0	OSTS	HFIOFS	SCS1	SCS0	246
OSCCON2	—	—	—	—	—	PRI_SD	HFIOFL	LFIOFS	246
OSCTUNE	INTSRC	PLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	248
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCLIP	—	TMR3IP	—	248
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCLIE	—	TMR3IE	—	248
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCLIF	—	TMR3IF	—	248
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	246

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by oscillators.
Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

3.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 Enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 4.0 "Flash Program Memory"**. Data EEPROM is discussed separately in **Section 5.0 "Data EEPROM Memory"**.

3.1 Program Memory Organization

PIC18 microcontrollers implement a 21-bit program counter, which is capable of addressing a 2-Mbyte Program Memory (PC) space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

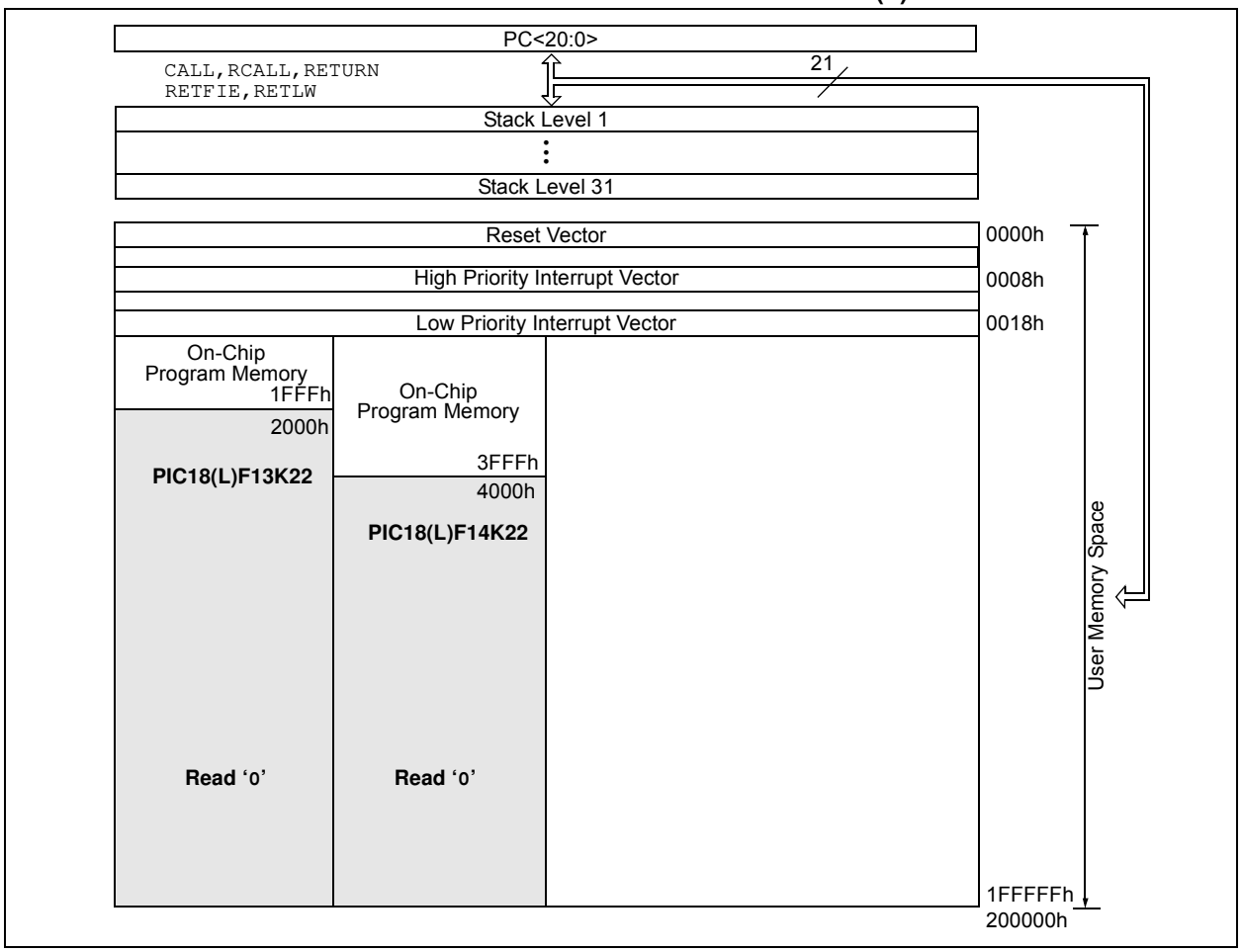
This family of devices contain the following:

- PIC18(L)F13K22: 8 Kbytes of Flash Memory, up to 4,096 single-word instructions
- PIC18(L)F14K22: 16 Kbytes of Flash Memory, up to 8,192 single-word instructions

PIC18 devices have two interrupt vectors and one Reset vector. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory map for PIC18(L)F1XK22 devices is shown in Figure 3-1. Memory block details are shown in Figure 3-2.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC18(L)F1XK22 DEVICES



3.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21-bit wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see **Section 3.1.4.1 "Computed GOTO"**).

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit (LSb) of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

The CALL, RCALL, GOTO and program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

3.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack (TOS) Special File Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL type instruction causes a push onto the stack; the Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack; the contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

The Stack Pointer is initialized to '00000' after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of '00000'; this is only a Reset value. Status bits indicate if the stack is full or has overflowed or has underflowed.

3.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 3-2). This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the global interrupt enable bits while accessing the stack to prevent inadvertent stack corruption.

FIGURE 3-2: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS