



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MICROCHIP

**PIC18F46J11 Family
Data Sheet**

28/44-Pin, Low-Power,
High-Performance Microcontrollers
with nanoWatt XLP Technology

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2011, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-60932-959-4

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==**



PIC18F46J11 FAMILY

28/44-Pin, Low-Power, High-Performance Microcontrollers

Power Management Features with nanoWatt XLP for Extreme Low Power:

- Deep Sleep mode: CPU off, Peripherals off, Currents Down to 13 nA and 850 nA with RTCC
 - Able to wake-up on external triggers, programmable WDT or RTCC alarm
 - Ultra Low-Power Wake-up (ULPWU)
- Sleep mode: CPU off, Peripherals off, SRAM on, Fast Wake-up, Currents Down to 105 nA Typical
- Idle: CPU off, Peripherals on, Currents Down to 2.3 μ A Typical
- Run: CPU on, Peripherals on, Currents Down to 6.2 μ A Typical
- Timer1 Oscillator/w RTCC: 1 μ A, 32 kHz Typical
- Watchdog Timer: 813 nA, 2V Typical

Special Microcontroller Features:

- 5.5V Tolerant Inputs (digital only pins)
- Low-Power, High-Speed CMOS Flash Technology
- C Compiler Optimized Architecture for Re-Entrant Code
- Priority Levels for Interrupts
- Self-Programmable under Software Control
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Operating Voltage Range of 2.0V to 3.6V
- On-Chip 2.5V Regulator
- Flash Program Memory of 10,000 Erase/Write Cycles Minimum and 20-Year Data Retention

Peripheral Highlights:

- Peripheral Pin Select:
 - Allows independent I/O mapping of many peripherals
 - Continuous hardware integrity checking and safety interlocks prevent unintentional configuration changes
- Hardware Real-Time Clock and Calendar (RTCC):
 - Provides clock, calendar and alarm functions
- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)

Peripheral Highlights (Continued):

- Four Programmable External Interrupts
- Four Input Change Interrupts
- Two Enhanced Capture/Compare/PWM (ECCP) modules:
 - One, two or four PWM outputs
 - Selectable polarity
 - Programmable dead time
 - Auto-shutdown and auto-restart
 - Pulse steering control
- Two Master Synchronous Serial Port (MSSP) modules featuring:
 - 3-wire SPI (all 4 modes)
 - 1024-byte SPI Direct Memory Access (DMA) channel
 - I²C™ Master and Slave modes
- 8-Bit Parallel Master Port/Enhanced Parallel Slave Port
- Two-Rail – Rail Analog Comparators with Input Multiplexing
- 10-Bit, up to 13-Channel Analog-to-Digital (A/D) Converter module:
 - Auto-acquisition capability
 - Conversion available during Sleep
 - Self-Calibration
- High/Low-Voltage Detect module
- Charge Time Measurement Unit (CTMU):
 - Supports capacitive touch sensing for touch screens and capacitive switches
 - Provides a Precise Resolution Time Measurement for Both Flow Measurement and Simple Temperature Sensing
- Two Enhanced USART modules:
 - Supports RS-485, RS-232 and LIN/J2602
 - Auto-wake-up on Start bit
- Auto-Baud Detect

Flexible Oscillator Structure:

- 1% Accurate High-Precision Internal Oscillator
- Two External Clock modes, up to 48 MHz (12 MIPS)
- Low-Power 31 kHz Internal RC Oscillator
- Tunable Internal Oscillator (31 kHz to 8 MHz, $\pm 0.15\%$ Typical, $\pm 1\%$ Max).
- 4x PLL Option
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if any clock stops
- Two-Speed Oscillator Start-up
- Programmable Reference Clock Output Generator

PIC18F46J11 FAMILY

PIC18F/LF ⁽¹⁾ Device	Pins	Program Memory (bytes)	SRAM (bytes)	Remappable Pins	Timers 8/16-Bit	ECCP/(PWM)	EUSART	MSSP		10-Bit A/D (ch)	Comparators	Deep Sleep	PMP/PSP	CTMU	RTCC	
								SPI w/DMA	I ² C™							
PIC18F24J11	28	16K	3776	19	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y
PIC18F25J11	28	32K	3776	19	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y
PIC18F26J11	28	64K	3776	19	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y
PIC18F44J11	44	16K	3776	25	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y
PIC18F45J11	44	32K	3776	25	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y
PIC18F46J11	44	64K	3776	25	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y
PIC18LF24J11	28	16K	3776	19	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y
PIC18LF25J11	28	32K	3776	19	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y
PIC18LF26J11	28	64K	3776	19	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y
PIC18LF44J11	44	16K	3776	25	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y
PIC18LF45J11	44	32K	3776	25	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y
PIC18LF46J11	44	64K	3776	25	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y

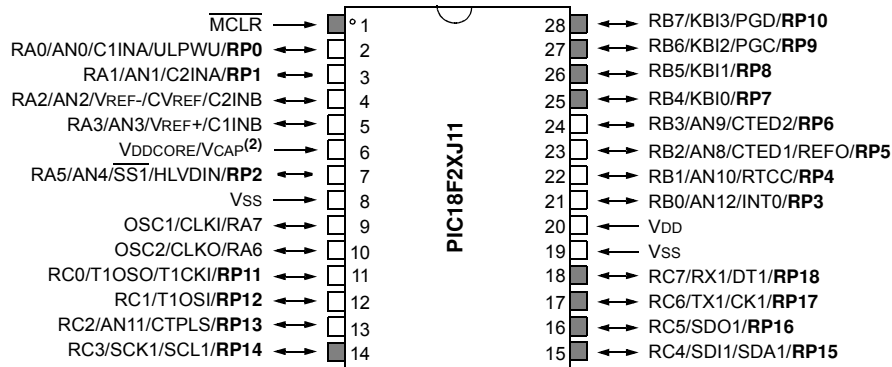
Note 1: See [Section 1.3 “Details on Individual Family Devices”](#), [Section 4.6 “Deep Sleep Mode”](#) and [Section 26.3 “On-Chip Voltage Regulator”](#) for details describing the functional differences between PIC18F and PIC18LF variants in this device family.

PIC18F46J11 FAMILY

Pin Diagrams

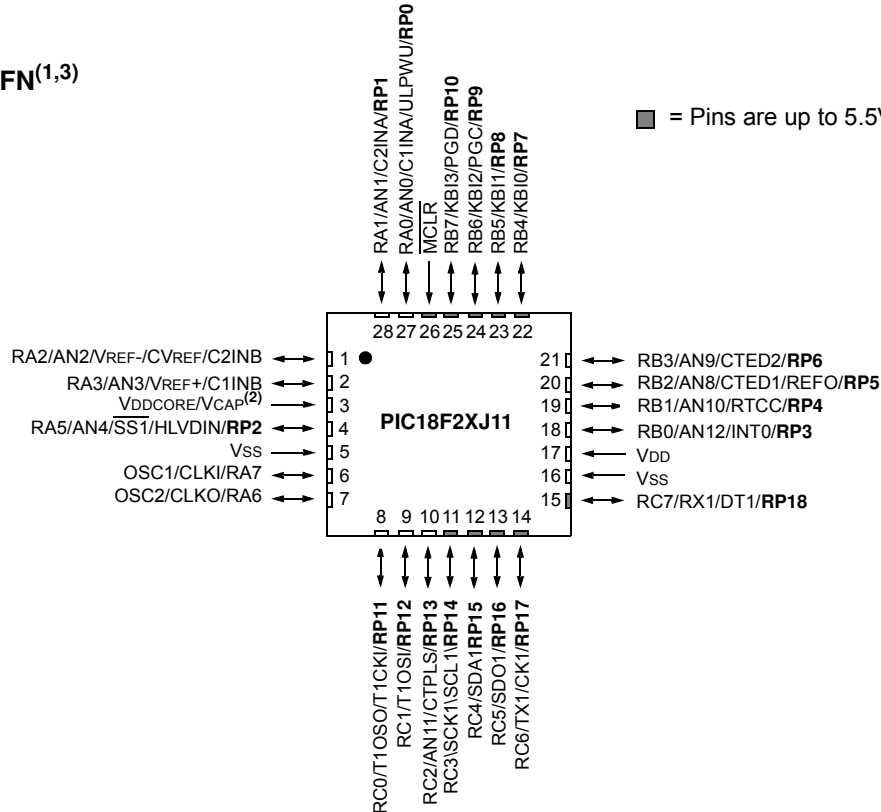
28-Pin SPDIP/SOIC/SSOP⁽¹⁾

■ = Pins are up to 5.5V tolerant



28-Pin QFN^(1,3)

■ = Pins are up to 5.5V tolerant



Legend: RPn represents remappable pins.

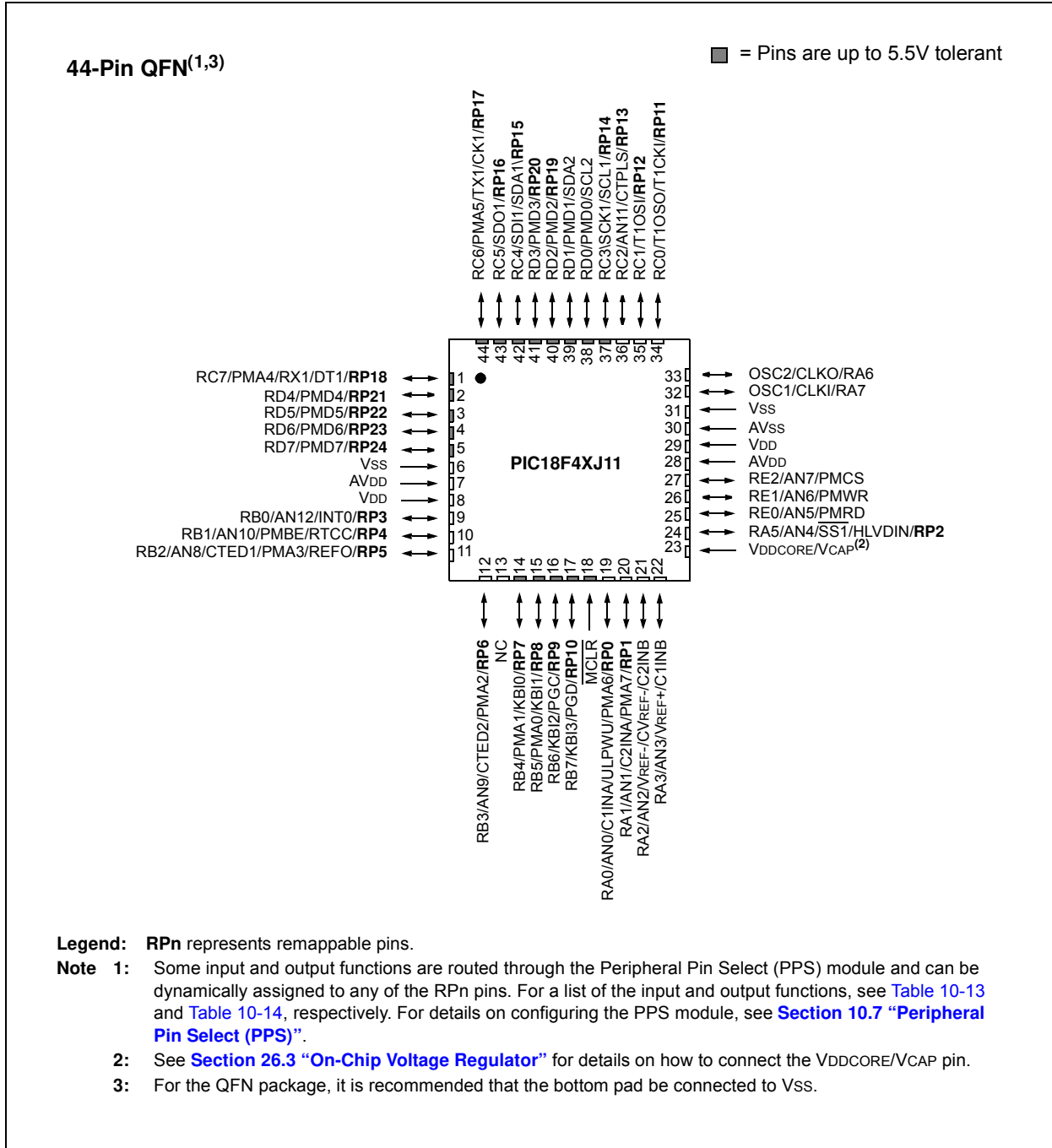
Note 1: Some input and output functions are routed through the Peripheral Pin Select (PPS) module and can be dynamically assigned to any of the RPn pins. For a list of the input and output functions, see [Table 10-13](#) and [Table 10-14](#), respectively. For details on configuring the PPS module, see [Section 10.7 "Peripheral Pin Select \(PPS\)"](#).

2: See [Section 26.3 "On-Chip Voltage Regulator"](#) for details on how to connect the VDDCORE/VCAP pin.

3: For the QFN package, it is recommended that the bottom pad be connected to Vss.

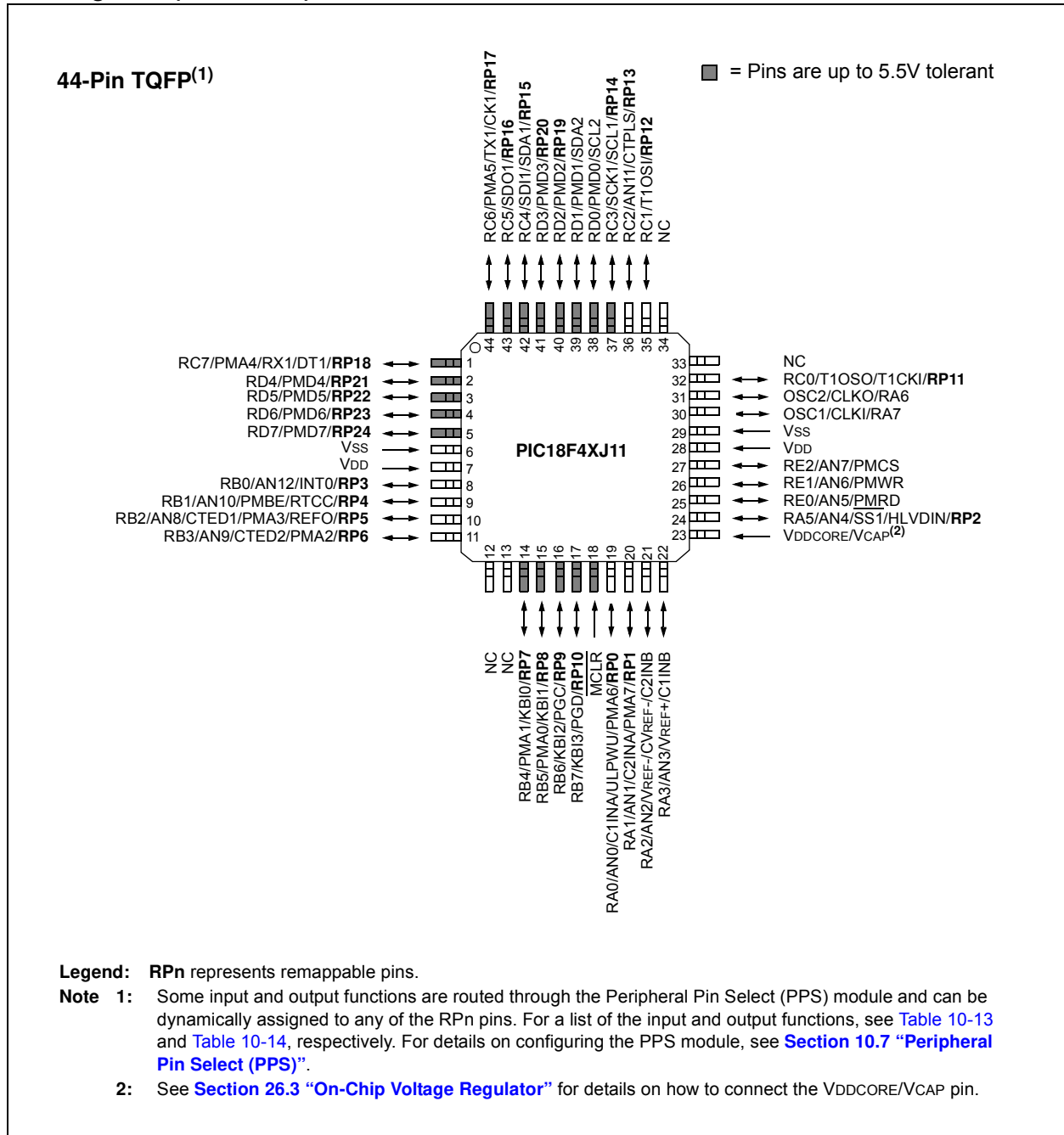
PIC18F46J11 FAMILY

Pin Diagrams (Continued)



PIC18F46J11 FAMILY

Pin Diagrams (Continued)



PIC18F46J11 FAMILY

Table of Contents

Device Overview	11
Guidelines for Getting Started with PIC18FJ Microcontrollers	31
Oscillator Configurations	37
Low-Power Modes	47
Reset	63
Memory Organization	77
Flash Program Memory	103
8 x 8 Hardware Multiplier	113
Interrupts	115
I/O Ports	131
Parallel Master Port (PMP)	171
Timer0 Module	197
Timer1 Module	201
Timer2 Module	213
Timer3 Module	215
Timer4 Module	225
Real-Time Clock and Calendar (RTCC)	227
Enhanced Capture/Compare/PWM (ECCP) Module	247
Master Synchronous Serial Port (MSSP) Module	271
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	327
10-bit Analog-to-Digital Converter (A/D) Module	351
Comparator Module	361
Comparator Voltage Reference Module	369
High/Low Voltage Detect (HLVD)	373
Charge Time Measurement Unit (CTMU)	379
Special Features of the CPU	395
Instruction Set Summary	413
Development Support	463
Electrical Characteristics	467
Packaging Information	507
Appendix A: Revision History	519
Appendix B: Device Differences	519
The Microchip Web Site	533
Customer Change Notification Service	533
Customer Support	533
Reader Response	534
Product Identification System	535

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com to receive the most current information on all of our products.

PIC18F46J11 FAMILY

NOTES:

PIC18F46J11 FAMILY

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F24J11
- PIC18F25J11
- PIC18F26J11
- PIC18F44J11
- PIC18F45J11
- PIC18F46J11
- PIC18LF24J11
- PIC18LF25J11
- PIC18LF26J11
- PIC18LF44J11
- PIC18LF45J11
- PIC18LF46J11

1.1 Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F46J11 family incorporate a range of features that can significantly reduce power consumption during operation. Key features are:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal RC oscillator, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operational requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the users to incorporate power-saving ideas into their application's software design.

1.1.2 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F46J11 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes using crystals or ceramic resonators.
- Two External Clock modes offering the option of a divide-by-4 clock output.
- An internal oscillator block, which provides an 8 MHz clock and an INTRC source (approximately 31 kHz, stable over temperature and VDD), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of eight clock frequencies. This option frees an oscillator pin for use as an additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to the high-speed crystal, and external and internal oscillators, providing a clock speed up to 48 MHz.

The internal oscillator block provides a stable reference source that gives the PIC18F46J11 family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset (POR), or wake-up from Sleep mode, until the primary clock source is available.

1.1.3 EXPANDED MEMORY

The PIC18F46J11 family provides ample room for application code, from 16 Kbytes to 64 Kbytes of code space. The Flash cells for program memory are rated to last in excess of 10000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 20 years.

The Flash program memory is readable and writable during normal operation. The PIC18F46J11 family also provides plenty of room for dynamic application data with up to 3.8 Kbytes of data RAM.

PIC18F46J11 FAMILY

1.1.4 EXTENDED INSTRUCTION SET

The PIC18F46J11 family implements the optional extension to the PIC18 instruction set, adding eight new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.

1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device.

The PIC18F46J11 family is also pin compatible with other PIC18 families, such as the PIC18F4620, PIC18F4520 and PIC18F45J10. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining the same feature set.

1.2 Other Special Features

- **Communications:** The PIC18F46J11 family incorporates a range of serial and parallel communication peripherals. This device also includes two independent Enhanced USARTs and two Master Synchronous Serial Port (MSSP) modules, capable of both Serial Peripheral Interface (SPI) and I²C™ (Master and Slave) modes of operation. The device also has a parallel port and can be configured to serve as either a Parallel Master Port (PMP) or as a Parallel Slave Port (PSP).
- **ECCP Modules:** All devices in the family incorporate three Enhanced Capture/Compare/PWM (ECCP) modules to maximize flexibility in control applications. Up to four different time bases may be used to perform several different operations at once. Each of the ECCPs offers up to four PWM outputs, allowing for a total of eight PWMs. The ECCPs also offer many beneficial features, including polarity selection, programmable dead time, auto-shutdown and restart and Half-Bridge and Full-Bridge Output modes.

- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and thus, reducing code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See [Section 29.0 “Electrical Characteristics”](#) for time-out periods.

1.3 Details on Individual Family Devices

Devices in the PIC18F46J11 family are available in 28-pin and 44-pin packages. Block diagrams for the two groups are shown in [Figure 1-1](#) and [Figure 1-2](#). The devices are differentiated from each other in two ways:

- Flash program memory (three sizes: 16 Kbytes for the PIC18FX4J11, 32 Kbytes for PIC18FX5J11 devices and 64 Kbytes for PIC18FX6J11)
- I/O ports (three bidirectional ports on 28-pin devices, five bidirectional ports on 44-pin devices)

All other features for devices in this family are identical. These are summarized in [Table 1-1](#) and [Table 1-2](#).

The pinouts for the PIC18F2XJ11 devices are listed in [Table 1-3](#) and the pinouts for the PIC18F4XJ11 devices are listed in [Table 1-4](#).

The PIC18F46J11 family of devices provides an on-chip voltage regulator to supply the correct voltage levels to the core. Parts designated with an “F” part number (such as PIC18F46J11) have the voltage regulator enabled.

These parts can run from 2.15V-3.6V on VDD, but should have the VDDCORE pin connected to VSS through a low-ESR capacitor. Parts designated with an “LF” part number (such as PIC18LF46J11) do not enable the voltage regulator. For “LF” parts, an external supply of 2.0V-2.7V has to be supplied to the VDDCORE pin with 2.0V-3.6V supplied to VDD (VDDCORE should never exceed VDD).

For more details about the internal voltage regulator, see [Section 26.3 “On-Chip Voltage Regulator”](#).

PIC18F46J11 FAMILY

TABLE 1-1: DEVICE FEATURES FOR THE PIC18F2XJ11 (28-PIN DEVICES)

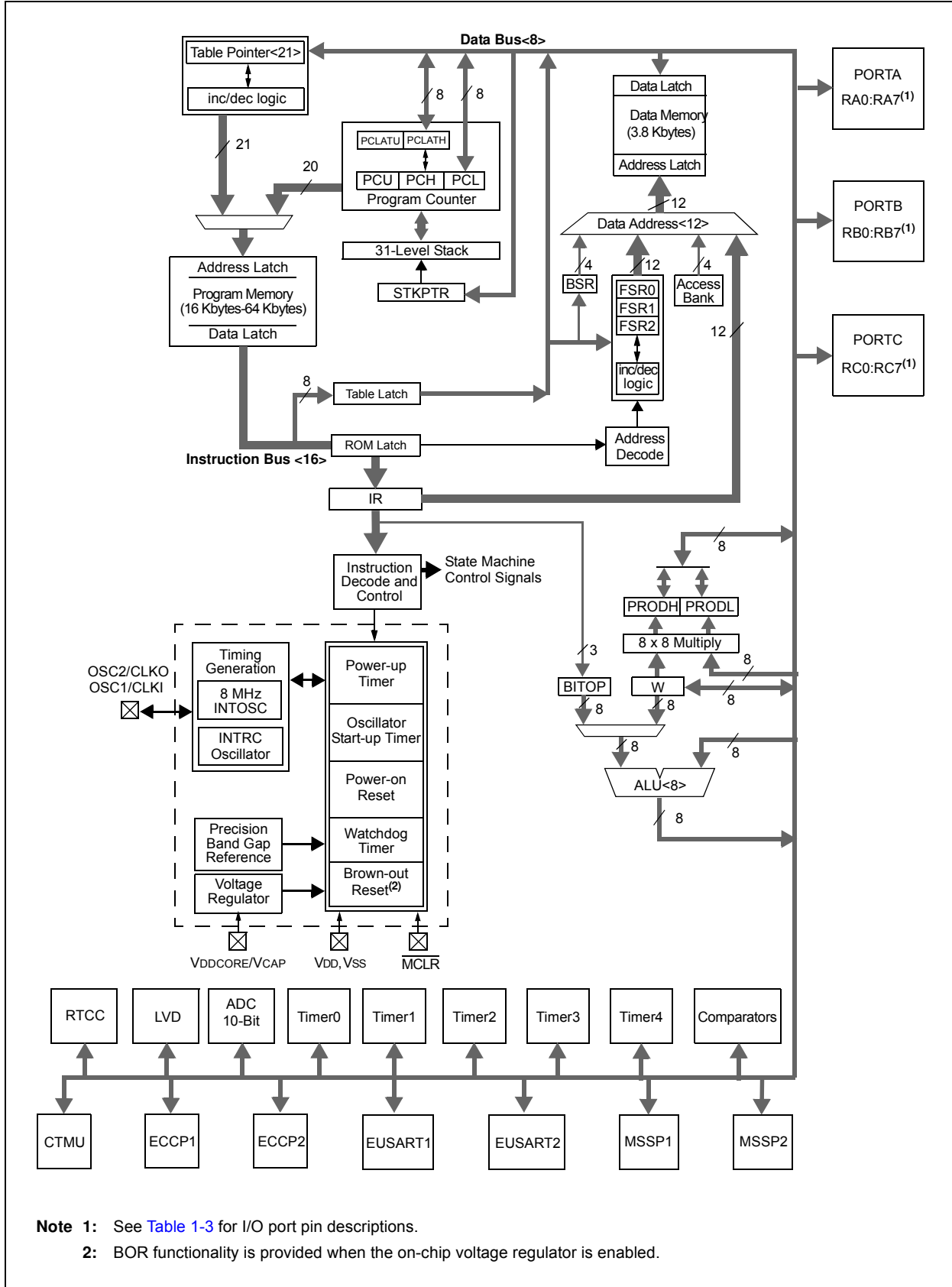
Features	PIC18F24J11	PIC18F25J11	PIC18F26J11
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16K	32K	64K
Program Memory (Instructions)	8,192	16,384	32,768
Data Memory (Bytes)	3.8K	3.8K	3.8K
Interrupt Sources	30		
I/O Ports	Ports A, B, C		
Timers	5		
Enhanced Capture/Compare/PWM Modules	2		
Serial Communications	MSSP (2), Enhanced USART (2)		
Parallel Communications (PMP/PSP)	No		
10-Bit Analog-to-Digital Module	10 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	28-Pin QFN, SOIC, SSOP and SPDIP (300 mil)		

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F4XJ11 (44-PIN DEVICES)

Features	PIC18F44J11	PIC18F45J11	PIC18F46J11
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16K	32K	64K
Program Memory (Instructions)	8,192	16,384	32,768
Data Memory (Bytes)	3.8K	3.8K	3.8K
Interrupt Sources	30		
I/O Ports	Ports A, B, C, D, E		
Timers	5		
Enhanced Capture/Compare/PWM Modules	2		
Serial Communications	MSSP (2), Enhanced USART (2)		
Parallel Communications (PMP/PSP)	Yes		
10-Bit Analog-to-Digital Module	13 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	44-Pin QFN and TQFP		

PIC18F46J11 FAMILY

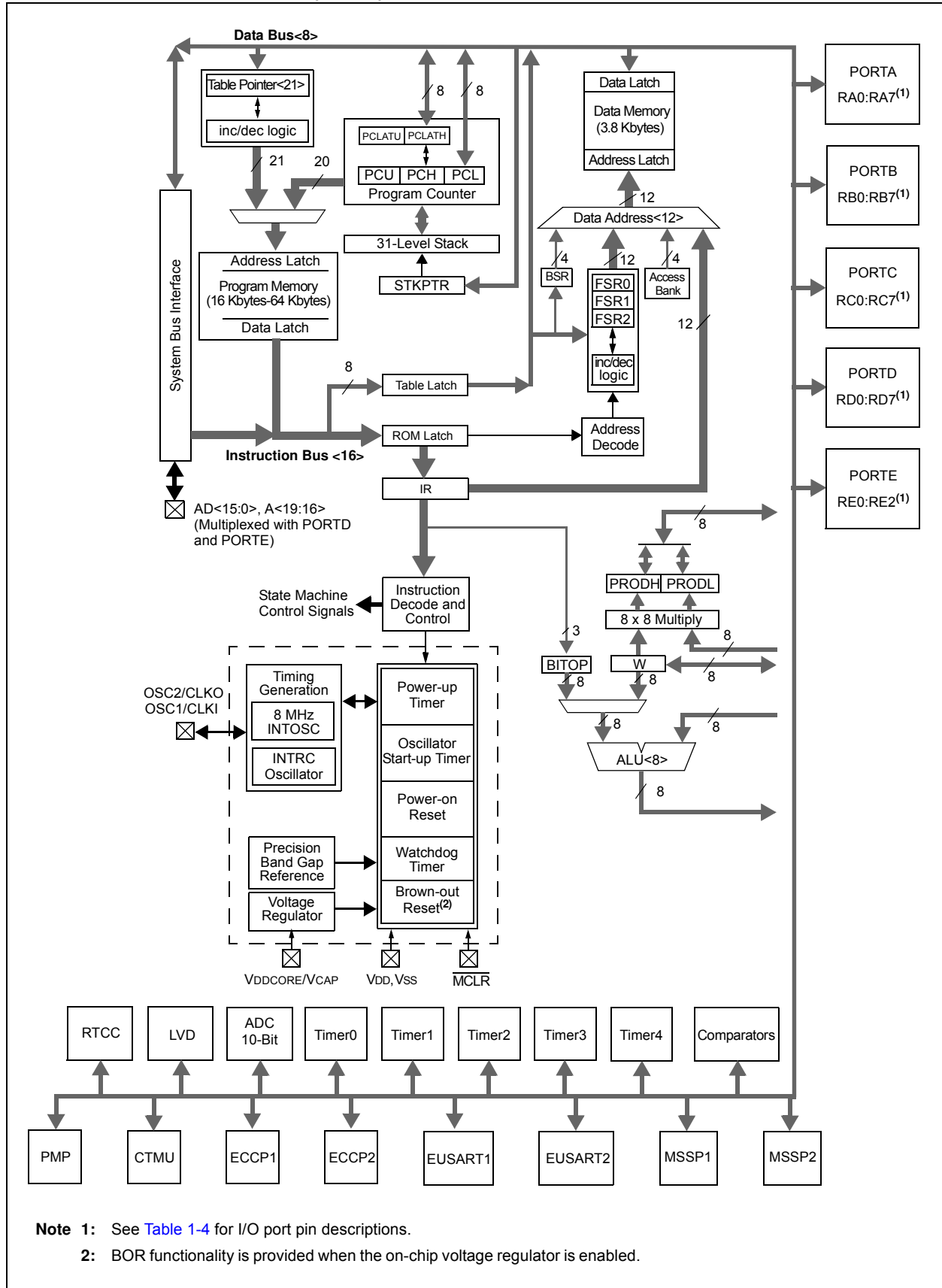
FIGURE 1-1: PIC18F2XJ11 (28-PIN) BLOCK DIAGRAM



- Note 1:** See Table 1-3 for I/O port pin descriptions.
Note 2: BOR functionality is provided when the on-chip voltage regulator is enabled.

PIC18F46J11 FAMILY

FIGURE 1-2: PIC18F4XJ11 (44-PIN) BLOCK DIAGRAM



PIC18F46J11 FAMILY

TABLE 1-3: PIC18F2XJ11 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
MCLR	1	26	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OSC1/CLKI/RA7 OSC1	9	6	I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. Main oscillator input connection.
CLKI			I	CMOS	External clock source input; always associated with pin function OSC1 (see related OSC1/CLKI pins).
RA7 ⁽¹⁾			I/O	TTL	Digital I/O.
OSC2/CLKO/RA6 OSC2	10	7	O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O	—	Main oscillator feedback output connection. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6 ⁽¹⁾			I/O	TTL	Digital I/O.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 DIG = Digital output
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-3: PIC18F2XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
RA0/AN0/C1INA/ULPWU/RP0 RA0 AN0 C1INA ULPWU RP0	2	27	I/O I I I I/O	DIG Analog Analog Analog DIG	PORTA is a bidirectional I/O port. Digital I/O. Analog input 0. Comparator 1 input A. Ultra low-power wake-up input. Remappable peripheral pin 0.
RA1/AN1/C2INA/RP1 RA1 AN1 C2INA RP1	3	28	I/O O I I/O	DIG Analog Analog DIG	Digital I/O. Analog input 1. Comparator 2 input A. Remappable peripheral pin 1.
RA2/AN2/VREF-/CVREF/C2INB RA2 AN2 VREF- CVREF C2INB	4	1	I/O I O I I	DIG Analog Analog Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input. Comparator reference voltage output. Comparator 2 input B.
RA3/AN3/VREF+/C1INB RA3 AN3 VREF+ C1INB	5	2	I/O I I I	DIG Analog Analog Analog	Digital I/O Analog input 3 A/D reference voltage (high) input Comparator 1 input B
RA5/AN4/ $\overline{SS1}$ /HLVDIN/ RP2 RA5 AN4 $\overline{SS1}$ HLVDIN RP2	7	4	I/O I I I I/O	DIG Analog TTL Analog DIG	Digital I/O. Analog input 4. SPI slave select input. High/low-voltage detect input. Remappable peripheral pin 2.
RA6 ⁽¹⁾ RA7 ⁽¹⁾					See the OSC2/CLKO/RA6 pin. See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 DIG = Digital output
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-3: PIC18F2XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
RB0/AN12/INT0/RP3 RB0 AN12 INT0 RP3	21	18	I/O I I I/O	DIG Analog ST DIG	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O. Analog input 12. External interrupt 0. Remappable peripheral pin 3.
RB1/AN10/RTCC/RP4 RB1 AN10 RTCC RP4	22	19	I/O I O I/O	DIG Analog DIG DIG	Digital I/O. Analog input 10. Real Time Clock Calendar output. Remappable peripheral pin 4.
RB2/AN8/CTED1/ REFO/RP5 RB2 AN8 CTED1 REFO RP5	23	20	I/O I I O I/O	DIG Analog ST DIG DIG	Digital I/O. Analog input 8. CTMU edge 1 input. Reference output clock. Remappable peripheral pin 5.
RB3/AN9/CTED2/RP6 RB3 AN9 CTED2 RP6	24	21	I/O I I/O I	DIG Analog ST DIG	Digital I/O. Analog input 9. CTMU edge 2 input. Remappable peripheral pin 6.
RB4/KBI0/RP7 RB4 KBI0 RP7	25	22	I/O I I/O	DIG TTL DIG	Digital I/O. Interrupt-on-change pin. Remappable peripheral pin 7.
RB5/KBI1/RP8 RB5 KBI1 RP8	26	23	I/O I I/O	DIG TTL DIG	Digital I/O. Interrupt-on-change pin. Remappable peripheral pin 8.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 DIG = Digital output
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-3: PIC18F2XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
RB6/KBI2/PGC/RP9	27	24	I/O	DIG	PORTB (continued) Digital I/O. Interrupt-on-change pin. ICSP™ clock input. Remappable peripheral pin 9.
RB6			I	TTL	
KBI2			I	ST	
PGC			I/O	DIG	
RP9					
RB7/KBI3/PGD/RP10	28	25	I/O	DIG	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin. Remappable peripheral pin 10.
RB7			I	TTL	
KBI3			I/O	ST	
PGD			I/O	DIG	
RP10					

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

I = Input

P = Power

DIG = Digital output

CMOS = CMOS compatible input or output

Analog = Analog input

O = Output

OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-3: PIC18F2XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
RC0/T1OSO/T1CKI/RP11	11	8	I/O	ST	PORTC is a bidirectional I/O port Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input. Remappable peripheral pin 11.
RC0			O	Analog	
T1OSO			I	ST	
T1CKI			I/O	DIG	
RP11					
RC1/T1OSI/RP12	12	9	I/O	ST	Digital I/O. Timer1 oscillator input. Remappable peripheral pin 12.
RC1			I	Analog	
RP12			I/O	DIG	
RC2/AN11/CTPLS/RP13	13	10	I/O	ST	Digital I/O. Analog input 11. CTMU pulse generator output. Remappable peripheral pin 13.
RC2			I	Analog	
AN11			O	DIG	
CTPLS			I/O	DIG	
RP13					
RC3/SCK1/SCL1/RP14	14	11	I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C™ mode. Remappable peripheral pin 14.
RC3			I/O	DIG	
SCK1					
SCL1			I/O	I ² C	
RP14			I/O	DIG	
RC4/SDI1/SDA1/RP15	15	12	I/O	ST	Digital I/O. SPI data input. I ² C data I/O. Remappable peripheral pin 15.
RC4			I	ST	
SDI1			I/O	I ² C	
SDA1			I/O	DIG	
RP15					
RC5/SDO1/RP16	16	13	I/O	ST	Digital I/O. SPI data output. Remappable peripheral pin 16.
RC5			O	DIG	
SDO1			I/O	DIG	
RP16					
RC6/TX1/CK1/RP17	17	14	I/O	ST	Digital I/O. EUSART1 asynchronous transmit. EUSART1 synchronous clock (see related RX1/DT1). Remappable peripheral pin 17.
RC6			O	DIG	
TX1			I/O	ST	
CK1					
RP17			I/O	DIG	
RC7/RX1/DT1/RP18	18	15	I/O	ST	Digital I/O. Asynchronous serial receive data input. Synchronous serial data output/input. Remappable peripheral pin 18.
RC7			I	ST	
RX1			I/O	ST	
DT1			I/O	DIG	
RP18			I/O	DIG	

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
DIG = Digital output
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-3: PIC18F2XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
VSS1	8	5	P	—	Ground reference for logic and I/O pins.
VSS2	19	16	—	—	
VDD	20	17	P	—	Positive supply for peripheral digital logic and I/O pins.
VDDCORE/VCAP	6	3			Core logic power or external filter capacitor connection.
VDDCORE			P	—	Positive supply for microcontroller core logic (regulator disabled).
VCAP			P	—	External filter capacitor connection (regulator enabled).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 DIG = Digital output

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-4: PIC18F4XJ11 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	44-QFN	44-TQFP			
MCLR	18	18	I	ST	Master Clear (Reset) input; this is an active-low Reset to the device.
OSC1/CLKI/RA7 OSC1	32	30	I	ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS. Main oscillator input connection.
CLKI			I	CMOS	External clock source input; always associated with pin function OSC1 (see related OSC1/CLKI pins).
RA7 ⁽¹⁾			I/O	TTL	Digital I/O.
OSC2/CLKO/RA6 OSC2	33	31	O	—	Oscillator crystal or clock output Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O	—	Main oscillator feedback output connection in RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6 ⁽¹⁾			I/O	TTL	Digital I/O.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 DIG = Digital output
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-4: PIC18F4XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	44-QFN	44-TQFP			
RA0/AN0/C1INA/ULPWU/PMA6/RP0 RA0 AN0 C1INA ULPWU PMA6 RP0	19	19	I/O	DIG	PORTA is a bidirectional I/O port. Digital I/O. Analog input 0. Comparator 1 input A. Ultra low-power wake-up input. Parallel Master Port digital output. Remappable peripheral pin 0.
RA1/AN1/C2INA/PMA7/RP1 RA1 AN1 C2INA PMA7 RP1	20	20	I/O	DIG	Digital I/O. Analog input 1. Comparator 2 input A. Parallel Master Port digital output. Remappable peripheral pin 1.
RA2/AN2/VREF-/CVREF/C2INB RA2 AN2 VREF- CVREF C2INB	21	21	I/O	DIG	Digital I/O. Analog input 2. A/D reference voltage (low) input. Comparator reference voltage output. Comparator 2 input B.
RA3/AN3/VREF+/C1INB RA3 AN3 VREF+ C1INB	22	22	I/O	DIG	Digital I/O. Analog input 3. A/D reference voltage (high) input. Comparator 1 input B.
RA5/AN4/ $\overline{SS1}$ /HLVDIN/RP2 RA5 AN4 $\overline{SS1}$ HLVDIN RP2	24	24	I/O	DIG	Digital I/O. Analog input 4. SPI slave select input. High/low-voltage detect input. Remappable peripheral pin 2.
RA6 ⁽¹⁾ RA7 ⁽¹⁾					See the OSC2/CLKO/RA6 pin. See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 DIG = Digital output
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-4: PIC18F4XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	44-QFN	44-TQFP			
RB0/AN12/INT0/RP3 RB0 AN12 INT0 RP3	9	8	I/O	DIG	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O.
RB1/AN10/PMBE/RTCC/RP4 RB1 AN10 PMBE RTCC RP4	10	9	I/O	DIG	Analog input 12. External interrupt 0. Remappable peripheral pin 3. Digital I/O.
RB2/AN8/CTED1/PMA3/REFO/ RP5 RB2 AN8 CTED1 PMA3 REFO RP5	11	10	I/O	DIG	Analog input 10. Parallel Master Port byte enable. Real Time Clock Calendar output. Remappable peripheral pin 4. Digital I/O.
RB3/AN9/CTED2/PMA2/ RP6 RB3 AN9 CTED2 PMA2 RP6	12	11	I/O	DIG	Analog input 8. CTMU edge 1 input. Parallel Master Port address. Reference output clock. Remappable peripheral pin 5. Digital I/O.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 DIG = Digital output

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

PIC18F46J11 FAMILY

TABLE 1-4: PIC18F4XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description	
	44-QFN	44-TQFP				
PORTB (continued)						
RB4/PMA1/KBI0/RP7	14	14	I/O	DIG	Digital I/O.	
RB4			O	DIG	Parallel Master Port address.	
PMA1			I	TTL	Interrupt-on-change pin.	
KBI0			I/O	DIG	Remappable peripheral pin 7	
RP7						
RB5/PMA0/KBI1/RP8	15	15	I/O	DIG	Digital I/O.	
RB5			O	DIG	Parallel Master Port address.	
PMA0			I	TTL	Interrupt-on-change pin.	
KBI1			I/O	DIG	Remappable peripheral pin 8.	
RP8						
RB6/KBI2/PGC/RP9	16	16	I/O	DIG	Digital I/O.	
RB6			I	TTL	Interrupt-on-change pin.	
KBI2			I	ST	ICSP™ clock input.	
PGC			I/O	DIG	Remappable peripheral pin 9.	
RP9						
RB7/KBI3/PGD/RP10	17	17	I/O	DIG	Digital I/O.	
RB7			I	TTL	Interrupt-on-change pin.	
KBI3			I/O	ST	In-Circuit Debugger and ICSP programming data pin.	
PGD						
RP10					I/O	DIG

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 DIG = Digital output
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.