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# PIC18F66K80 FAMILY

## 28/40/44/64-Pin, Enhanced Flash Microcontrollers with ECAN™ and nanoWatt XLP Technology

### Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Two-Speed Oscillator Start-up
- Fail-Safe Clock Monitor (FSCM)
- Power-Saving Peripheral Module Disable (PMD)
- Ultra Low-Power Wake-up
- Fast Wake-up, 1 μs, Typical
- Low-Power WDT, 300 nA, Typical
- Run mode Currents Down to Very Low 3.8 μA, Typical
- Idle mode Currents Down to Very Low 880 nA, Typical
- Sleep mode Current Down to Very Low 13 nA, Typical

### ECAN Bus Module Features:

- Conforms to CAN 2.0B Active Specification
- Three Operating modes:
  - Legacy mode (full backward compatibility with existing PIC18CXX8/FXX8 CAN modules)
  - Enhanced mode
  - FIFO mode or programmable TX/RX buffers
- Message Bit Rates up to 1 Mbps
- DeviceNet™ Data Byte Filter Support
- Six Programmable Receive/Transmit Buffers
- Three Dedicated Transmit Buffers with Prioritization
- Two Dedicated Receive Buffers

### ECAN Bus Module Features (Continued):

- 16 Full, 29-Bit Acceptance Filters with Dynamic Association
- Three Full, 29-Bit Acceptance Masks
- Automatic Remote Frame Handling
- Advanced Error Management Features

### Special Microcontroller Features:

- Operating Voltage Range: 1.8V to 5.5V
- On-Chip 3.3V Regulator
- Operating Speed up to 64 MHz
- Up to 64 Kbytes On-Chip Flash Program Memory:
  - 10,000 erase/write cycle, typical
  - 20 years minimum retention, typical
- 1,024 Bytes of Data EEPROM:
  - 100,000 Erase/write cycle data EEPROM memory, typical
- 3.6 Kbytes of General Purpose Registers (SRAM)
- Three Internal Oscillators: LF-INTOSC (31 KHz), MF-INTOSC (500 kHz) and HF-INTOSC (16 MHz)
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 4,194s
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins
- Programmable BOR
- Programmable LVD

**TABLE 1: DEVICE COMPARISON**

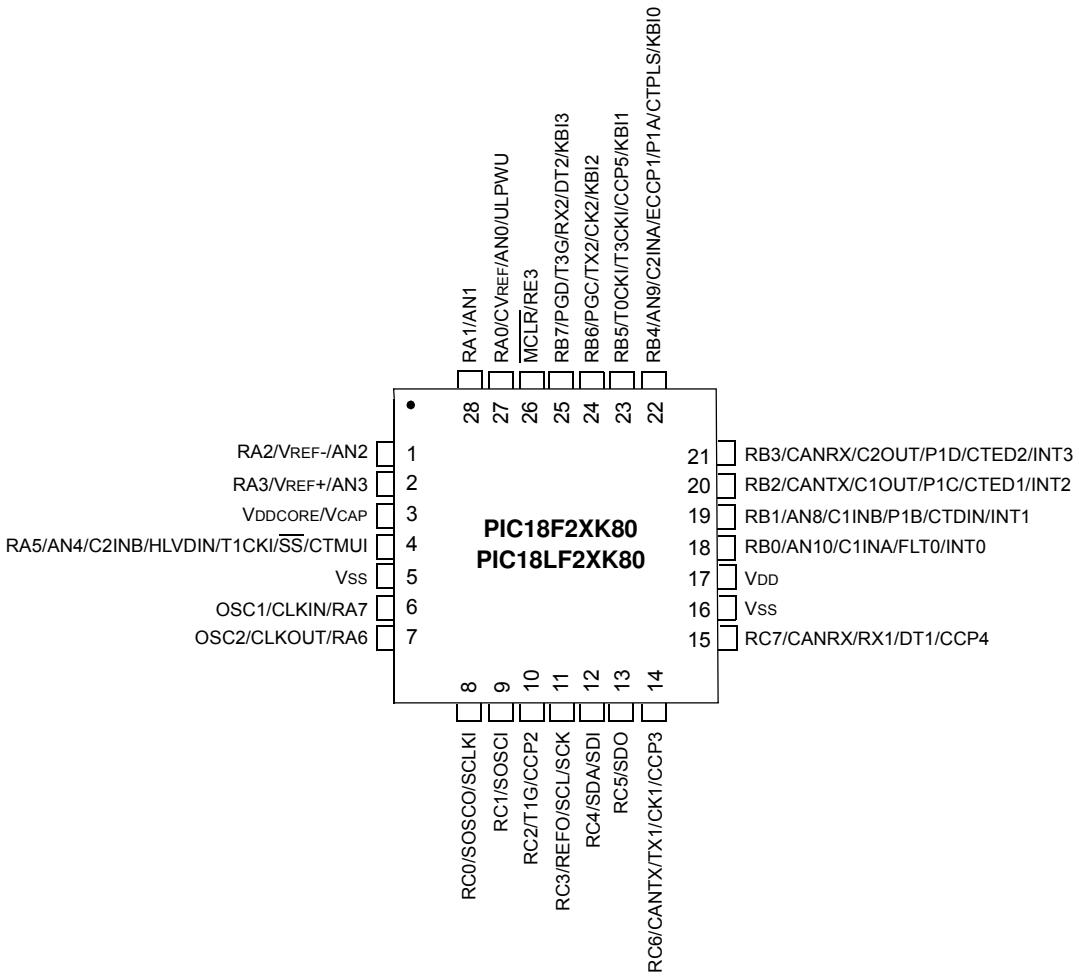
| Device | Program Memory | Data Memory (Bytes) | Data EE (Bytes) | Pins | I/O | CTMU | 12-Bit A/D Channels | CCP/ ECCP | Timers 8-Bit/16-Bit | EUSART | Comparators | ECAN™ | MSSP | BORMV/LVD | DSM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIC18F25K80 | 32 Kbytes | 3,648 | 1,024 | 28 | 24 | 1 | 8-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18LF25K80 | 32 Kbytes | 3,648 | 1,024 | 28 | 24 | 1 | 8-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18F26K80 | 64 Kbytes | 3,648 | 1,024 | 28 | 24 | 1 | 8-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18LF26K80 | 64 Kbytes | 3,648 | 1,024 | 28 | 24 | 1 | 8-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18F45K80 | 32 Kbytes | 3,648 | 1,024 | 40/44 | 35 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18LF45K80 | 32 Kbytes | 3,648 | 1,024 | 40/44 | 35 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18F46K80 | 64 Kbytes | 3,648 | 1,024 | 40/44 | 35 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18LF46K80 | 64 Kbytes | 3,648 | 1,024 | 40/44 | 35 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | No |
| PIC18F65K80 | 32 Kbytes | 3,648 | 1,024 | 64 | 54 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | Yes |
| PIC18LF65K80 | 32 Kbytes | 3,648 | 1,024 | 64 | 54 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | Yes |
| PIC18F66K80 | 64 Kbytes | 3,648 | 1,024 | 64 | 54 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | Yes |
| PIC18LF66K80 | 64 Kbytes | 3,648 | 1,024 | 64 | 54 | 1 | 11-ch | 4/1 | 2/3 | 2 | 2 | 1 | 1 | Yes | Yes |

## Peripheral Highlights:

- Five CCP/ECCP modules:
  - Four Capture/Compare/PWM (CCP) modules
  - One Enhanced Capture/Compare/PWM (ECCP) module
- Five 8/16-Bit Timer/Counter modules:
  - Timer0: 8/16-bit timer/counter with 8-bit programmable prescaler
  - Timer1, Timer3: 16-bit timer/counter
  - Timer2, Timer4: 8-bit timer/counter
- Two Analog Comparators
- Configurable Reference Clock Output
- Charge Time Measurement Unit (CTMU):
  - Capacitance measurement
  - Time measurement with 1 ns typical resolution
  - Integrated voltage reference
- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Up to Four External Interrupts
- One Master Synchronous Serial Port (MSSP) module:
  - 3/4-wire SPI (supports all four SPI modes)
  - $I^2C$™ Master and Slave modes
- Two Enhanced Addressable USART modules:
  - LIN/J2602 support
  - Auto-Baud Detect (ABD)
- 12-Bit A/D Converter with up to 11 Channels:
  - Auto-acquisition and Sleep operation
  - Differential Input mode of operation
- Data Signal Modulator module:
  - Select modulator and carrier sources from various module outputs
- Integrated Voltage Reference

## Pin Diagrams

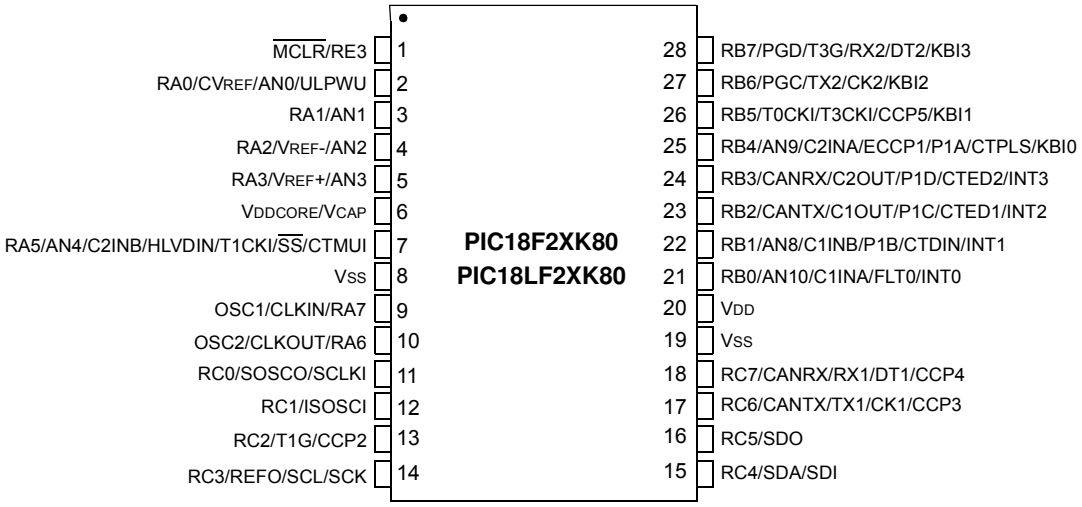
**28-Pin QFN(1)**



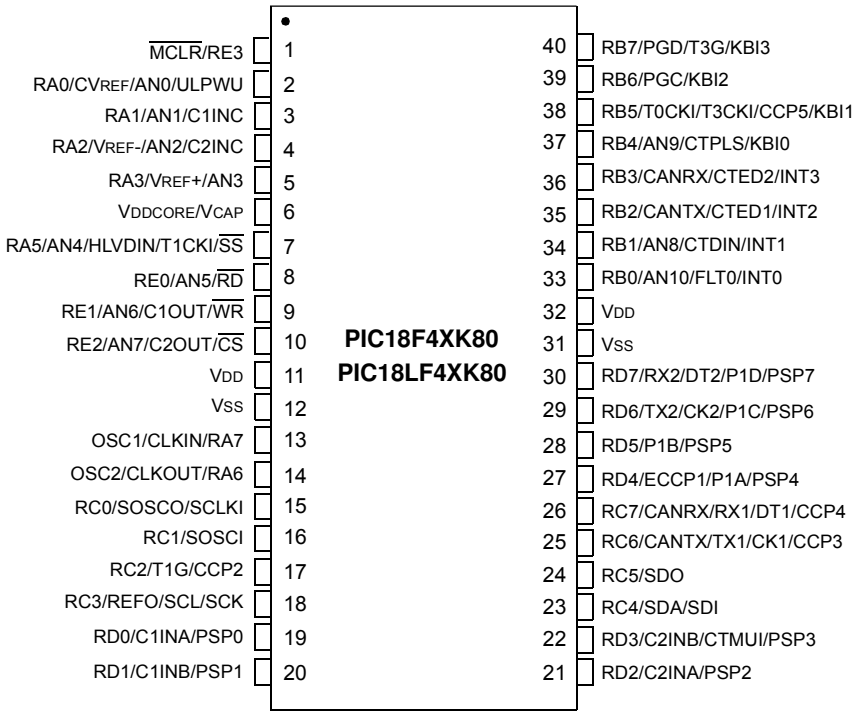

**Note 1:** For the QFN package, it is recommended that the bottom pad be connected to VSS.

## Pin Diagrams (Continued)

### 28-Pin SSOP/SPDIP/SOIC

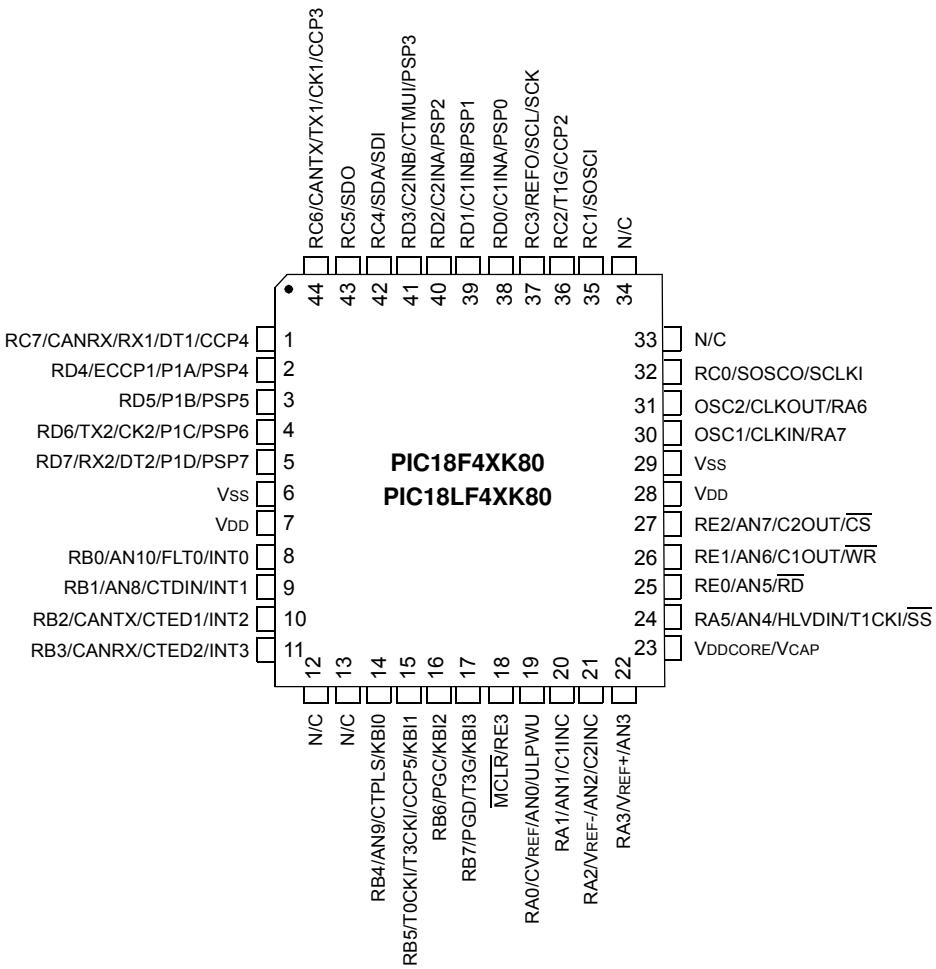



### 40-Pin PDIP



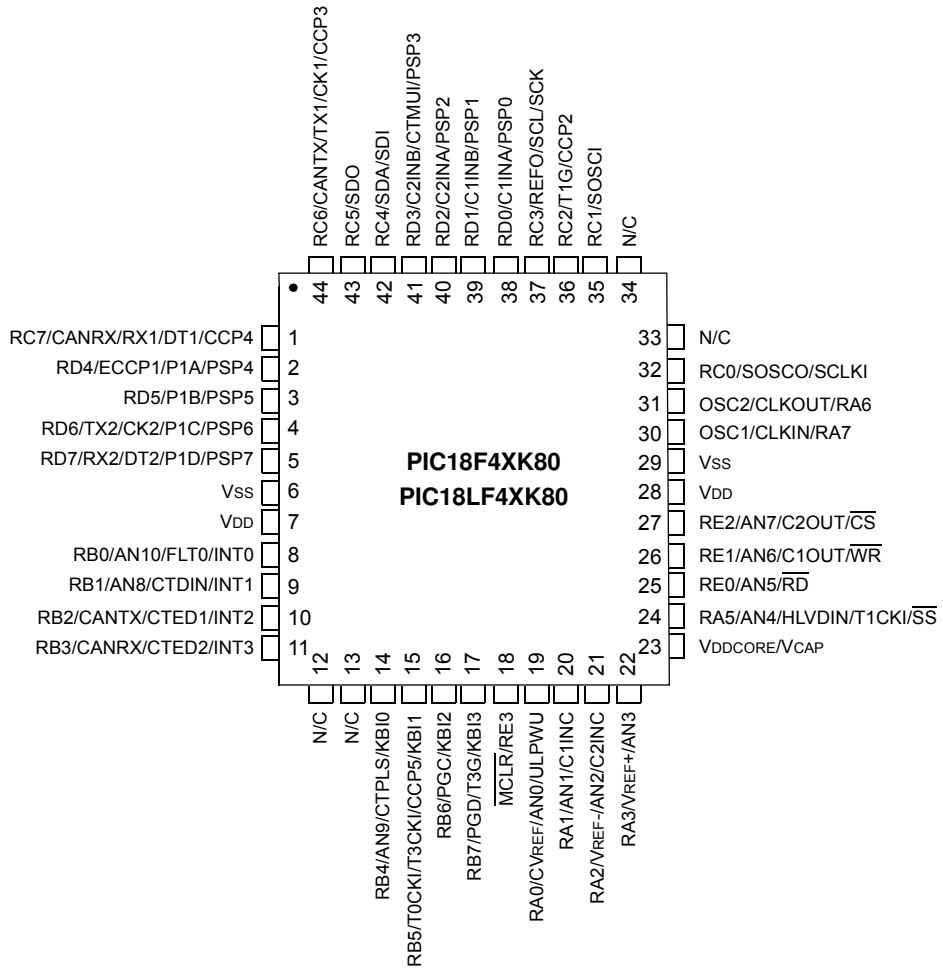
## Pin Diagrams (Continued)

**44-Pin TQFP**



## Pin Diagrams (Continued)

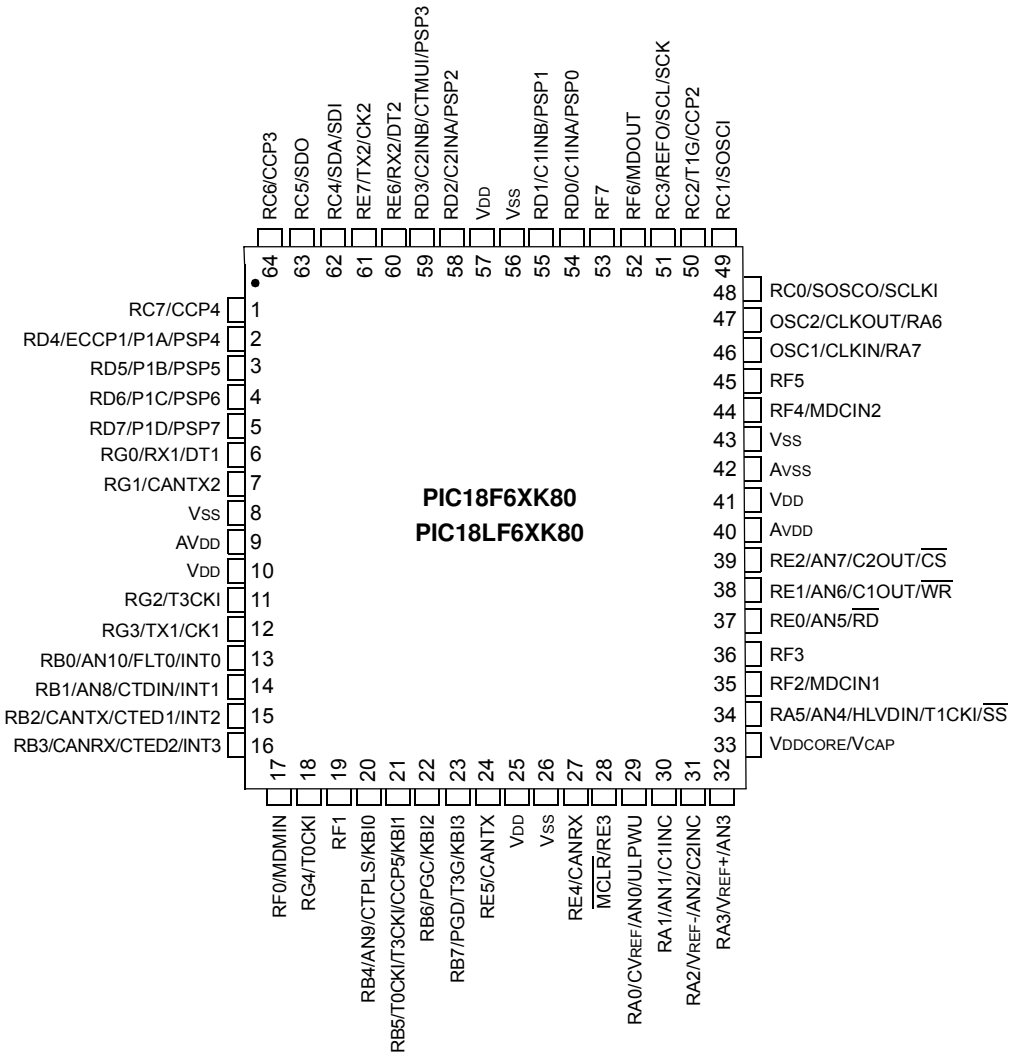
**44-Pin QFN(1)**




**Note 1:** For the QFN package, it is recommended that the bottom pad be connected to VSS.

## Pin Diagrams (Continued)

**64-Pin QFN(1)/TQFP**




**Note 1:** For the QFN package, it is recommended that the bottom pad be connected to VSS.

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**NOTES:**

# 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F25K80
- PIC18F26K80
- PIC18F45K80
- PIC18F46K80
- PIC18F65K80
- PIC18F66K80
- PIC18LF25K80
- PIC18LF26K80
- PIC18LF45K80
- PIC18LF46K80
- PIC18LF65K80
- PIC18LF66K80

This family combines the traditional advantages of all PIC18 microcontrollers – namely, high computational performance and a rich feature set – with an extremely competitive price point. These features make the PIC18F66K80 family a logical choice for many high-performance applications where price is a primary consideration.

## 1.1 Core Features

### 1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F66K80 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the Internal RC oscillator, power consumption during code execution can be reduced.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **nanoWatt XLP:** An extra low-power BOR and low-power Watchdog timer

### 1.1.2 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F66K80 family offer different oscillator options, allowing users a range of choices in developing application hardware. These include:

- External Resistor/Capacitor (RC); RA6 available
- External Resistor/Capacitor with Clock Out (RCIO)
- Three External Clock modes:
  - External Clock (EC); RA6 available
  - External Clock with Clock Out (ECIO)
  - External Crystal (XT, HS, LP)
- A Phase Lock Loop (PLL) frequency multiplier, available to the external oscillator modes which allows clock speeds of up to 64 MHz. PLL can also be used with the internal oscillator.
- An internal oscillator block that provides a 16 MHz clock (±2% accuracy) and an INTOSC source (approximately 31 kHz, stable over temperature and $V_{DD}$)
  - Operates as HF-INTOSC or MF-INTOSC when block is selected for 16 MHz or 500 kHz
  - Frees the two oscillator pins for use as additional general purpose I/O

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

### 1.1.3 MEMORY OPTIONS

The PIC18F66K80 family provides ample room for application code, from 32 Kbytes to 64 Kbytes of code space. The Flash cells for program memory are rated to last up to 10,000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 20 years.

The Flash program memory is readable and writable. During normal operation, the PIC18F66K80 family also provides plenty of room for dynamic application data with up to 3.6 Kbytes of data RAM.

### 1.1.4 EXTENDED INSTRUCTION SET

The PIC18F66K80 family implements the optional extension to the PIC18 instruction set, adding eight new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as 'C'.

### 1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between the 28-pin, 40-pin, 44-pin and 64-pin members, or even jumping from smaller to larger memory devices.

The PIC18F66K80 family is also largely pin compatible with other PIC18 families, such as the PIC18F4580, PIC18F4680 and PIC18F8680 families of microcontrollers with an ECAN module. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining a similar feature set.

## 1.2 Other Special Features

- **Communications:** The PIC18F66K80 family incorporates a range of serial communication peripherals, including two Enhanced USARTs that support LIN/J2602, one Master SSP module capable of both SPI and $I^2C$™ (Master and Slave) modes of operation and an Enhanced CAN module.
- **CCP Modules:** PIC18F66K80 family devices incorporate four Capture/Compare/PWM (CCP) modules. Up to four different time bases can be used to perform several different operations at once.
- **ECCP Modules:** The PIC18F66K80 family has one Enhanced CCP (ECCP) module to maximize flexibility in control applications:
  - Up to four different time bases for performing several different operations at once
  - Up to four PWM outputs
  - Other beneficial features, such as polarity selection, programmable dead time, auto-shutdown and restart, and Half-Bridge and Full-Bridge Output modes
- **12-Bit A/D Converter:** The PIC18F66K80 family has a differential A/D. It incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and thus, reducing code overhead.
- **Charge Time Measurement Unit (CTMU):** The CTMU is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation.

  Together with other on-chip analog modules, the CTMU can precisely measure time, measure capacitance or relative changes in capacitance, or generate output pulses that are independent of the system clock.
- **LP Watchdog Timer (WDT):** This enhanced version incorporates a 22-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 31.0 "Electrical Characteristics"** for time-out periods.

## 1.3 Details on Individual Family Members

Devices in the PIC18F66K80 family are available in 28-pin, 40/44-pin and 64-pin packages. Block diagrams for each package are shown in Figure 1-1, Figure 1-2 and Figure 1-3, respectively.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
  - PIC18FX5K80 (PIC18F25K80, PIC18F45K80 and PIC18F45K80) – 32 Kbytes
  - PIC18FX6K80 (PIC18F26K80, PIC18F46K80 and PIC18F66K80) – 64 Kbytes
- I/O Ports:
  - PIC18F2XK80 (28-pin devices) – Three bidirectional ports
  - PIC18F4XK80 (40/44-pin devices) – Five bidirectional ports
  - PIC18F6XK80 (64-pin devices) – Seven bidirectional ports

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

The pinouts for all devices are listed in Table 1-4, Table 1-5 and Table 1-6.

**TABLE 1-1: DEVICE FEATURES FOR THE PIC18F2XK80 (28-PIN DEVICES)**

| Features | PIC18F25K80 | PIC18F26K80 |
|---|---|---|
| Operating Frequency | DC – 64 MHz | |
| Program Memory (Bytes) | 32K | 64K |
| Program Memory (Instructions) | 16,384 | 32,768 |
| Data Memory (Bytes) | 3.6K | |
| Interrupt Sources | 31 | |
| I/O Ports | Ports A, B, C | |
| Parallel Communications | Parallel Slave Port (PSP) | |
| Timers | Five | |
| Comparators | Two | |
| CTMU | Yes | |
| Capture/Compare/PWM (CCP) Modules | Four | |
| Enhanced CCP (ECCP) Modules | One | |
| Serial Communications | One MSSP and Two Enhanced USARTs (EUSART) | |
| 12-Bit Analog-to-Digital Module | Eight Input Channels | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST) | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | |
| Packages | 28-Pin QFN-S, SOIC, SPDIP and SSOP | |

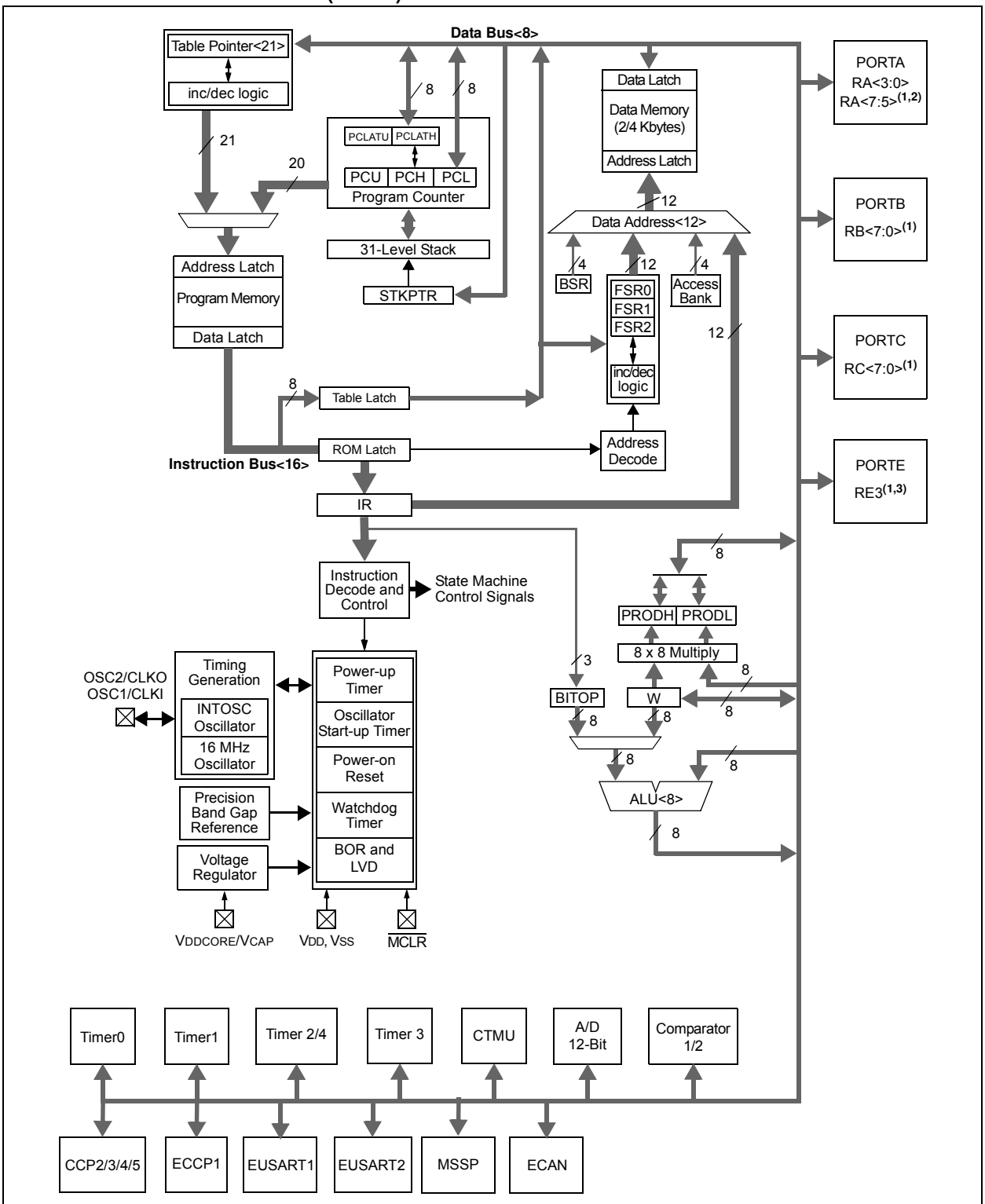
**TABLE 1-2: DEVICE FEATURES FOR THE PIC18F4XK80 (40/44-PIN DEVICES)**

| Features | PIC18F45K80 | PIC18F46K80 |
|---|---|---|
| Operating Frequency | DC – 64 MHz | |
| Program Memory (Bytes) | 32K | 64K |
| Program Memory (Instructions) | 16,384 | 32,768 |
| Data Memory (Bytes) | 3.6K | |
| Interrupt Sources | 32 | |
| I/O Ports | Ports A, B, C, D, E | |
| Parallel Communications | Parallel Slave Port (PSP) | |
| Timers | Five | |
| Comparators | Two | |
| CTMU | Yes | |
| Capture/Compare/PWM (CCP) Modules | Four | |
| Enhanced CCP (ECCP) Modules | One | |
| Serial Communications | One MSSP and Two Enhanced USARTs (EUSART) | |
| 12-Bit Analog-to-Digital Module | Eleven Input Channels | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST) | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | |
| Packages | 40-Pin PDIP and 44-Pin QFN and TQFP | |

**TABLE 1-3: DEVICE FEATURES FOR THE PIC18F6XK80 (64-PIN DEVICES)**

| Features | PIC18F65K80 | PIC18F66K80 |
|---|---|---|
| Operating Frequency | DC – 64 MHz | |
| Program Memory (Bytes) | 32K | 64K |
| Program Memory (Instructions) | 16,384 | 32,768 |
| Data Memory (Bytes) | 3.6K | |
| Interrupt Sources | 32 | |
| I/O Ports | Ports A, B, C, D, E, F, G | |
| Parallel Communications | Parallel Slave Port (PSP) | |
| Timers | Five | |
| Comparators | Two | |
| CTMU | Yes | |
| Capture/Compare/PWM (CCP) Modules | Four | |
| Enhanced CCP (ECCP) Modules | One | |
| DSM | Yes | Yes |
| Serial Communications | One MSSP and Two Enhanced USARTs (EUSART) | |
| 12-Bit Analog-to-Digital Module | Eleven Input Channels | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST) | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | |
| Packages | 64-Pin QFN and TQFP | |

**FIGURE 1-1: PIC18F2XK80 (28-PIN) BLOCK DIAGRAM**

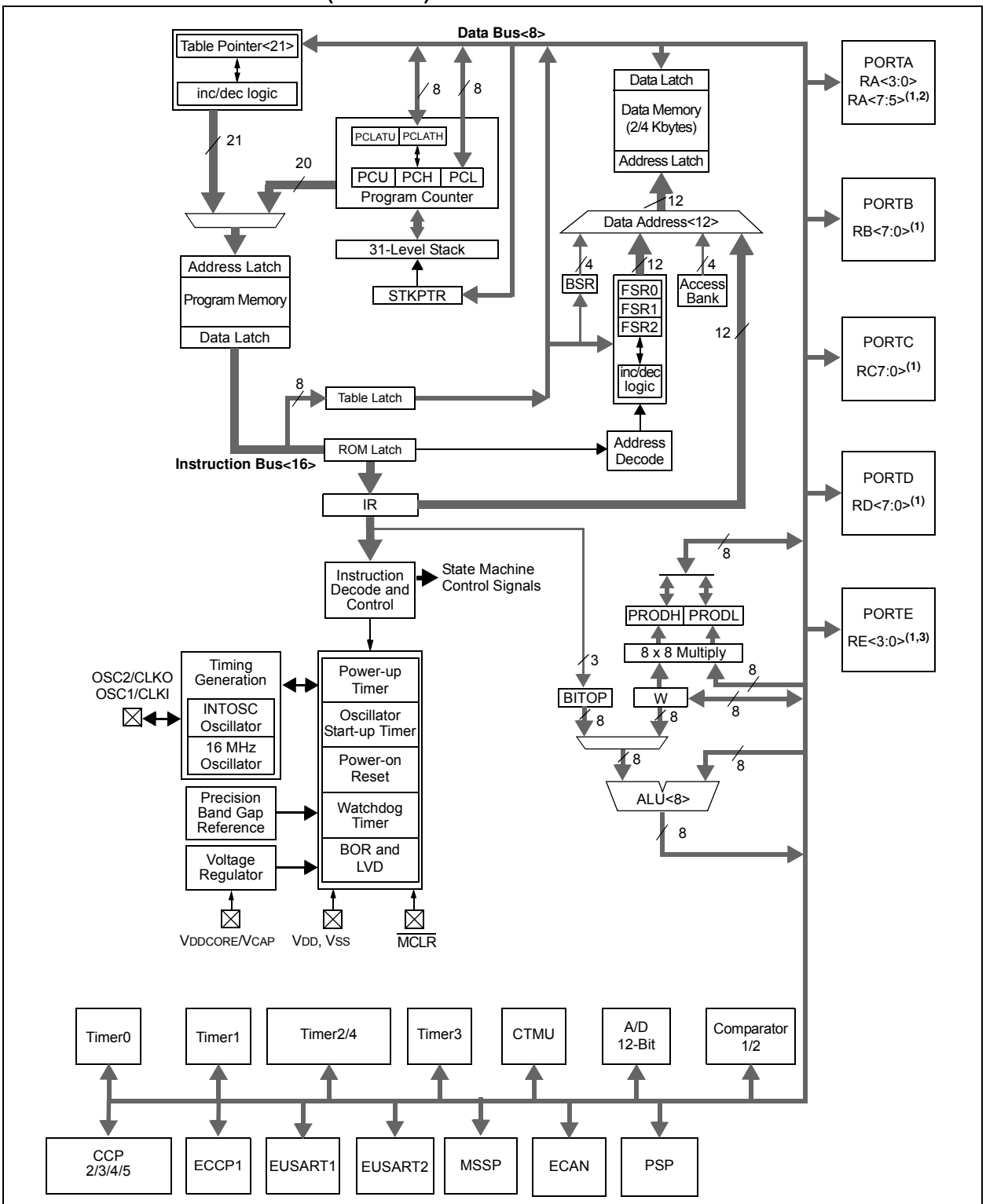



**Note 1:** See Table 1-4 for I/O port pin descriptions.

**2:** RA6 and RA7 are only available as digital I/O in select oscillator modes. For more information, see **Section 3.0 "Oscillator Configurations"**.

**3:** RE3 is only available when the MCLRE Configuration bit is cleared (MCLRE = 0).

**FIGURE 1-2: PIC18F4XK80 (40/44-PIN) BLOCK DIAGRAM**

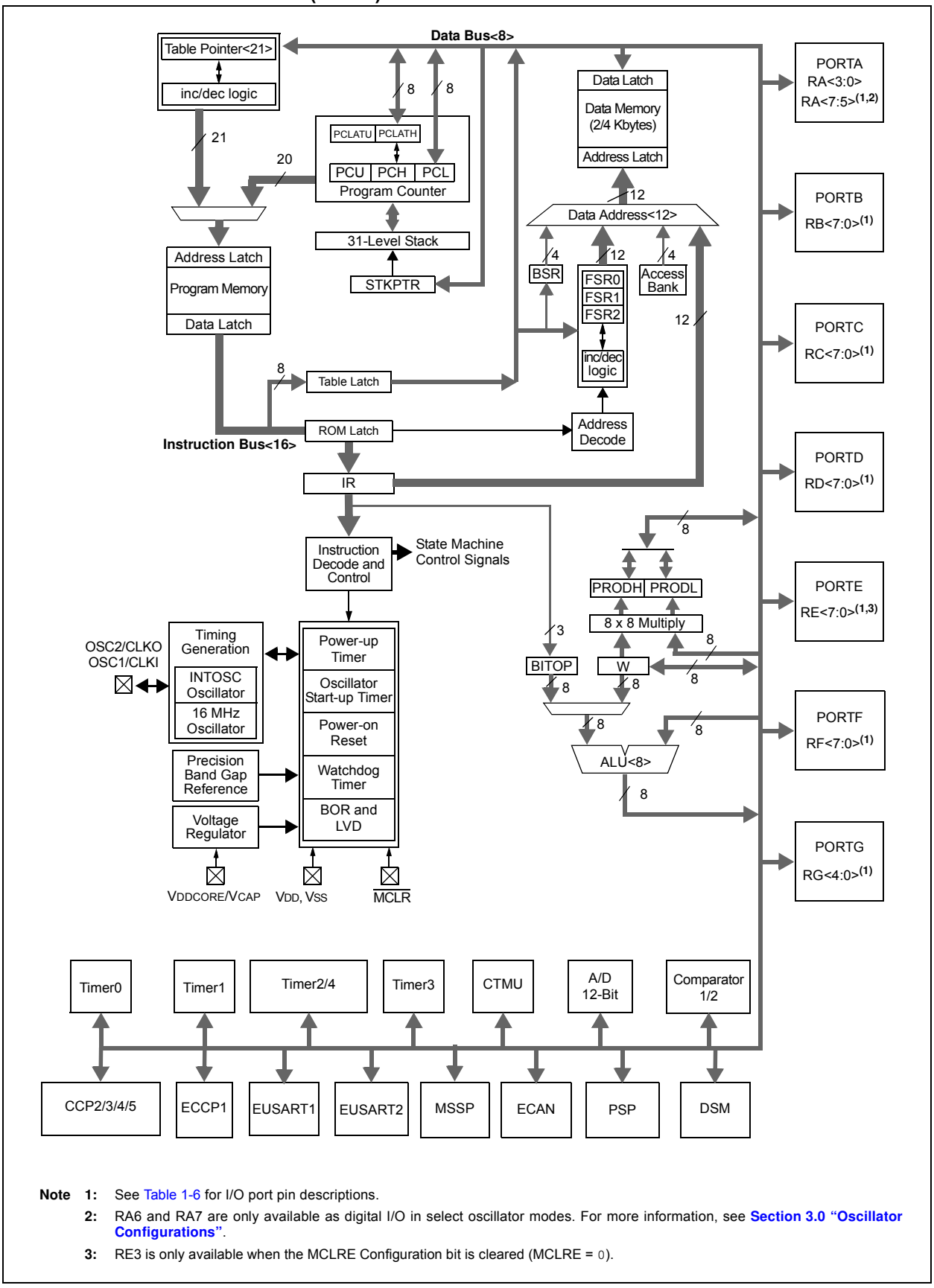



**Note 1:** See Table 1-5 for I/O port pin descriptions.

**2:** RA6 and RA7 are only available as digital I/O in select oscillator modes. For more information, see **Section 3.0 "Oscillator Configurations"**.

**3:** RE3 is only available when the MCLRE Configuration bit is cleared (MCLRE = 0).

**FIGURE 1-3: PIC18F6XK80 (64-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-6 for I/O port pin descriptions.

**2:** RA6 and RA7 are only available as digital I/O in select oscillator modes. For more information, see **Section 3.0 "Oscillator Configurations"**.

**3:** RE3 is only available when the MCLRE Configuration bit is cleared (MCLRE = 0).

**TABLE 1-4: PIC18F2XK80 I/O DESCRIPTIONS**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | QFN | SSOP/ SPDIP /SOIC | | | |
| $\overline{\text{MCLR}}$/RE3 | 26 | 1 | | | |
| MCLR | | | I | ST | Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device. |
| RE3 | | | I | ST | General purpose, input only pin. |
| OSC1/CLKIN/RA7 | 6 | 9 | | | |
| OSC1 | | | I | ST | Oscillator crystal input. |
| CLKIN | | | I | CMOS | External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | | I/O | ST/ CMOS | General purpose I/O pin. |
| OSC2/CLKOUT/RA6 | 7 | 10 | | | |
| OSC2 | | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKOUT | | | O | — | In certain oscillator modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | | I/O | ST/ CMOS | General purpose I/O pin. |

**Legend:** CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
$I^2C$™ = $I^2C$/SMBus input buffer
Analog = Analog input
O = Output

**TABLE 1-4: PIC18F2XK80 I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | QFN | SSOP/ SPDIP /SOIC | | | |
| | | | | | PORTA is a bidirectional I/O port. |
| RA0/CVREF/AN0/ULPWU | 27 | 2 | | | |
| RA0 | | | I/O | ST/ CMOS | General purpose I/O pin. |
| CVREF | | | O | Analog | Comparator reference voltage output. |
| AN0 | | | I | Analog | Analog Input 0. |
| ULPWU | | | I | Analog | Ultra Low-Power Wake-up input. |
| RA1/AN1 | 28 | 3 | | | |
| RA1 | | | I/O | ST/ CMOS | Digital I/O. |
| AN1 | | | I | Analog | Analog Input 1. |
| RA2/VREF-/AN2 | 1 | 4 | | | |
| RA2 | | | I/O | ST/ CMOS | Digital I/O. |
| VREF- | | | I | Analog | A/D reference voltage (low) input. |
| AN2 | | | I | Analog | Analog Input 2. |
| RA3/VREF+/AN3 | 2 | 5 | | | |
| RA3 | | | I/O | ST/ CMOS | Digital I/O. |
| VREF+ | | | I | Analog | A/D reference voltage (high) input. |
| AN3 | | | I | Analog | Analog Input 3. |
| RA5/AN4/C2INB/HLVDIN/ T1CKI/SS/CTMUI | 4 | 7 | | | |
| RA5 | | | I/O | ST/ CMOS | Digital I/O. |
| AN4 | | | I | Analog | Analog Input 4. |
| C2INB | | | I | Analog | Comparator 2 Input B. |
| HLVDIN | | | I | Analog | High/Low-Voltage Detect input. |
| T1CKI | | | I | ST | Timer1 clock input. |
| SS | | | I | ST | SPI slave select input. |
| CTMUI | | | | | CTMU pulse generator charger for the C2INB. |

**Legend:** CMOS = CMOS compatible input or output; $I^2C$™ = $I^2C$/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels; Analog = Analog input
I = Input; O = Output
P = Power

**TABLE 1-4: PIC18F2XK80 I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | QFN | SSOP/ SPDIP /SOIC | | | |
| | | | | | PORTB is a bidirectional I/O port. |
| RB0/AN10/C1INA/FLT0/ INT0 | 18 | 21 | | | |
| RB0 | | | I/O | ST/ CMOS | Digital I/O. |
| AN10 | | | I | Analog | Analog Input 10. |
| C1INA | | | I | Analog | Comparator 1 Input A. |
| FLT0 | | | I | ST | Enhanced PWM Fault input for ECCP1. |
| INT0 | | | I | ST | External Interrupt 0. |
| RB1/AN8/C1INB/P1B/ CTDIN/INT1 | 19 | 22 | | | |
| RB1 | | | I/O | ST/ CMOS | Digital I/O. |
| AN8 | | | I | Analog | Analog Input 8. |
| C1INB | | | I | Analog | Comparator 1 Input B. |
| P1B | | | O | CMOS | Enhanced PWM1 Output B. |
| CTDIN | | | I | ST | CTMU pulse delay input. |
| INT1 | | | I | ST | External Interrupt 1. |
| RB2/CANTX/C1OUT/ P1C/CTED1/INT2 | 20 | 23 | | | |
| RB2 | | | I/O | ST/ CMOS | Digital I/O. |
| CANTX | | | O | CMOS | CAN bus TX. |
| C1OUT | | | O | CMOS | Comparator 1 output. |
| P1C | | | O | CMOS | Enhanced PWM1 Output C. |
| CTED1 | | | I | ST | CTMU Edge 1 input. |
| INT2 | | | I | ST | External Interrupt 2. |
| RB3/CANRX/C2OUT/ P1D/CTED2/INT3 | 21 | 24 | | | |
| RB3 | | | I/O | ST/ CMOS | Digital I/O. |
| CANRX | | | I | ST | CAN bus RX. |
| C2OUT | | | O | CMOS | Comparator 2 output. |
| P1D | | | O | CMOS | Enhanced PWM1 Output D. |
| CTED2 | | | I | ST | CTMU Edge 2 input. |
| INT3 | | | I | ST | External Interrupt 3. |

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I = Input
P = Power
$I^2C$™ = $I^2C$/SMBus input buffer
Analog = Analog input
O = Output

**TABLE 1-4: PIC18F2XK80 I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | QFN | SSOP/ SPDIP /SOIC | | | |
| RB4/AN9/C2INA/ECCP1/ P1A/CTPLS/KBI0 | 22 | 25 | | | |
| RB4 | | | I/O | ST/ CMOS | Digital I/O. |
| AN9 | | | I | Analog | Analog Input 9. |
| C2INA | | | I | Analog | Comparator 2 Input A. |
| ECCP1 | | | I/O | ST | Capture 1 input/Compare 1 output/PWM1 output. |
| P1A | | | O | CMOS | Enhanced PWM1 Output A. |
| CTPLS | | | O | ST | CTMU pulse generator output. |
| KBI0 | | | I | ST | Interrupt-on-change pin. |
| RB5/T0CKI/T3CKI/CCP5/ KBI1 | 23 | 26 | | | |
| RB5 | | | I/O | ST/ CMOS | Digital I/O. |
| T0CKI | | | I | ST | Timer0 external clock input. |
| T3CKI | | | I | ST | Timer3 external clock input. |
| CCP5 | | | I/O | ST/ CMOS | Capture 5 input/Compare 5 output/PWM5 output. |
| KBI1 | | | I | ST | Interrupt-on-change pin. |
| RB6/PGC/TX2/CK2/KBI2 | 24 | 27 | | | |
| RB6 | | | I/O | ST/ CMOS | Digital I/O. |
| PGC | | | I | ST | In-Circuit Debugger and ICSP™ programming clock input pin. |
| TX2 | | | O | CMOS | EUSART asynchronous transmit. |
| CK2 | | | I/O | ST | EUSART synchronous clock. (See related RX2/DT2.) |
| KBI2 | | | I | ST | Interrupt-on-change pin. |
| RB7/PGD/T3G/RX2/DT2/ KBI3 | 25 | 28 | | | |
| RB7 | | | I/O | ST/ CMOS | Digital I/O. |
| PGD | | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |
| T3G | | | I | ST | Timer3 external clock gate input. |
| RX2 | | | I | ST | EUSART asynchronous receive. |
| DT2 | | | I/O | ST | EUSART synchronous data. (See related TX2/CK2.) |
| KBI3 | | | I | ST | Interrupt-on-change pin. |

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ST = Schmitt Trigger input with CMOS levels; Analog = Analog input
I = Input; O = Output
P = Power

**TABLE 1-4: PIC18F2XK80 I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | QFN | SSOP/ SPDIP /SOIC | | | |
| | | | | | PORTC is a bidirectional I/O port. |
| RC0/SOSCO/SCLKI | 8 | 11 | | | |
| RC0 | | | I/O | ST/ CMOS | Digital I/O. |
| SOSCO | | | I | ST | Timer1 oscillator output. |
| SCLKI | | | I | ST | Digital SOSC input. |
| RC1/SOSCI | 9 | 12 | | | |
| RC1 | | | I/O | ST/ CMOS | Digital I/O. |
| SOSCI | | | I | CMOS | SOSC oscillator input. |
| RC2/T1G/CCP2 | 10 | 13 | | | |
| RC2 | | | I/O | ST/ CMOS | Digital I/O. |
| T1G | | | I | ST | Timer1 external clock gate input. |
| CCP2 | | | I/O | ST | Capture 2 input/Compare 2 output/PWM2 output. |
| RC3/REFO/SCL/SCK | 11 | 14 | | | |
| RC3 | | | I/O | ST/ CMOS | Digital I/O. |
| REFO | | | O | — | Reference clock out. |
| SCL | | | I/O | $I^2C$ | Synchronous serial clock input/output for $I^2C$ mode. |
| SCK | | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| RC4/SDA/SDI | 12 | 15 | | | |
| RC4 | | | I/O | ST/ CMOS | Digital I/O. |
| SDA | | | I/O | $I^2C$ | $I^2C$ data input/output. |
| SDI | | | I | ST | SPI data in. |
| RC5/SDO | 13 | 16 | | | |
| RC5 | | | I/O | ST/ CMOS | Digital I/O. |
| SDO | | | O | CMOS | SPI data out. |
| RC6/CANTX/TX1/CK1/ CCP3 | 14 | 17 | | | |
| RC6 | | | I/O | ST/ CMOS | Digital I/O. |
| CANTX | | | O | CMOS | CAN bus TX. |
| TX1 | | | O | CMOS | EUSART asynchronous transmit. |
| CK1 | | | I/O | ST | EUSART synchronous clock. (See related RX1/DT1.) |
| CCP3 | | | I/O | ST/ CMOS | Capture 3 input/Compare 3 output/PWM3 output. |

**Legend:** CMOS = CMOS compatible input or output
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I = Input
P = Power
$I^2C$™ = $I^2C$/SMBus input buffer
Analog = Analog input
O = Output

**TABLE 1-4: PIC18F2XK80 I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | QFN | SSOP/ SPDIP /SOIC | | | |
| RC7/CANRX/RX1/DT1/ CCP4 | 15 | 18 | | | |
| RC7 | | | I/O | ST/ CMOS | Digital I/O. |
| CANRX | | | I | ST | CAN bus RX. |
| RX1 | | | I | ST | EUSART asynchronous receive. |
| DT1 | | | I/O | ST | EUSART synchronous data. (See related TX2/CK2.) |
| CCP4 | | | I/O | ST CMOS | Capture 4 input/Compare 4 output/PWM4 output. |
| VSS | 5 | 8 | P | | |
| VSS | | | | | Ground reference for logic and I/O pins. |
| VSS | 16 | 19 | | | |
| VSS | | | | | Ground reference for logic and I/O pins. |
| VDDCORE/VCAP | 3 | 6 | P | | |
| VDDCORE | | | | | External filter capacitor connection. |
| VCAP | | | | | External filter capacitor connection |
| VDD | 17 | 20 | P | | |
| VDD | | | | | Positive supply for logic and I/O pins. |

**Legend:** CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
$I^2C$™ = $I^2C$/SMBus input buffer
Analog = Analog input
O = Output

**TABLE 1-5: PIC18F4XK80 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | PDIP | QFN/ TQFP | | | |
| $\overline{MCLR}$/RE3 | 1 | 18 | | | |
| $\overline{MCLR}$ | | | I | ST | Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device. |
| RE3 | | | I | ST | General purpose, input only pin. |
| OSC1/CLKIN/RA7 | 13 | 30 | | | |
| OSC1 | | | I | ST | Oscillator crystal input. |
| CLKIN | | | I | CMOS | External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | | I/O | ST/ CMOS | General purpose I/O pin. |
| OSC2/CLKOUT/RA6 | 14 | 31 | | | |
| OSC2 | | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKOUT | | | O | — | In certain oscillator modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | | I/O | ST/ CMOS | General purpose I/O pin. |

**Legend:** $I^2C$™ = $I^2C$/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output

**TABLE 1-5: PIC18F4XK80 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | PDIP | QFN/ TQFP | | | |
| | | | | | PORTA is a bidirectional I/O port. |
| RA0/CVREF/AN0/ULPWU | 2 | 19 | | | |
| RA0 | | | I/O | ST/ CMOS | General purpose I/O pin. |
| CVREF | | | O | Analog | Comparator reference voltage output. |
| AN0 | | | I | Analog | Analog Input 0. |
| ULPWU | | | I | Analog | Ultra Low-Power Wake-up input. |
| RA1/AN1/C1INC | 3 | 20 | | | |
| RA1 | | | I/O | ST/ CMOS | Digital I/O. |
| AN1 | | | I | Analog | Analog Input 1. |
| C1INC | | | I | Analog | Comparator 1 Input C. |
| RA2/VREF-/AN2/C2INC | 4 | 21 | | | |
| RA2 | | | I/O | ST/ CMOS | Digital I/O. |
| VREF- | | | I | Analog | A/D reference voltage (low) input. |
| AN2 | | | I | Analog | Analog Input 2. |
| C2INC | | | I | Analog | Comparator 2 Input C. |
| RA3/VREF+/AN3 | 5 | 22 | | | |
| RA3 | | | I/O | ST/ CMOS | Digital I/O. |
| VREF+ | | | I | Analog | A/D reference voltage (high) input. |
| AN3 | | | I | Analog | Analog Input 3. |
| RA5/AN4/HLVDIN/T1CKI/ $\overline{SS}$ | 7 | 24 | | | |
| RA5 | | | I/O | ST/ CMOS | Digital I/O. |
| AN4 | | | I | Analog | Analog Input 4. |
| HLVDIN | | | I | Analog | High/Low-Voltage Detect input. |
| T1CKI | | | I | ST | Timer1 clock input. |
| $\overline{SS}$ | | | I | ST | SPI slave select input. |

**Legend:** $I^2C$™ = $I^2C$/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output