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# PIC18F87J10 Family Data Sheet

## 64/80-Pin, High-Performance 1-Mbit Flash Microcontrollers with nanoWatt Technology

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# PIC18F87J10 FAMILY

## 64/80-Pin, High-Performance, 1-Mbit Flash Microcontrollers with nanoWatt Technology

### Special Microcontroller Features:

- Operating Voltage Range: 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- On-Chip 2.5V Regulator
- Low-Power, High-Speed CMOS Flash Technology
- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Break points via Two Pins
- Power-Managed modes:
  - Run: CPU on, peripherals on
  - Idle: CPU off, peripherals on
  - Sleep: CPU off, peripherals off
- Flash Program Memory:
  - 1000 erase/write cycle endurance typical
  - 20 year retention minimum
  - Self-write capability during normal operation

### Flexible Oscillator Structure:

- Two Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (PLL)
- Two External Clock modes, up to 40 MHz
- Internal 31 kHz Oscillator
- Secondary Oscillator using Timer1 @ 32 kHz
- Two-Speed Oscillator Start-up
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops

### Peripheral Highlights:

- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Four Programmable External Interrupts
- Four Input Change Interrupts
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Two Master Synchronous Serial Port (MSSP) modules Supporting 3-Wire SPI (all 4 modes) and $I^2C$™ Master and Slave modes
- Two Enhanced Addressable USART modules:
  - Supports RS-485, RS-232 and LIN/2602
  - Auto-wake-up on Start bit
  - Auto-Baud Detect (ABD)
- 10-Bit, up to 15-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
  - Self-calibration feature
- Dual Analog Comparators with Input Multiplexing

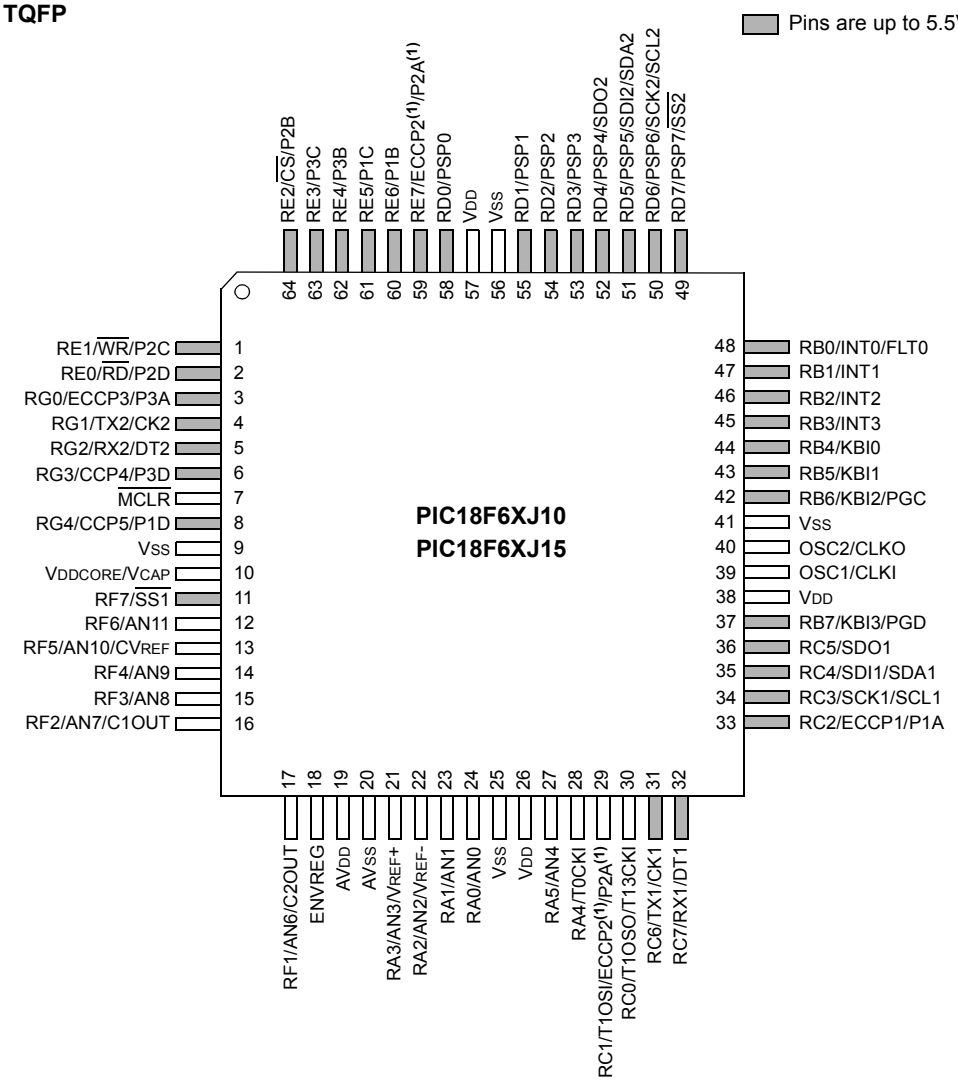
### External Memory Bus (PIC18F8XJ10/8XJ15 only):

- Address Capability of up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 12-Bit, 16-Bit and 20-Bit Addressing modes

| Device | Program Memory | | SRAM Data Memory (bytes) | I/O | 10-Bit A/D (ch) | CCP/ ECCP (PWM) | MSSP | | | EUSART | Comparators | Timers 8/16-Bit | External Bus |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Flash (bytes) | # Single-Word Instructions | | | | | | SPI | Master $I^2C$™ | | | | |
| PIC18F65J10 | 32K | 16384 | 2048 | 50 | 11 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F65J15 | 48K | 24576 | 2048 | 50 | 11 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F66J10 | 64K | 32768 | 2048 | 50 | 11 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F66J15 | 96K | 49152 | 3936 | 50 | 11 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F67J10 | 128K | 65536 | 3936 | 50 | 11 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F85J10 | 32K | 16384 | 2048 | 66 | 15 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |
| PIC18F85J15 | 48K | 24576 | 2048 | 66 | 15 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |
| PIC18F86J10 | 64K | 32768 | 2048 | 66 | 15 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |
| PIC18F86J15 | 96K | 49152 | 3936 | 66 | 15 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |
| PIC18F87J10 | 128K | 65536 | 3936 | 66 | 15 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |

## Pin Diagrams

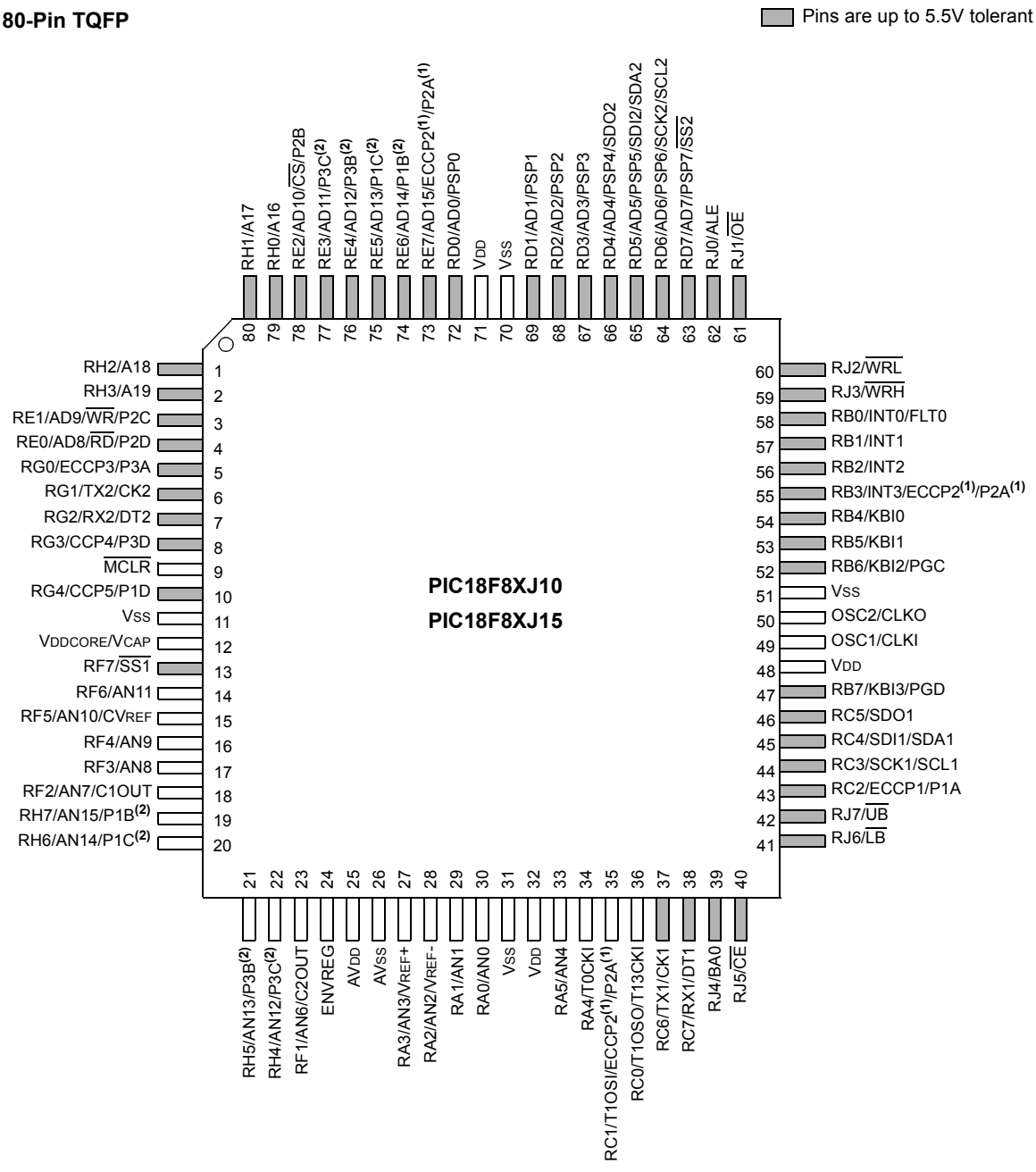
**64-Pin TQFP**




**Note 1:** The ECCP2/P2A pin placement depends on the setting of the CCP2MX Configuration bit.

## Pin Diagrams (Continued)

**80-Pin TQFP**




**Note 1:** The ECCP2/P2A pin placement depends on the setting of the CCP2MX Configuration bit and the program memory mode.

**2:** P1B, P1C, P3B and P3C pin placement depends on the setting of the ECCPMX Configuration bit.

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# 1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F65J10
- PIC18F65J15
- PIC18F66J10
- PIC18F66J15
- PIC18F67J10
- PIC18F85J10
- PIC18F85J15
- PIC18F86J10
- PIC18F86J15
- PIC18F87J10

This family introduces a new line of low-voltage devices with the main traditional advantage of all PIC18 microcontrollers – namely, high computational performance and a rich feature set – at an extremely competitive price point. These features make the PIC18F87J10 family a logical choice for many high-performance applications where cost is a primary consideration.

## 1.1 Core Features

### 1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F87J10 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal RC oscillator, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.

### 1.1.2 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F87J10 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of a divide-by-4 clock output.
- A Phase Lock Loop (PLL) frequency multiplier, available to the external oscillator modes which allows clock speeds of up to 40 MHz.
- An internal RC oscillator with a fixed 31-kHz output which provides an extremely low-power option for timing-insensitive applications.

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

### 1.1.3 EXPANDED MEMORY

The PIC18F87J10 family provides ample room for application code, from 32 Kbytes to 128 Kbytes of code space. The Flash cells for program memory are rated to last up to 100 erase/write cycles. The PIC18F87J10 family also provides plenty of room for dynamic application data, with up to 3936 bytes of data RAM.

### 1.1.4 EXTERNAL MEMORY BUS

In the unlikely event that 128 Kbytes of memory are inadequate for an application, the 80-pin members of the PIC18F87J10 family also implement an external memory bus. This allows the controller's internal program counter to address a memory space of up to 2 Mbytes, permitting a level of data access that few 8-bit devices can claim. This allows additional memory options, including:

- Using combinations of on-chip and external memory up to the 2-Mbyte limit
- Using external Flash memory for reprogrammable application code or large data tables
- Using external RAM devices for storing large amounts of variable data

### 1.1.5 EXTENDED INSTRUCTION SET

The PIC18F87J10 family implements the optional extension to the PIC18 instruction set, adding 8 new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as 'C'.

### 1.1.6 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 80-pin members, or even jumping from 64-pin to 80-pin devices.

The PIC18F87J10 family is also pin compatible with other PIC18 families, such as the PIC18F8720 and PIC18F8722. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining the same feature set.

## 1.2 Other Special Features

- **Communications:** The PIC18F87J10 family incorporates a range of serial communication peripherals, including 2 independent Enhanced USARTs and 2 Master SSP modules, capable of both SPI and $I^2C$™ (Master and Slave) modes of operation. In addition, one of the general purpose I/O ports can be reconfigured as an 8-bit Parallel Slave Port for direct processor-to-processor communications.
- **CCP Modules:** All devices in the family incorporate two Capture/Compare/PWM (CCP) modules and three Enhanced CCP modules to maximize flexibility in control applications. Up to four different time bases may be used to perform several different operations at once. Each of the three ECCPs offers up to four PWM outputs, allowing for a total of 12 PWMs. The ECCPs also offer many beneficial features, including polarity selection, programmable dead time, auto-shutdown and restart and Half-Bridge and Full-Bridge Output modes.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reducing code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 27.0 "Electrical Characteristics"** for time-out periods.

## 1.3 Details on Individual Family Members

Devices in the PIC18F87J10 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in four ways:

1. Flash program memory (six sizes, ranging from 32 Kbytes for PIC18FX5J10 devices to 128 Kbytes for PIC18FX7J10).
2. Data RAM (2048 bytes for PIC18FX5J10/X5J15/X6J10 devices, 3936 bytes for PIC18FX6J15/X7J10 devices).
3. A/D channels (11 for 64-pin devices, 15 for 80-pin devices).
4. I/O ports (7 bidirectional ports on 64-pin devices, 9 bidirectional ports on 80-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

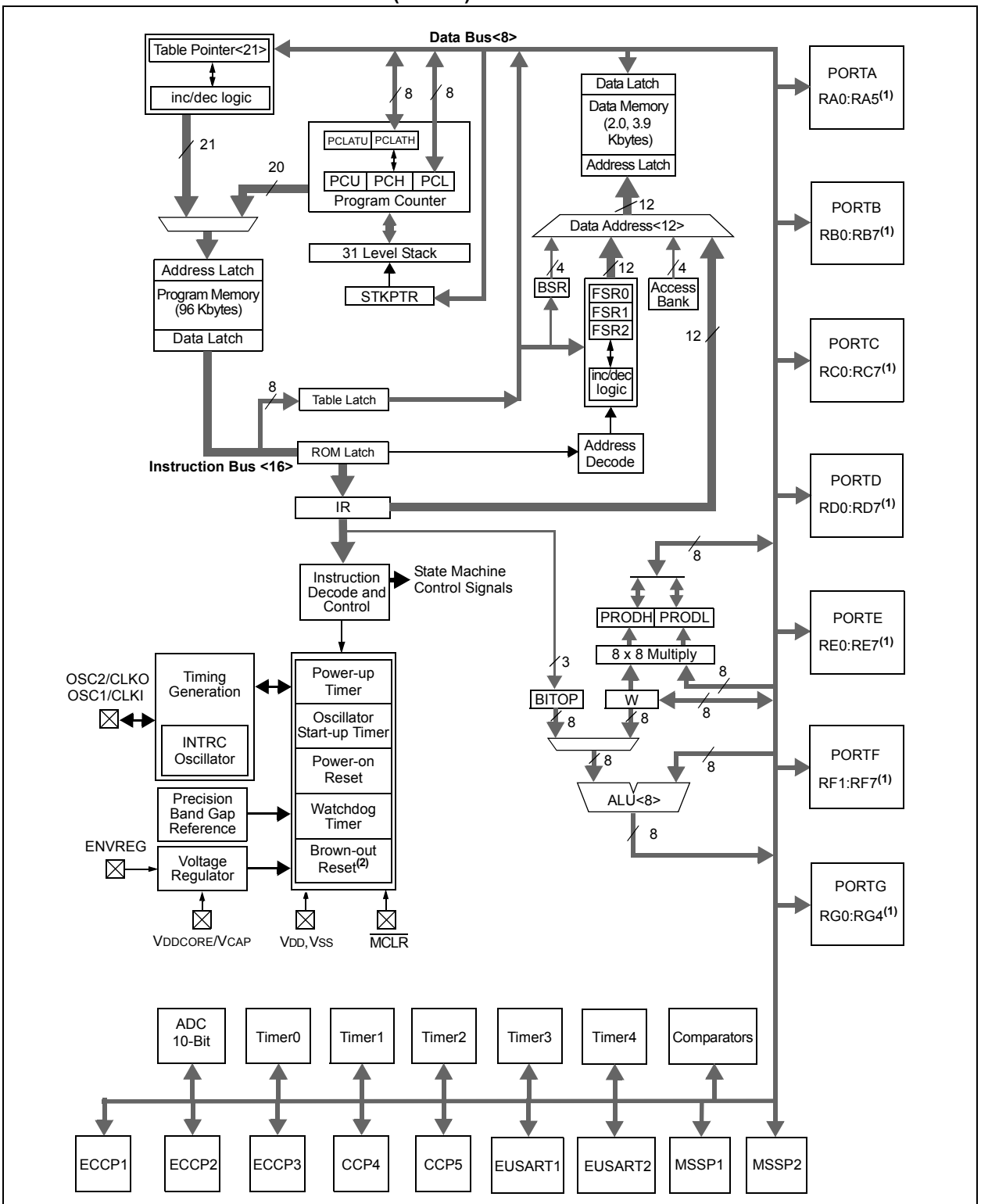
**TABLE 1-1: DEVICE FEATURES FOR THE PIC18F87J10 FAMILY (64-PIN DEVICES)**

| Features | PIC18F65J10 | PIC18F65J15 | PIC18F66J10 | PIC18F66J15 | PIC18F67J10 |
|---|---|---|---|---|---|
| Operating Frequency | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz |
| Program Memory (Bytes) | 32K | 48K | 64K | 96K | 128K |
| Program Memory (Instructions) | 16384 | 24576 | 32768 | 49152 | 65536 |
| Data Memory (Bytes) | 2048 | 2048 | 2048 | 3936 | 3936 |
| Interrupt Sources | 27 | | | | |
| I/O Ports | Ports A, B, C, D, E, F, G | | | | |
| Timers | 5 | | | | |
| Capture/Compare/PWM Modules | 2 | | | | |
| Enhanced Capture/ Compare/PWM Modules | 3 | | | | |
| Serial Communications | MSSP (2), Enhanced USART (2) | | | | |
| Parallel Communications (PSP) | Yes | | | | |
| 10-Bit Analog-to-Digital Module | 11 Input Channels | | | | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST) | | | | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set enabled | | | | |
| Packages | 64-pin TQFP | | | | |

**TABLE 1-2: DEVICE FEATURES FOR THE PIC18F87J10 FAMILY (80-PIN DEVICES)**

| Features | PIC18F85J10 | PIC18F85J15 | PIC18F86J10 | PIC18F86J15 | PIC18F87J10 |
|---|---|---|---|---|---|
| Operating Frequency | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz |
| Program Memory (Bytes) | 32K | 48K | 64K | 96K | 128K |
| Program Memory (Instructions) | 16384 | 24576 | 32768 | 49152 | 65536 |
| Data Memory (Bytes) | 2048 | 2048 | 2048 | 3936 | 3936 |
| Interrupt Sources | 27 | | | | |
| I/O Ports | Ports A, B, C, D, E, F, G, H, J | | | | |
| Timers | 5 | | | | |
| Capture/Compare/PWM Modules | 2 | | | | |
| Enhanced Capture/ Compare/PWM Modules | 3 | | | | |
| Serial Communications | MSSP (2), Enhanced USART (2) | | | | |
| Parallel Communications (PSP) | Yes | | | | |
| 10-Bit Analog-to-Digital Module | 15 Input Channels | | | | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST) | | | | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set enabled | | | | |
| Packages | 80-pin TQFP | | | | |

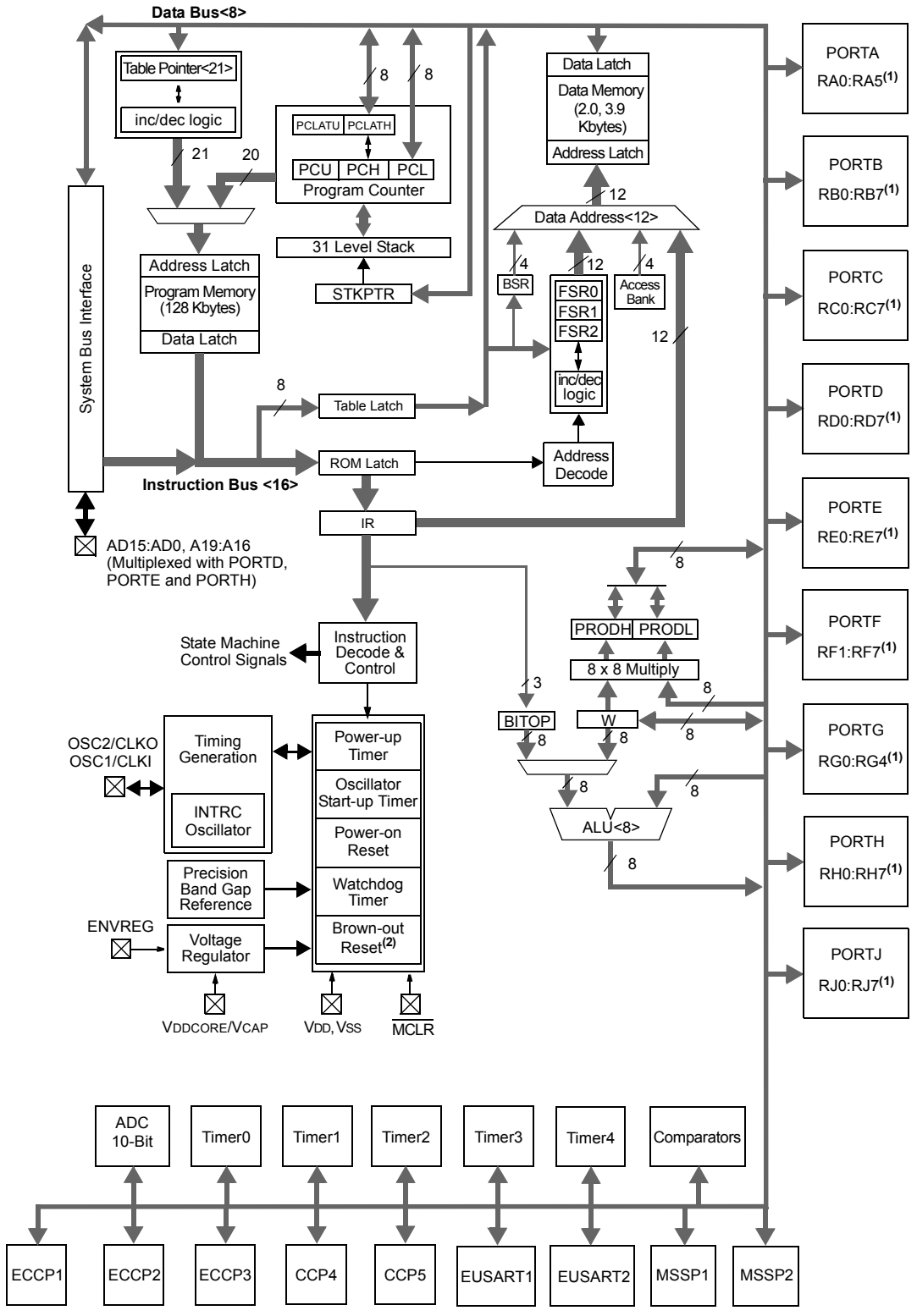
**FIGURE 1-1: PIC18F6XJ10/6XJ15 (64-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-3 for I/O port pin descriptions.

**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

**FIGURE 1-2: PIC18F8XJ10/8XJ15 (80-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-4 for I/O port pin descriptions.

**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

**TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| $\overline{MCLR}$ | 7 | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| OSC1/CLKI | 39 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| OSC2/CLKO | 40 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 24 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 23 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/$V_{REF-}$ | 22 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| $V_{REF-}$ | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/$V_{REF+}$ | 21 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| $V_{REF+}$ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 28 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4 | 27 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0 | 48 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| INT0 | | I | ST | External interrupt 0. |
| FLT0 | | I | ST | ECCP1/2/3 Fault input. |
| RB1/INT1 | 47 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| INT1 | | I | ST | External interrupt 1. |
| RB2/INT2 | 46 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| INT2 | | I | ST | External interrupt 2. |
| RB3/INT3 | 45 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| INT3 | | I | ST | External interrupt 3. |
| RB4/KBI0 | 44 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| RB5/KBI1 | 43 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| RB6/KBI2/PGC | 42 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP™ programming clock pin. |
| RB7/KBI3/PGD | 37 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP™ programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 30 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/ECCP2/P2A | 29 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| ECCP2(1) | | I/O | ST | Capture 2 input/Compare 2 output/PWM 2 output. |
| P2A(1) | | O | — | ECCP2 PWM output A. |
| RC2/ECCP1/P1A | 33 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| ECCP1 | | I/O | ST | Capture 1 input/Compare 1 output/PWM 1 output. |
| P1A | | O | — | ECCP1 PWM output A. |
| RC3/SCK1/SCL1 | 34 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK1 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL1 | | I/O | $I^2C$/SMB | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI1/SDA1 | 35 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI1 | | I | ST | SPI data in. |
| SDA1 | | I/O | $I^2C$/SMB | $I^2C$ data I/O. |
| RC5/SDO1 | 36 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO1 | | O | — | SPI data out. |
| RC6/TX1/CK1 | 31 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART1 asynchronous transmit. |
| CK1 | | I/O | ST | EUSART1 synchronous clock (see related RX1/DT1). |
| RC7/RX1/DT1 | 32 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART1 asynchronous receive. |
| DT1 | | I/O | ST | EUSART1 synchronous data (see related TX1/CK1). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTD is a bidirectional I/O port. |
| RD0/PSP0 | 58 | | | |
| RD0 | | I/O | ST | Digital I/O. |
| PSP0 | | I/O | TTL | Parallel Slave Port data. |
| RD1/PSP1 | 55 | | | |
| RD1 | | I/O | ST | Digital I/O. |
| PSP1 | | I/O | TTL | Parallel Slave Port data. |
| RD2/PSP2 | 54 | | | |
| RD2 | | I/O | ST | Digital I/O. |
| PSP2 | | I/O | TTL | Parallel Slave Port data. |
| RD3/PSP3 | 53 | | | |
| RD3 | | I/O | ST | Digital I/O. |
| PSP3 | | I/O | TTL | Parallel Slave Port data. |
| RD4/PSP4/SDO2 | 52 | | | |
| RD4 | | I/O | ST | Digital I/O. |
| PSP4 | | I/O | TTL | Parallel Slave Port data. |
| SDO2 | | O | — | SPI data out. |
| RD5/PSP5/SDI2/SDA2 | 51 | | | |
| RD5 | | I/O | ST | Digital I/O. |
| PSP5 | | I/O | TTL | Parallel Slave Port data. |
| SDI2 | | I | ST | SPI data in. |
| SDA2 | | I/O | $I^2C$/SMB | $I^2C$™ data I/O. |
| RD6/PSP6/SCK2/SCL2 | 50 | | | |
| RD6 | | I/O | ST | Digital I/O. |
| PSP6 | | I/O | TTL | Parallel Slave Port data. |
| SCK2 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL2 | | I/O | $I^2C$/SMB | Synchronous serial clock input/output for $I^2C$ mode. |
| RD7/PSP7/$\overline{SS2}$ | 49 | | | |
| RD7 | | I/O | ST | Digital I/O. |
| PSP7 | | I/O | TTL | Parallel Slave Port data. |
| $\overline{SS2}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTE is a bidirectional I/O port. |
| RE0/$\overline{RD}$/P2D | 2 | | | |
| RE0 | | I/O | ST | Digital I/O. |
| $\overline{RD}$ | | I | TTL | Read control for Parallel Slave Port. |
| P2D | | O | — | ECCP2 PWM output D. |
| RE1/$\overline{WR}$/P2C | 1 | | | |
| RE1 | | I/O | ST | Digital I/O. |
| $\overline{WR}$ | | I | TTL | Write control for Parallel Slave Port. |
| P2C | | O | — | ECCP2 PWM output C. |
| RE2/$\overline{CS}$/P2B | 64 | | | |
| RE2 | | I/O | ST | Digital I/O. |
| $\overline{CS}$ | | I | TTL | Chip select control for Parallel Slave Port. |
| P2B | | O | — | ECCP2 PWM output B. |
| RE3/P3C | 63 | | | |
| RE3 | | I/O | ST | Digital I/O. |
| P3C | | O | — | ECCP3 PWM output C. |
| RE4/P3B | 62 | | | |
| RE4 | | I/O | ST | Digital I/O. |
| P3B | | O | — | ECCP3 PWM output B. |
| RE5/P1C | 61 | | | |
| RE5 | | I/O | ST | Digital I/O. |
| P1C | | O | — | ECCP1 PWM output C. |
| RE6/P1B | 60 | | | |
| RE6 | | I/O | ST | Digital I/O. |
| P1B | | O | — | ECCP1 PWM output B. |
| RE7/ECCP2/P2A | 59 | | | |
| RE7 | | I/O | ST | Digital I/O. |
| ECCP2**(2)** | | I/O | ST | Capture 2 input/Compare 2 output/PWM 2 output. |
| P2A**(2)** | | O | — | ECCP2 PWM output A. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTF is a bidirectional I/O port. |
| RF1/AN6/C2OUT | 17 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| RF2/AN7/C1OUT | 16 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| RF3/AN8 | 15 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog input 8. |
| RF4/AN9 | 14 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog input 9. |
| RF5/AN10/CVREF | 13 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog input 10. |
| CVREF | | O | — | Comparator reference voltage output. |
| RF6/AN11 | 12 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog input 11. |
| RF7/$\overline{SS1}$ | 11 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| $\overline{SS1}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F6XJ10/6XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTG is a bidirectional I/O port. |
| RG0/ECCP3/P3A | 3 | | | |
| RG0 | | I/O | ST | Digital I/O. |
| ECCP3 | | I/O | ST | Capture 3 input/Compare 3 output/PWM 3 output. |
| P3A | | O | — | ECCP3 PWM output A. |
| RG1/TX2/CK2 | 4 | | | |
| RG1 | | I/O | ST | Digital I/O. |
| TX2 | | O | — | EUSART2 asynchronous transmit. |
| CK2 | | I/O | ST | EUSART2 synchronous clock (see related RX2/DT2). |
| RG2/RX2/DT2 | 5 | | | |
| RG2 | | I/O | ST | Digital I/O. |
| RX2 | | I | ST | EUSART2 asynchronous receive. |
| DT2 | | I/O | ST | EUSART2 synchronous data (see related TX2/CK2). |
| RG3/CCP4/P3D | 6 | | | |
| RG3 | | I/O | ST | Digital I/O. |
| CCP4 | | I/O | ST | Capture 4 input/Compare 4 output/PWM 4 output. |
| P3D | | O | — | ECCP3 PWM output D. |
| RG4/CCP5/P1D | 8 | | | |
| RG4 | | I/O | ST | Digital I/O. |
| CCP5 | | I/O | ST | Capture 5 input/Compare 5 output/PWM 5 output. |
| P1D | | O | — | ECCP1 PWM output D. |
| VSS | 9, 25, 41, 56 | P | — | Ground reference for logic and I/O pins. |
| VDD | 26, 38, 57 | P | — | Positive supply for peripheral digital logic and I/O pins. |
| AVSS | 20 | P | — | Ground reference for analog modules. |
| AVDD | 19 | P | — | Positive supply for analog modules. |
| ENVREG | 18 | I | ST | Enable for on-chip voltage regulator. |
| VDDCORE/VCAP | 10 | | | Core logic power or external filter capacitor connection. |
| VDDCORE | | P | — | Positive supply for microcontroller core logic (regulator disabled). |
| VCAP | | P | — | External filter capacitor connection (regulator enabled). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

**TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| $\overline{MCLR}$ | 9 | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| OSC1/CLKI | 49 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| OSC2/CLKO | 50 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 30 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 29 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/VREF- | 28 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/VREF+ | 27 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 34 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4 | 33 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).

**2:** Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

**3:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**4:** Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

**5:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

**TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0 | 58 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| INT0 | | I | ST | External interrupt 0. |
| FLT0 | | I | ST | ECCP1/2/3 Fault input. |
| RB1/INT1 | 57 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| INT1 | | I | ST | External interrupt 1. |
| RB2/INT2 | 56 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| INT2 | | I | ST | External interrupt 2. |
| RB3/INT3/ECCP2/P2A | 55 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| INT3 | | I | ST | External interrupt 3. |
| ECCP2(1) | | I/O | ST | Capture 2 input/Compare 2 output/PWM 2 output. |
| P2A(1) | | O | — | ECCP2 PWM output A. |
| RB4/KBI0 | 54 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| RB5/KBI1 | 53 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| RB6/KBI2/PGC | 52 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP™ programming clock pin. |
| RB7/KBI3/PGD | 47 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP™ programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).

**2:** Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

**3:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**4:** Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

**5:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

**TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 36 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/ECCP2/P2A | 35 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| ECCP2(2) | | I/O | ST | Capture 2 input/Compare 2 output/PWM 2 output. |
| P2A(2) | | O | — | ECCP2 PWM output A. |
| RC2/ECCP1/P1A | 43 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| ECCP1 | | I/O | ST | Capture 1 input/Compare 1 output/PWM 1 output. |
| P1A | | O | — | ECCP1 PWM output A. |
| RC3/SCK1/SCL1 | 44 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK1 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL1 | | I/O | $I^2C$/SMB | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI1/SDA1 | 45 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI1 | | I | ST | SPI data in. |
| SDA1 | | I/O | $I^2C$/SMB | $I^2C$ data I/O. |
| RC5/SDO1 | 46 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO1 | | O | — | SPI data out. |
| RC6/TX1/CK1 | 37 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART1 asynchronous transmit. |
| CK1 | | I/O | ST | EUSART1 synchronous clock (see related RX1/DT1). |
| RC7/RX1/DT1 | 38 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART1 asynchronous receive. |
| DT1 | | I/O | ST | EUSART1 synchronous data (see related TX1/CK1). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).

**2:** Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

**3:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**4:** Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

**5:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

**TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTD is a bidirectional I/O port. |
| RD0/AD0/PSP0 | 72 | | | |
| RD0 | | I/O | ST | Digital I/O. |
| AD0 | | I/O | TTL | External memory address/data 0. |
| PSP0 | | I/O | TTL | Parallel Slave Port data. |
| RD1/AD1/PSP1 | 69 | | | |
| RD1 | | I/O | ST | Digital I/O. |
| AD1 | | I/O | TTL | External memory address/data 1. |
| PSP1 | | I/O | TTL | Parallel Slave Port data. |
| RD2/AD2/PSP2 | 68 | | | |
| RD2 | | I/O | ST | Digital I/O. |
| AD2 | | I/O | TTL | External memory address/data 2. |
| PSP2 | | I/O | TTL | Parallel Slave Port data. |
| RD3/AD3/PSP3 | 67 | | | |
| RD3 | | I/O | ST | Digital I/O. |
| AD3 | | I/O | TTL | External memory address/data 3. |
| PSP3 | | I/O | TTL | Parallel Slave Port data. |
| RD4/AD4/PSP4/SDO2 | 66 | | | |
| RD4 | | I/O | ST | Digital I/O. |
| AD4 | | I/O | TTL | External memory address/data 4. |
| PSP4 | | I/O | TTL | Parallel Slave Port data. |
| SDO2 | | O | — | SPI data out. |
| RD5/AD5/PSP5/ SDI2/SDA2 | 65 | | | |
| RD5 | | I/O | ST | Digital I/O. |
| AD5 | | I/O | TTL | External memory address/data 5. |
| PSP5 | | I/O | TTL | Parallel Slave Port data. |
| SDI2 | | I | ST | SPI data in. |
| SDA2 | | I/O | $I^2C$/SMB | $I^2C$™ data I/O. |
| RD6/AD6/PSP6/ SCK2/SCL2 | 64 | | | |
| RD6 | | I/O | ST | Digital I/O. |
| AD6 | | I/O | TTL | External memory address/data 6. |
| PSP6 | | I/O | TTL | Parallel Slave Port data. |
| SCK2 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL2 | | I/O | $I^2C$/SMB | Synchronous serial clock input/output for $I^2C$ mode. |
| RD7/AD7/PSP7/$\overline{SS2}$ | 63 | | | |
| RD7 | | I/O | ST | Digital I/O. |
| AD7 | | I/O | TTL | External memory address/data 7. |
| PSP7 | | I/O | TTL | Parallel Slave Port data. |
| $\overline{SS2}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).

**2:** Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

**3:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**4:** Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

**5:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

**TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTE is a bidirectional I/O port. |
| RE0/AD8/$\overline{RD}$/P2D | 4 | | | |
| RE0 | | I/O | ST | Digital I/O. |
| AD8 | | I/O | TTL | External memory address/data 8. |
| $\overline{RD}$ | | I | TTL | Read control for Parallel Slave Port. |
| P2D | | O | — | ECCP2 PWM output D. |
| RE1/AD9/$\overline{WR}$/P2C | 3 | | | |
| RE1 | | I/O | ST | Digital I/O. |
| AD9 | | I/O | TTL | External memory address/data 9. |
| $\overline{WR}$ | | I | TTL | Write control for Parallel Slave Port. |
| P2C | | O | — | ECCP2 PWM output C. |
| RE2/AD10/$\overline{CS}$/P2B | 78 | | | |
| RE2 | | I/O | ST | Digital I/O. |
| AD10 | | I/O | TTL | External memory address/data 10. |
| $\overline{CS}$ | | I | TTL | Chip select control for Parallel Slave Port. |
| P2B | | O | — | ECCP2 PWM output B. |
| RE3/AD11/P3C | 77 | | | |
| RE3 | | I/O | ST | Digital I/O. |
| AD11 | | I/O | TTL | External memory address/data 11. |
| P3C(3) | | O | — | ECCP3 PWM output C. |
| RE4/AD12/P3B | 76 | | | |
| RE4 | | I/O | ST | Digital I/O. |
| AD12 | | I/O | TTL | External memory address/data 12. |
| P3B(3) | | O | — | ECCP3 PWM output B. |
| RE5/AD13/P1C | 75 | | | |
| RE5 | | I/O | ST | Digital I/O. |
| AD13 | | I/O | TTL | External memory address/data 13. |
| P1C(3) | | O | — | ECCP1 PWM output C. |
| RE6/AD14/P1B | 74 | | | |
| RE6 | | I/O | ST | Digital I/O. |
| AD14 | | I/O | TTL | External memory address/data 14. |
| P1B(3) | | O | — | ECCP1 PWM output B. |
| RE7/AD15/ECCP2/P2A | 73 | | | |
| RE7 | | I/O | ST | Digital I/O. |
| AD15 | | I/O | TTL | External memory address/data 15. |
| ECCP2(4) | | I/O | ST | Capture 2 input/Compare 2 output/PWM 2 output. |
| P2A(4) | | O | — | ECCP2 PWM output A. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).

**2:** Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

**3:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**4:** Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

**5:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

**TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTF is a bidirectional I/O port. |
| RF1/AN6/C2OUT | 23 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| RF2/AN7/C1OUT | 18 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| RF3/AN8 | 17 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog input 8. |
| RF4/AN9 | 16 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog input 9. |
| RF5/AN10/CVREF | 15 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog input 10. |
| CVREF | | O | — | Comparator reference voltage output. |
| RF6/AN11 | 14 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog input 11. |
| RF7/$\overline{SS1}$ | 13 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| $\overline{SS1}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).

**2:** Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

**3:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**4:** Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

**5:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

**TABLE 1-4: PIC18F8XJ10/8XJ15 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTG is a bidirectional I/O port. |
| RG0/ECCP3/P3A | 5 | | | |
| RG0 | | I/O | ST | Digital I/O. |
| ECCP3 | | I/O | ST | Capture 3 input/Compare 3 output/PWM 3 output. |
| P3A | | O | — | ECCP3 PWM output A. |
| RG1/TX2/CK2 | 6 | | | |
| RG1 | | I/O | ST | Digital I/O. |
| TX2 | | O | — | EUSART2 asynchronous transmit. |
| CK2 | | I/O | ST | EUSART2 synchronous clock (see related RX2/DT2). |
| RG2/RX2/DT2 | 7 | | | |
| RG2 | | I/O | ST | Digital I/O. |
| RX2 | | I | ST | EUSART2 asynchronous receive. |
| DT2 | | I/O | ST | EUSART2 synchronous data (see related TX2/CK2). |
| RG3/CCP4/P3D | 8 | | | |
| RG3 | | I/O | ST | Digital I/O. |
| CCP4 | | I/O | ST | Capture 4 input/Compare 4 output/PWM 4 output. |
| P3D | | O | — | ECCP3 PWM output D. |
| RG4/CCP5/P1D | 10 | | | |
| RG4 | | I/O | ST | Digital I/O. |
| CCP5 | | I/O | ST | Capture 5 input/Compare 5 output/PWM 5 output. |
| P1D | | O | — | ECCP1 PWM output D. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$/SMB = $I^2C$™/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared (Extended Microcontroller mode).

**2:** Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

**3:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**4:** Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

**5:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).