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# PIC18F97J60 Family Data Sheet

## 64/80/100-Pin, High-Performance, 1-Mbit Flash Microcontrollers with Ethernet

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# PIC18F97J60 FAMILY

## 64/80/100-Pin High-Performance, 1-Mbit Flash Microcontrollers with Ethernet

### Ethernet Features:

- IEEE 802.3™ Compatible Ethernet Controller
- Fully Compatible with 10/100/1000Base-T Networks
- Integrated MAC and 10Base-T PHY
- 8-Kbyte Transmit/Receive Packet Buffer SRAM
- Supports One 10Base-T Port
- Programmable Automatic Retransmit on Collision
- Programmable Padding and CRC Generation
- Programmable Automatic Rejection of Erroneous Packets
- Activity Outputs for 2 LED Indicators
- Buffer:
  - Configurable transmit/receive buffer size
  - Hardware-managed circular receive FIFO
  - Byte-wide random and sequential access
  - Internal DMA for fast memory copying
  - Hardware assisted checksum calculation for various protocols
- MAC:
  - Support for Unicast, Multicast and Broadcast packets
  - Programmable Pattern Match of up to 64 bytes within packet at user-defined offset
  - Programmable wake-up on multiple packet formats
- PHY:
  - Wave shaping output filter

### Flexible Oscillator Structure:

- Selectable System Clock derived from Single 25 MHz External Source:
  - 2.778 to 41.667 MHz
- Internal 31 kHz Oscillator
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if oscillator stops
- Two-Speed Oscillator Start-up

### External Memory Bus (100-pin devices only):

- Address Capability of up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 12-Bit, 16-Bit and 20-Bit Addressing modes

### Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA on PORTB and PORTC
- Five Timer modules (Timer0 to Timer4)
- Four External Interrupt pins
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Up to Two Master Synchronous Serial Port (MSSP) modules supporting SPI (all 4 modes) and $I^2C$™ Master and Slave modes
- Up to Two Enhanced USART modules:
  - Supports RS-485, RS-232 and LIN/J2602
  - Auto-wake-up on Start bit
  - Auto-Baud Detect (ABD)
- 10-Bit, Up to 16-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
- Dual Analog Comparators with Input Multiplexing
- Parallel Slave Port (PSP) module (100-pin devices only)

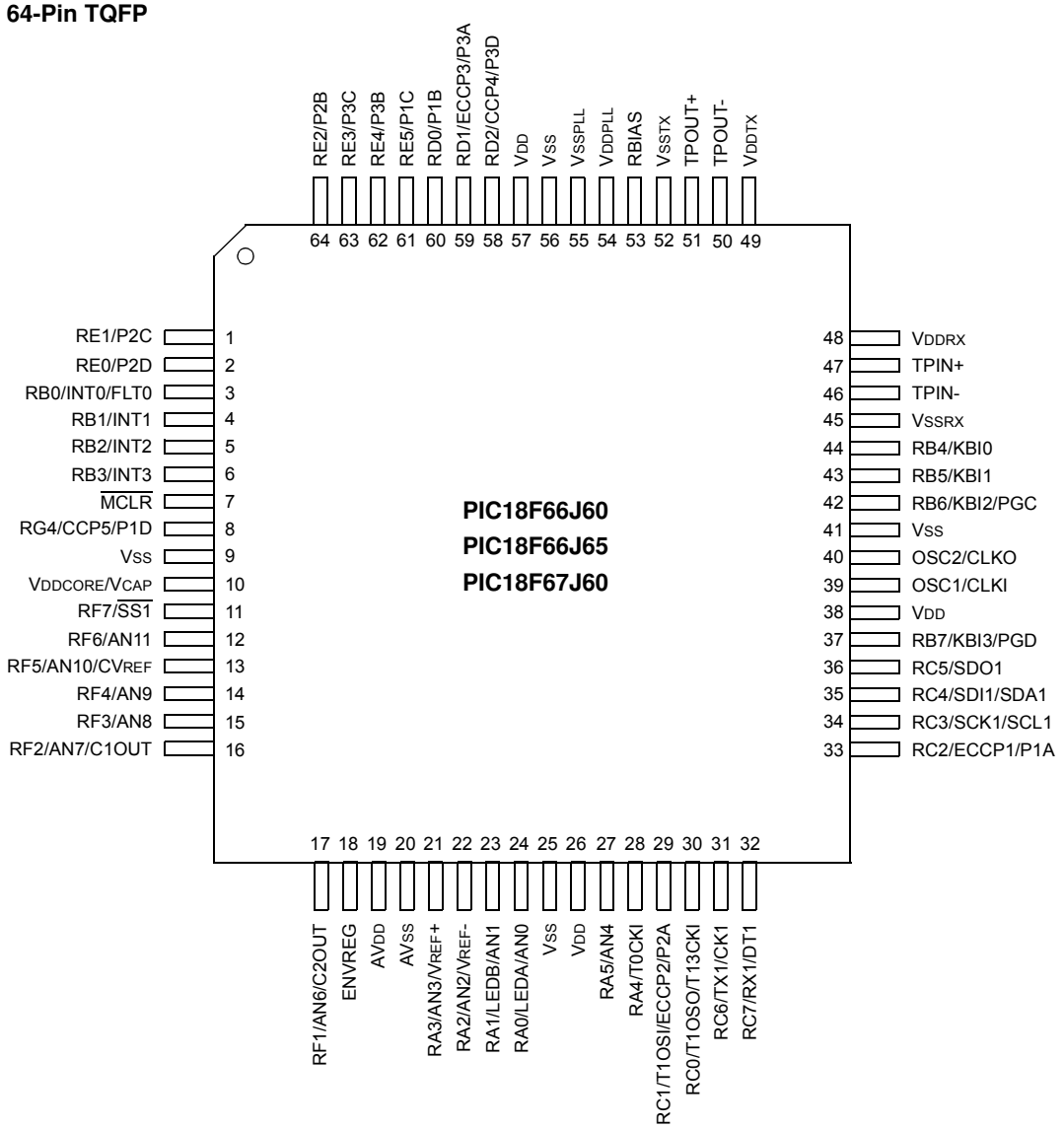
### Special Microcontroller Features:

- 5.5V Tolerant Inputs (digital-only pins)
- Low-Power, High-Speed CMOS Flash Technology:
  - Self-reprogrammable under software control
- C compiler Optimized Architecture for Reentrant Code
- Power Management Features:
  - Run: CPU on, peripherals on
  - Idle: CPU off, peripherals on
  - Sleep: CPU off, peripherals off
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 134s
- Single-Supply 3.3V In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with 3 Breakpoints via Two Pins
- Operating Voltage Range of 2.35V to 3.6V (3.1V to 3.6V using Ethernet module)
- On-Chip 2.5V Regulator

| Device | Flash Program Memory (bytes) | SRAM Data Memory (bytes) | Ethernet TX/RX Buffer (bytes) | I/O | 10-Bit A/D (ch) | CCP/ ECCP | MSSP | | | EUSART | Comparators | Timers 8/16-Bit | PSP | External Memory Bus |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SPI | Master $I^2C$™ | | | | | |
| PIC18F66J60 | 64K | 3808 | 8192 | 39 | 11 | 2/3 | 1 | Y | Y | 1 | 2 | 2/3 | N | N |
| PIC18F66J65 | 96K | 3808 | 8192 | 39 | 11 | 2/3 | 1 | Y | Y | 1 | 2 | 2/3 | N | N |
| PIC18F67J60 | 128K | 3808 | 8192 | 39 | 11 | 2/3 | 1 | Y | Y | 1 | 2 | 2/3 | N | N |
| PIC18F86J60 | 64K | 3808 | 8192 | 55 | 15 | 2/3 | 1 | Y | Y | 2 | 2 | 2/3 | N | N |
| PIC18F86J65 | 96K | 3808 | 8192 | 55 | 15 | 2/3 | 1 | Y | Y | 2 | 2 | 2/3 | N | N |
| PIC18F87J60 | 128K | 3808 | 8192 | 55 | 15 | 2/3 | 1 | Y | Y | 2 | 2 | 2/3 | N | N |
| PIC18F96J60 | 64K | 3808 | 8192 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y | Y |
| PIC18F96J65 | 96K | 3808 | 8192 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y | Y |
| PIC18F97J60 | 128K | 3808 | 8192 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y | Y |

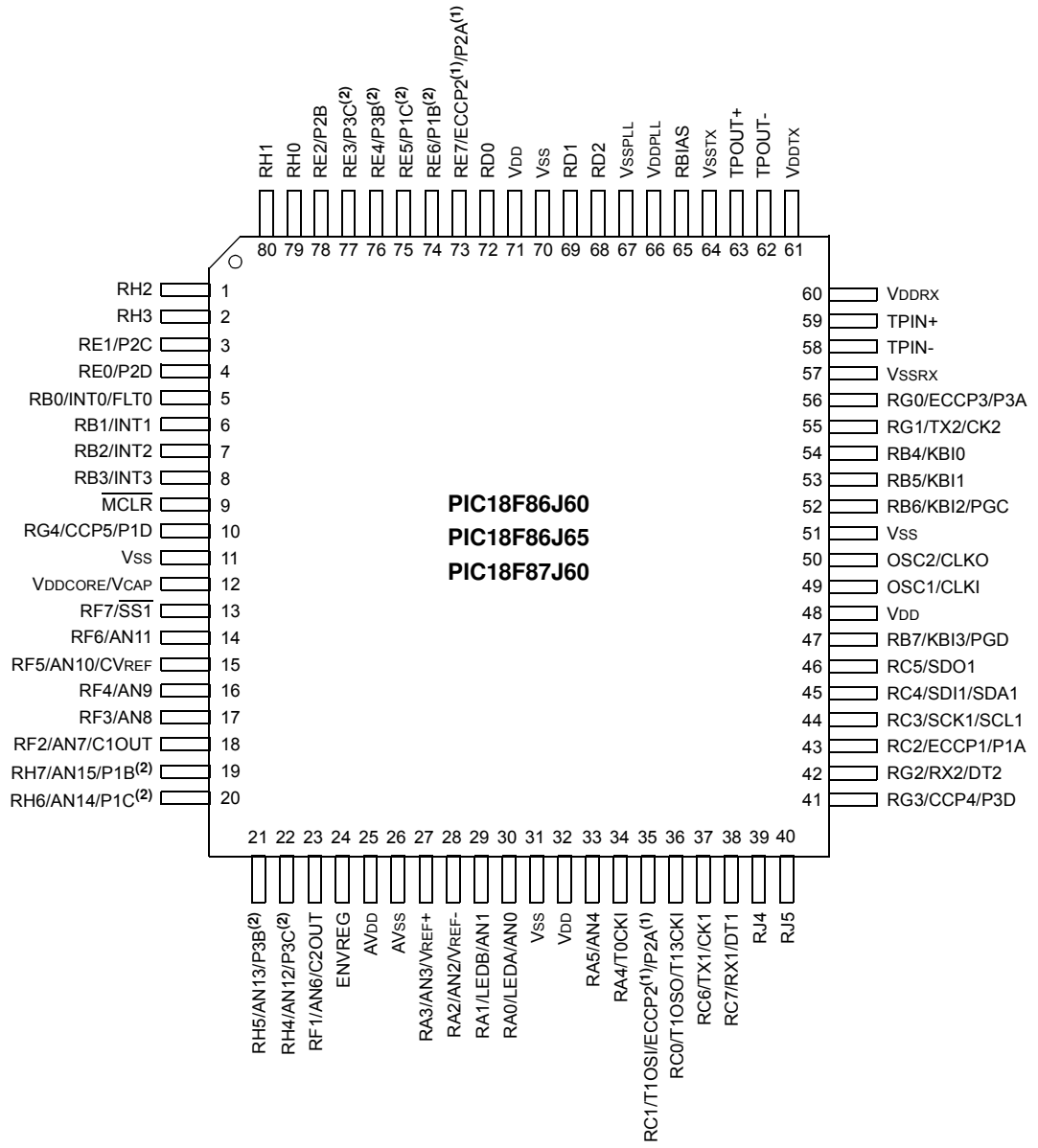
## Pin Diagrams

**64-Pin TQFP**



## Pin Diagrams (Continued)

**80-Pin TQFP**

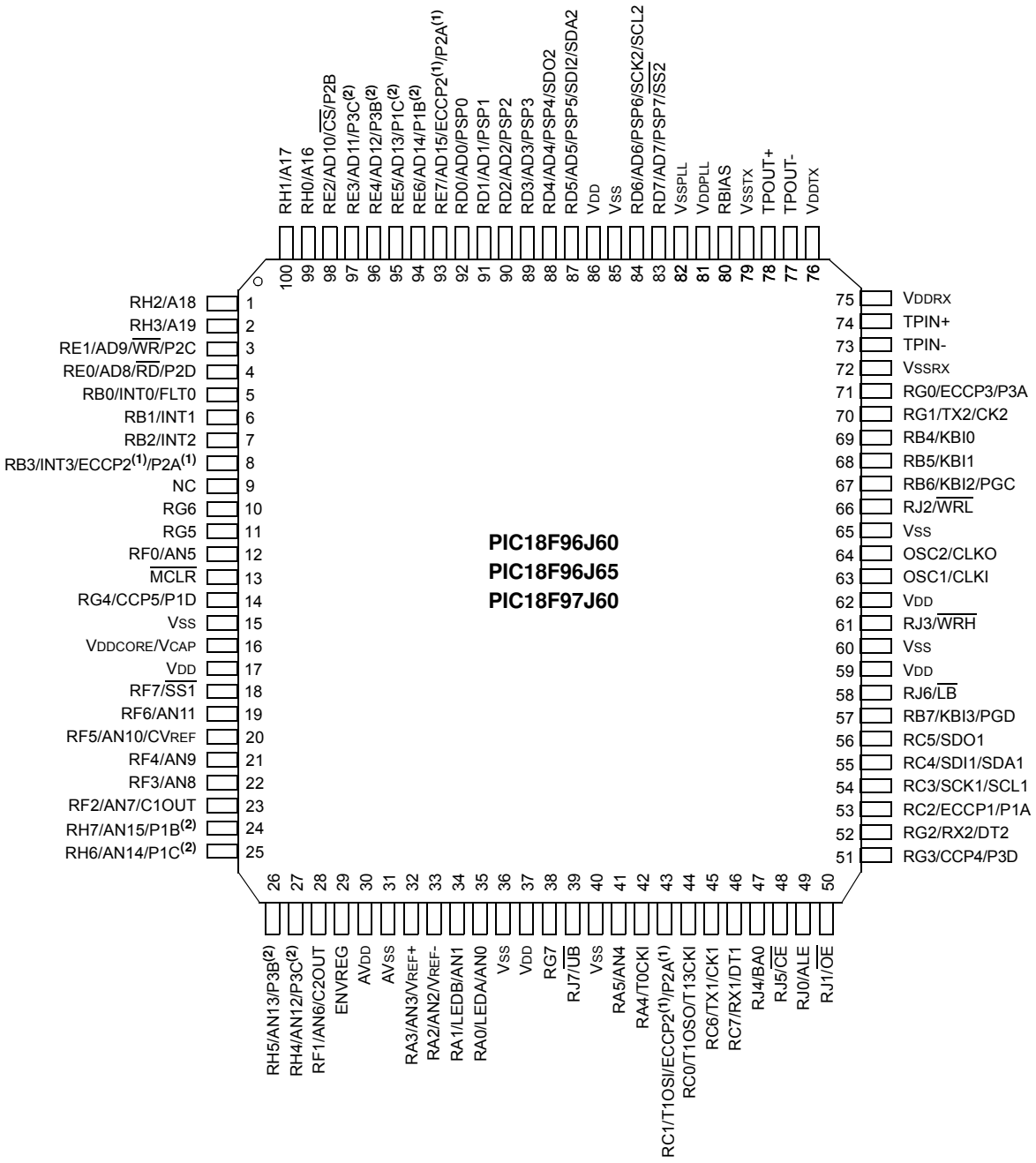



**Note 1:** The ECCP2/P2A pin placement depends on the CCP2MX Configuration bit setting.

**2:** P1B, P1C, P3B and P3C pin placement depends on the ECCPMX Configuration bit setting.

## Pin Diagrams (Continued)

**100-Pin TQFP**




**Note 1:** The ECCP2/P2A pin placement depends on the CCP2MX Configuration bit and Processor mode settings.

**2:** P1B, P1C, P3B and P3C pin placement depends on the ECCPMX Configuration bit setting.

## Table of Contents

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**NOTES:**

# 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F66J60
- PIC18F66J65
- PIC18F67J60
- PIC18F86J60
- PIC18F86J65
- PIC18F87J60
- PIC18F96J60
- PIC18F96J65
- PIC18F97J60

This family introduces a new line of low-voltage devices with the foremost traditional advantage of all PIC18 microcontrollers – namely, high computational performance and a rich feature set at an extremely competitive price point. These features make the PIC18F97J60 family a logical choice for many high-performance applications where cost is a primary consideration.

## 1.1 Core Features

### 1.1.1 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F97J60 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These options include:

- Two Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of a divide-by-4 clock output.
- A Phase Lock Loop (PLL) frequency multiplier, available to the external oscillator modes, which allows clock speeds of up to 41.667 MHz.
- An internal RC oscillator with a fixed 31 kHz output which provides an extremely low-power option for timing-insensitive applications.

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

### 1.1.2 EXPANDED MEMORY

The PIC18F97J60 family provides ample room for application code, from 64 Kbytes to 128 Kbytes of code space. The Flash cells for program memory are rated to last 100 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 20 years.

The PIC18F97J60 family also provides plenty of room for dynamic application data with 3808 bytes of data RAM.

### 1.1.3 EXTERNAL MEMORY BUS

In the unlikely event that 128 Kbytes of memory are inadequate for an application, the 100-pin members of the PIC18F97J60 family also implement an External Memory Bus (EMB). This allows the controller's internal program counter to address a memory space of up to 2 Mbytes, permitting a level of data access that few 8-bit devices can claim. This allows additional memory options, including:

- Using combinations of on-chip and external memory up to the 2-Mbyte limit
- Using external Flash memory for reprogrammable application code or large data tables
- Using external RAM devices for storing large amounts of variable data

### 1.1.4 EXTENDED INSTRUCTION SET

The PIC18F97J60 family implements the optional extension to the PIC18 instruction set, adding eight new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize reentrant application code originally developed in high-level languages, such as C.

### 1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

## 1.2 Other Special Features

- **Communications:** The PIC18F97J60 family incorporates a range of serial communication peripherals, including up to two independent Enhanced USARTs and up to two Master SSP modules, capable of both SPI and $I^2C$™ (Master and Slave) modes of operation. In addition, one of the general purpose I/O ports can be reconfigured as an 8-bit Parallel Slave Port for direct processor-to-processor communications.
- **CCP Modules:** All devices in the family incorporate two Capture/Compare/PWM (CCP) modules and three Enhanced CCP (ECCP) modules to maximize flexibility in control applications. Up to four different time bases may be used to perform several different operations at once. Each of the three ECCP modules offers up to four PWM outputs, allowing for a total of twelve PWMs. The ECCP modules also offer many beneficial features, including polarity selection, programmable dead time, auto-shutdown and restart and Half-Bridge and Full-Bridge Output modes.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reducing code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range. See **Section 28.0 "Electrical Characteristics"** for time-out periods.

## 1.3 Details on Individual Family Members

Devices in the PIC18F97J60 family are available in 64-pin, 80-pin and 100-pin packages. Block diagrams for the three groups are shown in Figure 1-1, Figure 1-2 and Figure 1-3.

The devices are differentiated from each other in four ways:

1. Flash program memory (three sizes, ranging from 64 Kbytes for PIC18FX6J60 devices to 128 Kbytes for PIC18FX7J60 devices).
2. A/D channels (eleven for 64-pin devices, fifteen for 80-pin pin devices and sixteen for 100-pin devices).
3. Serial communication modules (one EUSART module and one MSSP module on 64-pin devices, two EUSART modules and one MSSP module on 80-pin devices and two EUSART modules and two MSSP modules on 100-pin devices).
4. I/O pins (39 on 64-pin devices, 55 on 80-pin devices and 70 on 100-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

The pinouts for all devices are listed in Table 1-4, Table 1-5 and Table 1-6.

**TABLE 1-1: DEVICE FEATURES FOR THE PIC18F97J60 FAMILY (64-PIN DEVICES)**

| Features | PIC18F66J60 | PIC18F66J65 | PIC18F67J60 |
|---|---|---|---|
| Operating Frequency | DC – 41.667 MHz | DC – 41.667 MHz | DC – 41.667 MHz |
| Program Memory (Bytes) | 64K | 96K | 128K |
| Program Memory (Instructions) | 32764 | 49148 | 65532 |
| Data Memory (Bytes) | 3808 | | |
| Interrupt Sources | 26 | | |
| I/O Ports | Ports A, B, C, D, E, F, G | | |
| I/O Pins | 39 | | |
| Timers | 5 | | |
| Capture/Compare/PWM Modules | 2 | | |
| Enhanced Capture/Compare/PWM Modules | 3 | | |
| Serial Communications | MSSP (1), Enhanced USART (1) | | |
| Ethernet Communications (10Base-T) | Yes | | |
| Parallel Slave Port Communications (PSP) | No | | |
| External Memory Bus | No | | |
| 10-Bit Analog-to-Digital Module | 11 Input Channels | | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$ , WDT (PWRT, OST) | | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | | |
| Packages | 64-Pin TQFP | | |

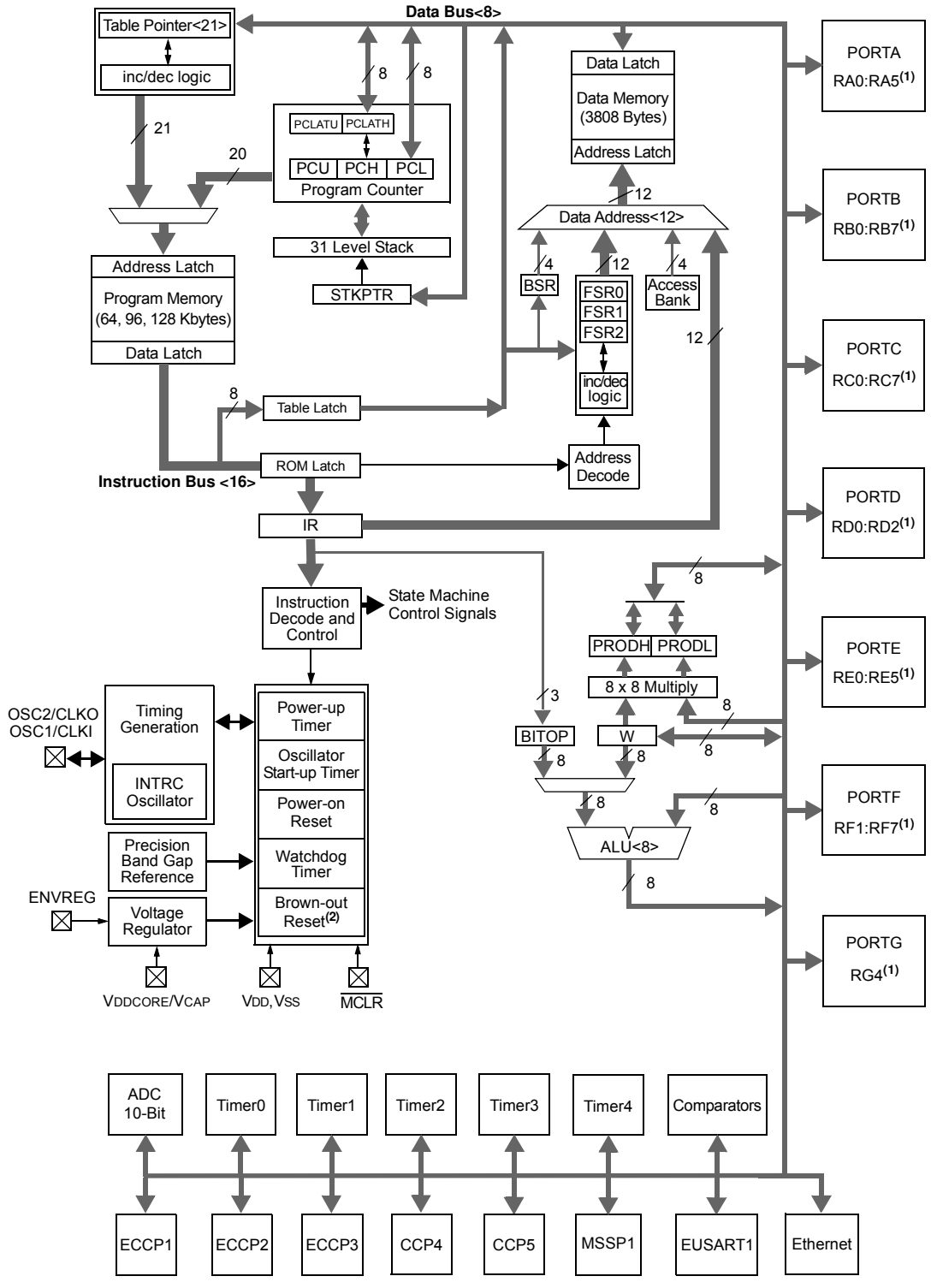
**TABLE 1-2: DEVICE FEATURES FOR THE PIC18F97J60 FAMILY (80-PIN DEVICES)**

| Features | PIC18F86J60 | PIC18F86J65 | PIC18F87J60 |
|---|---|---|---|
| Operating Frequency | DC – 41.667 MHz | DC – 41.667 MHz | DC – 41.667 MHz |
| Program Memory (Bytes) | 64K | 96K | 128K |
| Program Memory (Instructions) | 32764 | 49148 | 65532 |
| Data Memory (Bytes) | 3808 | | |
| Interrupt Sources | 27 | | |
| I/O Ports | Ports A, B, C, D, E, F, G, H, J | | |
| I/O Pins | 55 | | |
| Timers | 5 | | |
| Capture/Compare/PWM Modules | 2 | | |
| Enhanced Capture/Compare/PWM Modules | 3 | | |
| Serial Communications | MSSP (1), Enhanced USART (2) | | |
| Ethernet Communications (10Base-T) | Yes | | |
| Parallel Slave Port Communications (PSP) | No | | |
| External Memory Bus | No | | |
| 10-Bit Analog-to-Digital Module | 15 Input Channels | | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$ , WDT (PWRT, OST) | | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | | |
| Packages | 80-Pin TQFP | | |

**TABLE 1-3: DEVICE FEATURES FOR THE PIC18F97J60 FAMILY (100-PIN DEVICES)**

| Features | PIC18F96J60 | PIC18F96J65 | PIC18F97J60 |
|---|---|---|---|
| Operating Frequency | DC – 41.667 MHz | DC – 41.667 MHz | DC – 41.667 MHz |
| Program Memory (Bytes) | 64K | 96K | 128K |
| Program Memory (Instructions) | 32764 | 49148 | 65532 |
| Data Memory (Bytes) | 3808 | | |
| Interrupt Sources | 29 | | |
| I/O Ports | Ports A, B, C, D, E, F, G, H, J | | |
| I/O Pins | 70 | | |
| Timers | 5 | | |
| Capture/Compare/PWM Modules | 2 | | |
| Enhanced Capture/Compare/PWM Modules | 3 | | |
| Serial Communications | MSSP (2), Enhanced USART (2) | | |
| Ethernet Communications (10Base-T) | Yes | | |
| Parallel Slave Port Communications (PSP) | Yes | | |
| External Memory Bus | Yes | | |
| 10-Bit Analog-to-Digital Module | 16 Input Channels | | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$ , WDT (PWRT, OST) | | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | | |
| Packages | 100-Pin TQFP | | |

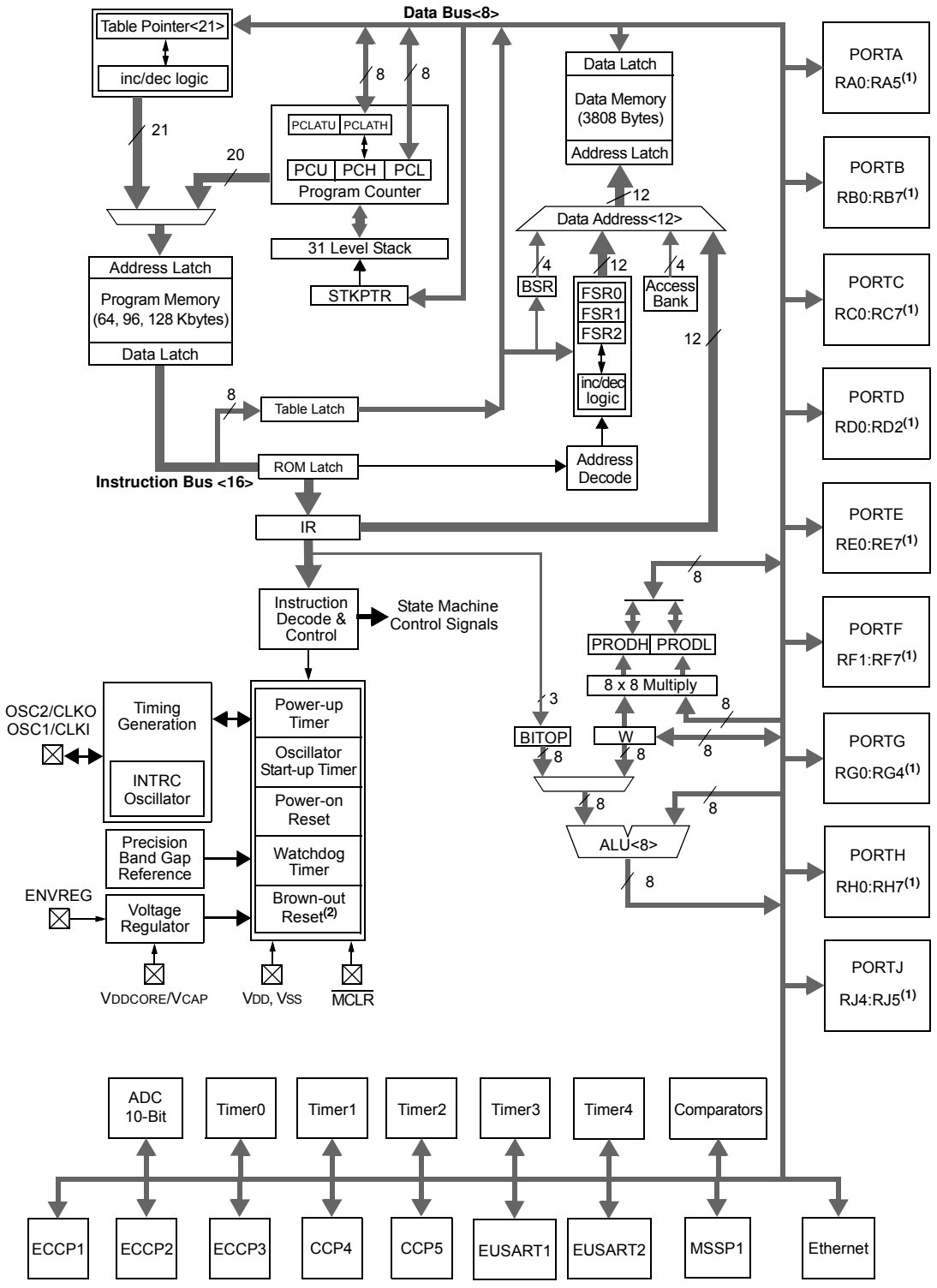
**FIGURE 1-1: PIC18F66J60/66J65/67J60 (64-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-4 for I/O port pin descriptions.

**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

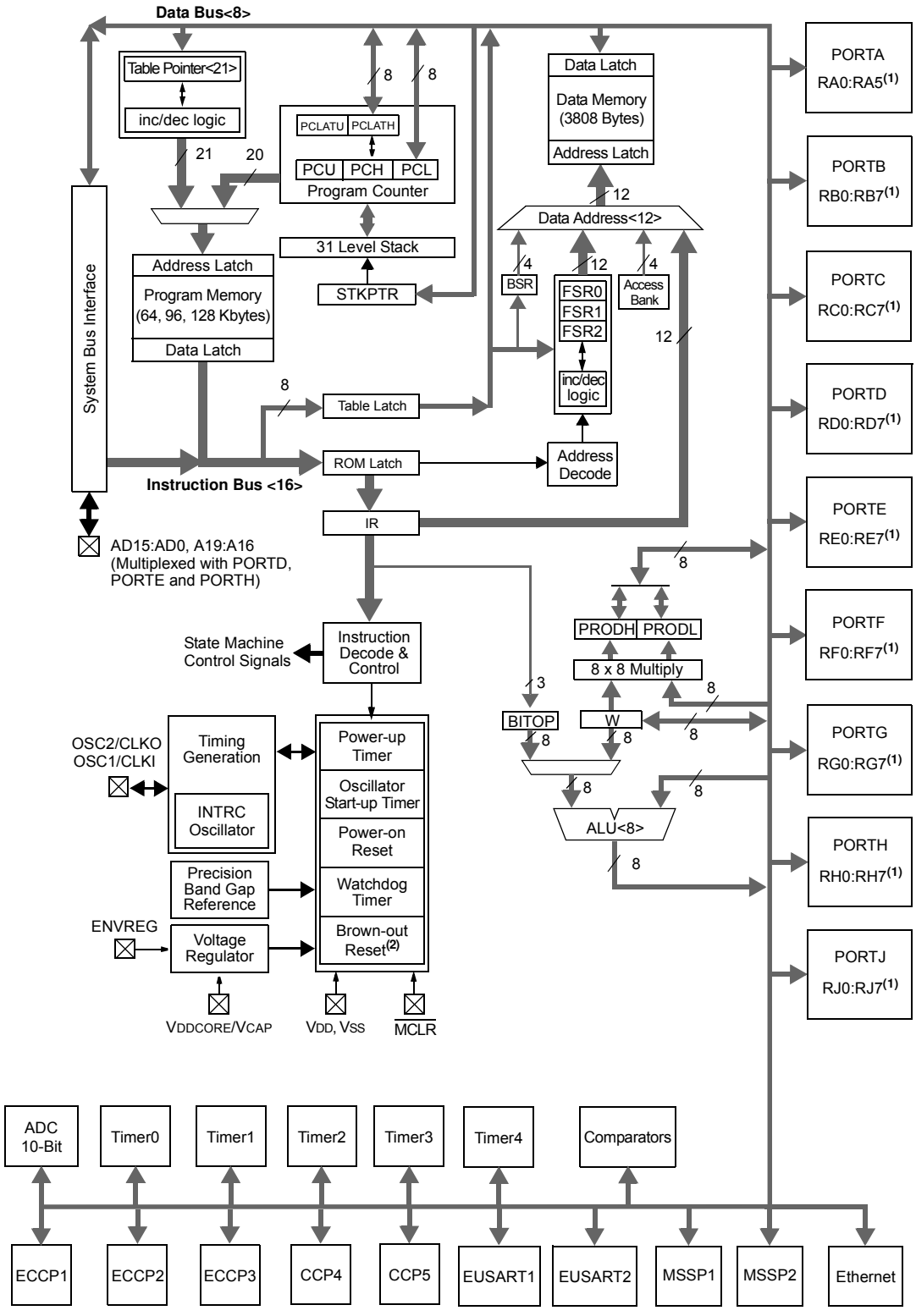
**FIGURE 1-2: PIC18F86J60/86J65/87J60 (80-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-5 for I/O port pin descriptions.

**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

**FIGURE 1-3: PIC18F96J60/96J65/97J60 (100-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-6 for I/O port pin descriptions.

**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

**TABLE 1-4: PIC18F66J60/66J65/67J60 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| $\overline{MCLR}$ | 7 | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| OSC1/CLKI | 39 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in internal RC mode; CMOS otherwise. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function, OSC1. (See related OSC2/CLKO pin.) |
| OSC2/CLKO | 40 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In Internal RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/LEDA/AN0 | 24 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| LEDA | | O | — | Ethernet LEDA indicator output. |
| AN0 | | I | Analog | Analog Input 0. |
| RA1/LEDB/AN1 | 23 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| LEDB | | O | — | Ethernet LEDB indicator output. |
| AN1 | | I | Analog | Analog Input 1. |
| RA2/AN2/$V_{REF-}$ | 22 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog Input 2. |
| $V_{REF-}$ | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/$V_{REF+}$ | 21 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog Input 3. |
| $V_{REF+}$ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 28 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4 | 27 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog Input 4. |

**Legend:** TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to $V_{DD}$)

**TABLE 1-4: PIC18F66J60/66J65/67J60 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0 | 3 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| INT0 | | I | ST | External Interrupt 0. |
| FLT0 | | I | ST | Enhanced PWM Fault input (ECCP modules); enabled in software. |
| RB1/INT1 | 4 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| INT1 | | I | ST | External Interrupt 1. |
| RB2/INT2 | 5 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| INT2 | | I | ST | External Interrupt 2. |
| RB3/INT3 | 6 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| INT3 | | I | ST | External Interrupt 3. |
| RB4/KBI0 | 44 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| RB5/KBI1 | 43 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| RB6/KBI2/PGC | 42 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP™ programming clock pin. |
| RB7/KBI3/PGD | 37 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$)

**TABLE 1-4: PIC18F66J60/66J65/67J60 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 30 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/ECCP2/P2A | 29 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| ECCP2 | | I/O | ST | Capture 2 input/Compare 2 output/PWM2 output. |
| P2A | | O | — | ECCP2 PWM Output A. |
| RC2/ECCP1/P1A | 33 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| ECCP1 | | I/O | ST | Capture 1 input/Compare 1 output/PWM1 output. |
| P1A | | O | — | ECCP1 PWM Output A. |
| RC3/SCK1/SCL1 | 34 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK1 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL1 | | I/O | ST | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI1/SDA1 | 35 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI1 | | I | ST | SPI data in. |
| SDA1 | | I/O | ST | $I^2C$ data I/O. |
| RC5/SDO1 | 36 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO1 | | O | — | SPI data out. |
| RC6/TX1/CK1 | 31 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART1 asynchronous transmit. |
| CK1 | | I/O | ST | EUSART1 synchronous clock (see related RX1/DT1 pin). |
| RC7/RX1/DT1 | 32 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART1 asynchronous receive. |
| DT1 | | I/O | ST | EUSART1 synchronous data (see related TX1/CK1 pin). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

**TABLE 1-4: PIC18F66J60/66J65/67J60 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTD is a bidirectional I/O port. |
| RD0/P1B | 60 | | | |
| RD0 | | I/O | ST | Digital I/O. |
| P1B | | O | — | ECCP1 PWM Output B. |
| RD1/ECCP3/P3A | 59 | | | |
| RD1 | | I/O | ST | Digital I/O. |
| ECCP3 | | I/O | ST | Capture 3 input/Compare 3 output/PWM3 output. |
| P3A | | O | — | ECCP3 PWM Output A. |
| RD2/CCP4/P3D | 58 | | | |
| RD2 | | I/O | ST | Digital I/O. |
| CCP4 | | I/O | ST | Capture 4 input/Compare 4 output/PWM4 output. |
| P3D | | O | — | CCP4 PWM Output D. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$)

**TABLE 1-4: PIC18F66J60/66J65/67J60 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTE is a bidirectional I/O port. |
| RE0/P2D | 2 | | | |
| RE0 | | I/O | ST | Digital I/O. |
| P2D | | O | — | ECCP2 PWM Output D. |
| RE1/P2C | 1 | | | |
| RE1 | | I/O | ST | Digital I/O. |
| P2C | | O | — | ECCP2 PWM Output C. |
| RE2/P2B | 64 | | | |
| RE2 | | I/O | ST | Digital I/O. |
| P2B | | O | — | ECCP2 PWM Output B. |
| RE3/P3C | 63 | | | |
| RE3 | | I/O | ST | Digital I/O. |
| P3C | | O | — | ECCP3 PWM Output C. |
| RE4/P3B | 62 | | | |
| RE4 | | I/O | ST | Digital I/O. |
| P3B | | O | — | ECCP3 PWM Output B. |
| RE5/P1C | 61 | | | |
| RE5 | | I/O | ST | Digital I/O. |
| P1C | | O | — | ECCP1 PWM Output C. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

**TABLE 1-4: PIC18F66J60/66J65/67J60 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTF is a bidirectional I/O port. |
| RF1/AN6/C2OUT | 17 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog Input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| RF2/AN7/C1OUT | 16 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog Input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| RF3/AN8 | 15 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog Input 8. |
| RF4/AN9 | 14 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog Input 9. |
| RF5/AN10/CVREF | 13 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog Input 10. |
| CVREF | | O | — | Comparator reference voltage output. |
| RF6/AN11 | 12 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog Input 11. |
| RF7/$\overline{SS1}$ | 11 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| $\overline{SS1}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

**TABLE 1-4: PIC18F66J60/66J65/67J60 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| RG4/CCP5/P1D | 8 | | | PORTG is a bidirectional I/O port. |
| RG4 | | I/O | ST | Digital I/O. |
| CCP5 | | I/O | ST | Capture 5 input/Compare 5 output/PWM5 output. |
| P1D | | O | — | ECCP1 PWM Output D. |
| VSS | 9, 25, 41, 56 | P | — | Ground reference for logic and I/O pins. |
| VDD | 26, 38, 57 | P | — | Positive supply for peripheral digital logic and I/O pins. |
| AVSS | 20 | P | — | Ground reference for analog modules. |
| AVDD | 19 | P | — | Positive supply for analog modules. |
| ENVREG | 18 | I | ST | Enable for on-chip voltage regulator. |
| VDDCORE/VCAP | 10 | | | Core logic power or external filter capacitor connection. |
| VDDCORE | | P | — | Positive supply for microcontroller core logic (regulator disabled). |
| VCAP | | P | — | External filter capacitor connection (regulator enabled). |
| VSSPLL | 55 | P | — | Ground reference for Ethernet PHY PLL. |
| VDDPLL | 54 | P | — | Positive 3.3V supply for Ethernet PHY PLL. |
| VSSTX | 52 | P | — | Ground reference for Ethernet PHY transmit subsystem. |
| VDDTX | 49 | P | — | Positive 3.3V supply for Ethernet PHY transmit subsystem. |
| VSSRX | 45 | P | — | Ground reference for Ethernet PHY receive subsystem. |
| VDDRX | 48 | P | — | Positive 3.3V supply for Ethernet PHY receive subsystem. |
| RBIAS | 53 | I | Analog | Bias current for Ethernet PHY. Must be tied to VSS via a resistor; see **Section 19.0 "Ethernet Module"** for specification. |
| TPOUT+ | 51 | O | — | Ethernet differential signal output. |
| TPOUT- | 50 | O | — | Ethernet differential signal output. |
| TPIN+ | 47 | I | Analog | Ethernet differential signal input. |
| TPIN- | 46 | I | Analog | Ethernet differential signal input. |

**Legend:** TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; CMOS = CMOS compatible input or output; Analog = Analog input; O = Output; OD = Open-Drain (no P diode to VDD)

**TABLE 1-5: PIC18F86J60/86J65/87J60 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| $\overline{MCLR}$ | 9 | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| OSC1/CLKI | 49 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in internal RC mode; CMOS otherwise. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function, OSC1. (See related OSC2/CLKO pin.) |
| OSC2/CLKO | 50 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In Internal RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/LEDA/AN0 | 30 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| LEDA | | O | — | Ethernet LEDA indicator output. |
| AN0 | | I | Analog | Analog Input 0. |
| RA1/LEDB/AN1 | 29 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| LEDB | | O | — | Ethernet LEDB indicator output. |
| AN1 | | I | Analog | Analog Input 1. |
| RA2/AN2/VREF- | 28 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog Input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/VREF+ | 27 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog Input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 34 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4 | 33 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog Input 4. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

**2:** Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

**3:** Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

**4:** Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).