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PIC18F87J50 Family Data Sheet

64/80-Pin High-Performance, 1-Mbit Flash USB Microcontrollers with nanoWatt Technology

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- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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PIC18F87J50 FAMILY

64/80-Pin High-Performance, 1-Mbit Flash USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant SIE
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 3.9-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver

Flexible Oscillator Structure:

- High-Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal 31 kHz Oscillator, Tunable Internal Oscillator, 31 kHz to 8 MHz
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source 25 mA/25mA (PORTB and PORTC)
- Four Programmable External Interrupts
- Four Input Change Interrupts
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Two Master Synchronous Serial Port (MSSP) modules supporting 3-Wire SPI (all 4 modes) and I^2C™ Master and Slave modes
- 8-Bit Parallel Master Port/Enhanced Parallel Slave Port with 16 Address Lines
- Dual Analog Comparators with Input Multiplexing

Peripheral Highlights (continued):

- 10-Bit, up to 12-Channel Analog-to-Digital (A/D) Converter module:
  - Auto-acquisition capability
  - Conversion available during Sleep
- Two Enhanced USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect

External Memory Bus (80-pin devices only):

- Address Capability of up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 12-Bit, 16-Bit and 20-Bit Addressing modes

Special Microcontroller Features:

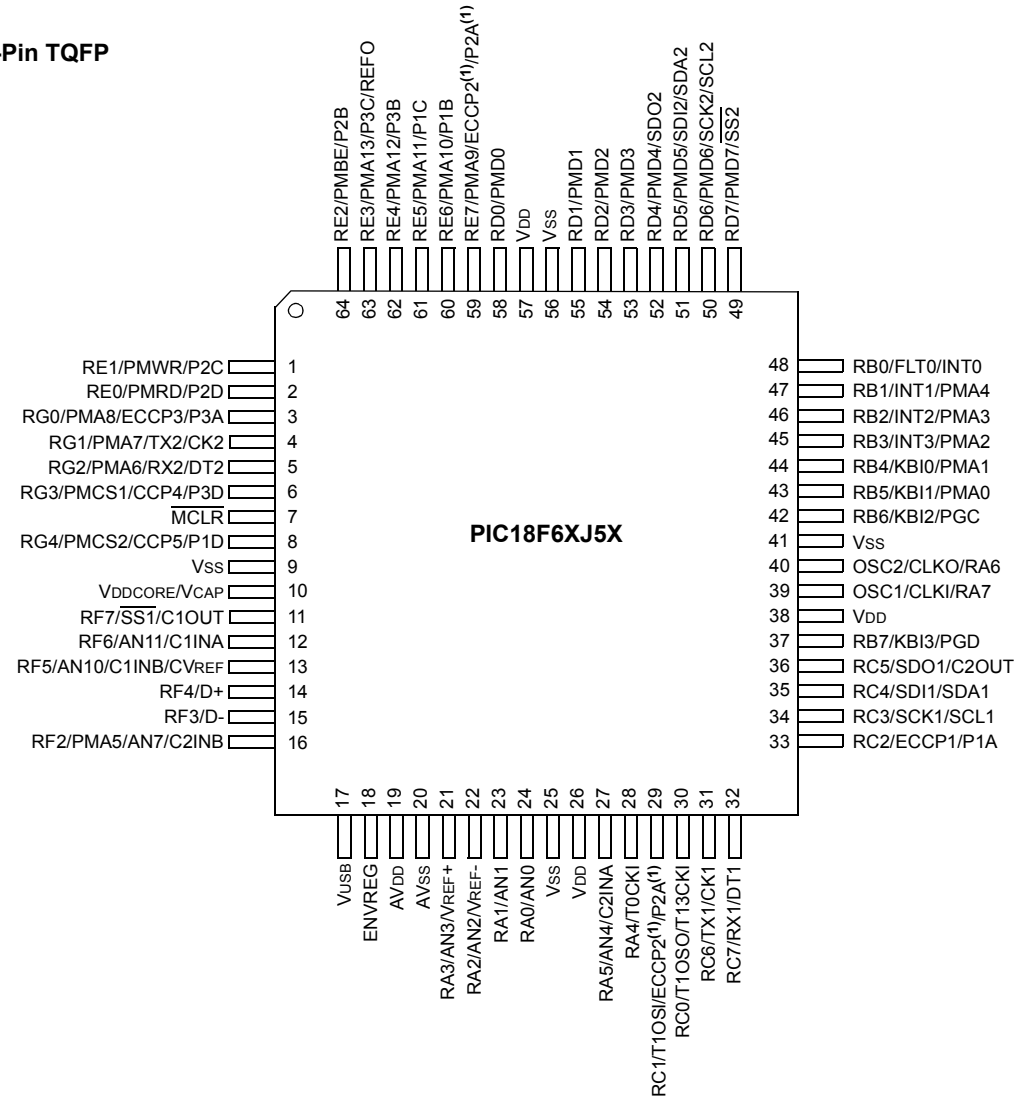
- 5.5V Tolerant Inputs (digital-only pins)
- Low-Power, High-Speed CMOS Flash Technology
- C Compiler Optimized Architecture for Re-Entrant Code
- Power Management Features:
  - Run: CPU on, peripherals on
  - Idle: CPU off, peripherals on
  - Sleep: CPU off, peripherals off
- Priority Levels for Interrupts
- Self-Programmable under Software Control
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with 3 Breakpoints via Two Pins
- Operating Voltage Range of 2.0V to 3.6V
- On-Chip 2.5V Regulator
- Flash Program Memory of 10000 Erase/Write Cycles and 20-Year Data Retention

Device	Flash Program Memory (bytes)	SRAM Data Memory (bytes)	I/O	10-Bit A/D (ch)	CCP/ ECCP (PWM)	MSSP			EUSART	Comparators	Timers 8/16-Bit	External Bus	PMP/PSP
							SPI	Master I^2C™					
PIC18F65J50	32K	3904*	49	8	2/3	2	Y	Y	2	2	2/3	N	Y
PIC18F66J50	64K	3904*	49	8	2/3	2	Y	Y	2	2	2/3	N	Y
PIC18F66J55	96K	3904*	49	8	2/3	2	Y	Y	2	2	2/3	N	Y
PIC18F67J50	128K	3904*	49	8	2/3	2	Y	Y	2	2	2/3	N	Y
PIC18F85J50	32K	3904*	65	12	2/3	2	Y	Y	2	2	2/3	Y	Y
PIC18F86J50	64K	3904*	65	12	2/3	2	Y	Y	2	2	2/3	Y	Y
PIC18F86J55	96K	3904*	65	12	2/3	2	Y	Y	2	2	2/3	Y	Y
PIC18F87J50	128K	3904*	65	12	2/3	2	Y	Y	2	2	2/3	Y	Y

* Includes the dual access RAM used by the USB module which is shared with data memory.

Pin Diagrams

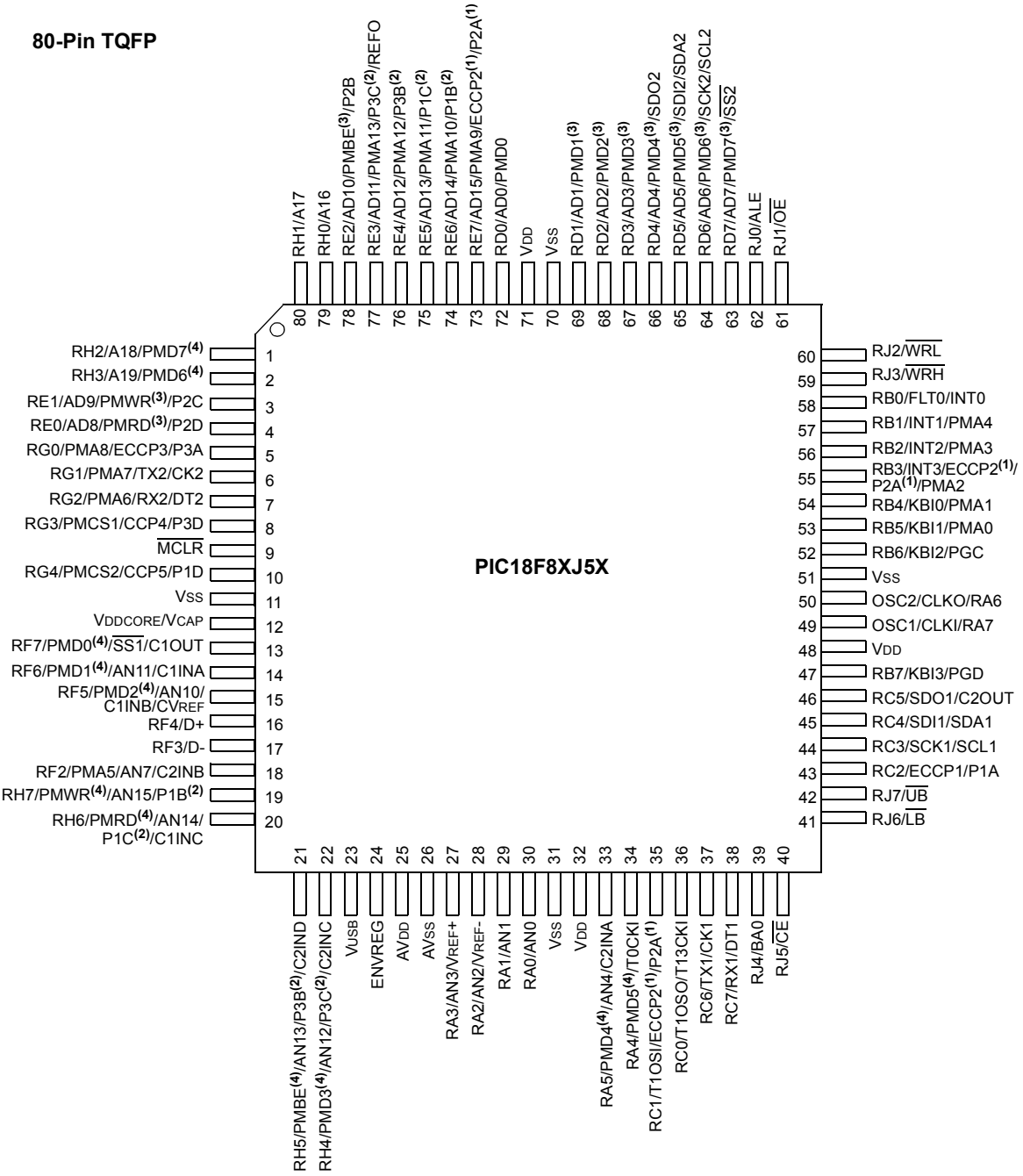
64-Pin TQFP



Note 1: The ECCP2/P2A pin placement depends on the setting of the CCP2MX Configuration bit.

Pin Diagrams (Continued)

80-Pin TQFP



Note 1: The ECCP2/P2A pin placement depends on the setting of the CCP2MX Configuration bit and the program memory mode.

2: P1B, P1C, P3B and P3C pin placement depends on the setting of the ECCPMX Configuration bit.

3: PMP pin placement when PMPMX = 1.

4: PMP pin placement when PMPMX = 0.

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F65J50
- PIC18F66J50
- PIC18F66J55
- PIC18F67J50
- PIC18F85J50
- PIC18F86J50
- PIC18F86J55
- PIC18F87J50

This family introduces a new line of low-voltage USB microcontrollers with the main traditional advantage of all PIC18 microcontrollers – namely, high computational performance and a rich feature set – at an extremely competitive price point. These features make the PIC18F87J10 family a logical choice for many high-performance applications, where cost is a primary consideration.

1.1 Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F87J10 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal RC oscillator, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.

1.1.2 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F87J10 family incorporate a fully-featured Universal Serial Bus communications module with a built-in transceiver that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full-speed communication for all supported data transfer types.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F87J10 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of a divide-by-4 clock output.
- An internal oscillator block which provides an 8 MHz clock and an INTRC source (approximately 31 kHz, stable over temperature and V_{DD}), as well as a range of 6 user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of 8 clock frequencies. This option frees an oscillator pin for use as an additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to the high-speed crystal, external oscillator and internal oscillator, providing a clock speed up to 48 MHz.
- Dual clock operation, allowing the USB module to run from a high-frequency oscillator while the rest of the microcontroller is clocked at a different frequency.

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.1.4 EXPANDED MEMORY

The PIC18F87J10 family provides ample room for application code, from 32 Kbytes to 128 Kbytes of code space. The Flash cells for program memory are rated to last in excess of 10000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 20 years.

The Flash program memory is readable and writable during normal operation. The PIC18F87J10 family also provides plenty of room for dynamic application data with up to 3904 bytes of data RAM.

1.1.5 EXTERNAL MEMORY BUS

In the event that 128 Kbytes of memory are inadequate for an application, the 80-pin members of the PIC18F87J10 family also implement an External Memory Bus (EMB). This allows the controller's internal program counter to address a memory space of up to 2 Mbytes, permitting a level of data access that few 8-bit devices can claim. This allows additional memory options, including:

- Using combinations of on-chip and external memory up to the 2-Mbyte limit
- Using external Flash memory for reprogrammable application code or large data tables
- Using external RAM devices for storing large amounts of variable data

1.1.6 EXTENDED INSTRUCTION SET

The PIC18F87J10 family implements the optional extension to the PIC18 instruction set, adding 8 new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as 'C'.

1.1.7 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 80-pin members, or even jumping from 64-pin to 80-pin devices.

The PIC18F87J10 family is also pin compatible with other PIC18 families, such as the PIC18F87J10, PIC18F87J11, PIC18F8720 and PIC18F8722. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining the same feature set.

1.2 Other Special Features

- **Communications:** The PIC18F87J10 family incorporates a range of serial and parallel communication peripherals, including a fully featured Universal Serial Bus communications module that is compliant with the USB Specification Revision 2.0. This device also includes 2 independent Enhanced USARTs and 2 Master SSP modules, capable of both SPI and I2C™ (Master and Slave) modes of operation. The device also has a parallel port and can be configured to serve as either a Parallel Master Port or as a Parallel Slave Port.
- **CCP Modules:** All devices in the family incorporate two Capture/Compare/PWM (CCP) modules and three Enhanced CCP modules to maximize flexibility in control applications. Up to four different time bases may be used to perform several different operations at once. Each of the three ECCPs offers up to four PWM outputs, allowing for a total of 12 PWMs. The ECCPs also offer many beneficial features, including polarity selection, programmable dead time, auto-shutdown and restart and Half-Bridge and Full-Bridge Output modes.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and thus, reducing code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 28.0 "Electrical Characteristics"** for time-out periods.

1.3 Details on Individual Family Members

Devices in the PIC18F87J10 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2. The devices are differentiated from each other in two ways:

1. Flash program memory (six sizes, ranging from 32 Kbytes for PIC18FX5J50 devices to 128 Kbytes for PIC18FX7J50).
2. I/O ports (7 bidirectional ports on 64-pin devices, 9 bidirectional ports on 80-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

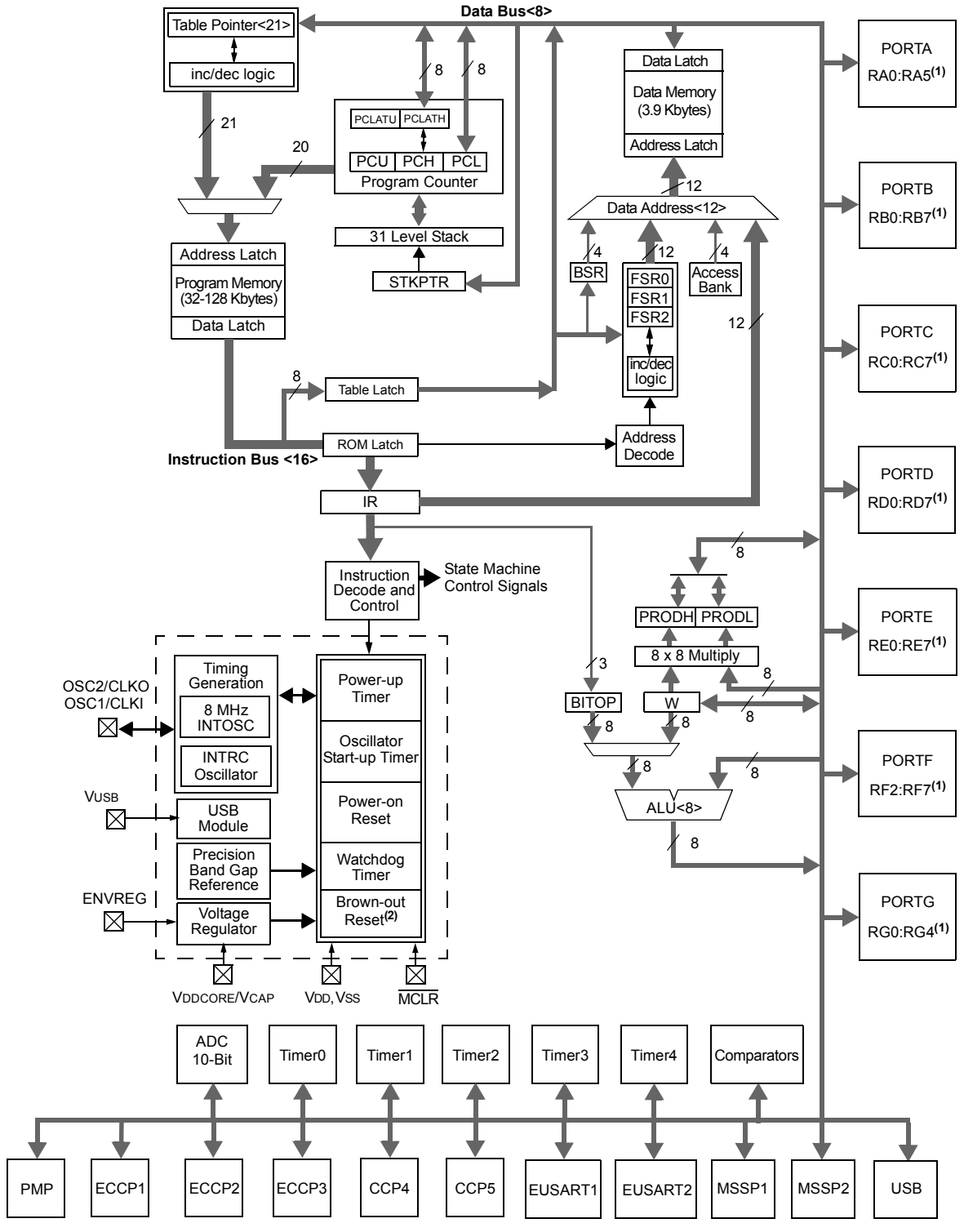
TABLE 1-1: DEVICE FEATURES FOR THE PIC18F6XJ5X (64-PIN DEVICES)

Features	PIC18F65J50	PIC18F66J50	PIC18F66J55	PIC18F67J50
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	32K	64K	96K	128K
Program Memory (Instructions)	16384	32768	49152	65536
Data Memory (Bytes)	3904	3904	3904	3904
Interrupt Sources	30			
I/O Ports	Ports A, B, C, D, E, F, G			
Timers	5			
Capture/Compare/PWM Modules	2			
Enhanced Capture/ Compare/PWM Modules	3			
Serial Communications	MSSP (2), Enhanced USART (2), USB			
Parallel Communications (PMP)	Yes			
10-Bit Analog-to-Digital Module	8 Input Channels			
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)			
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled			
Packages	64-Pin TQFP			

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F8XJ5X (80-PIN DEVICES)

Features	PIC18F85J50	PIC18F86J50	PIC18F86J55	PIC18F87J50
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	32K	64K	96K	128K
Program Memory (Instructions)	16384	32768	49152	65536
Data Memory (Bytes)	3904	3904	3904	3904
Interrupt Sources	30			
I/O Ports	Ports A, B, C, D, E, F, G, H, J			
Timers	5			
Capture/Compare/PWM Modules	2			
Enhanced Capture/ Compare/PWM Modules	3			
Serial Communications	MSSP (2), Enhanced USART (2), USB			
Parallel Communications (PMP)	Yes			
10-Bit Analog-to-Digital Module	12 Input Channels			
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)			
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled			
Packages	80-Pin TQFP			

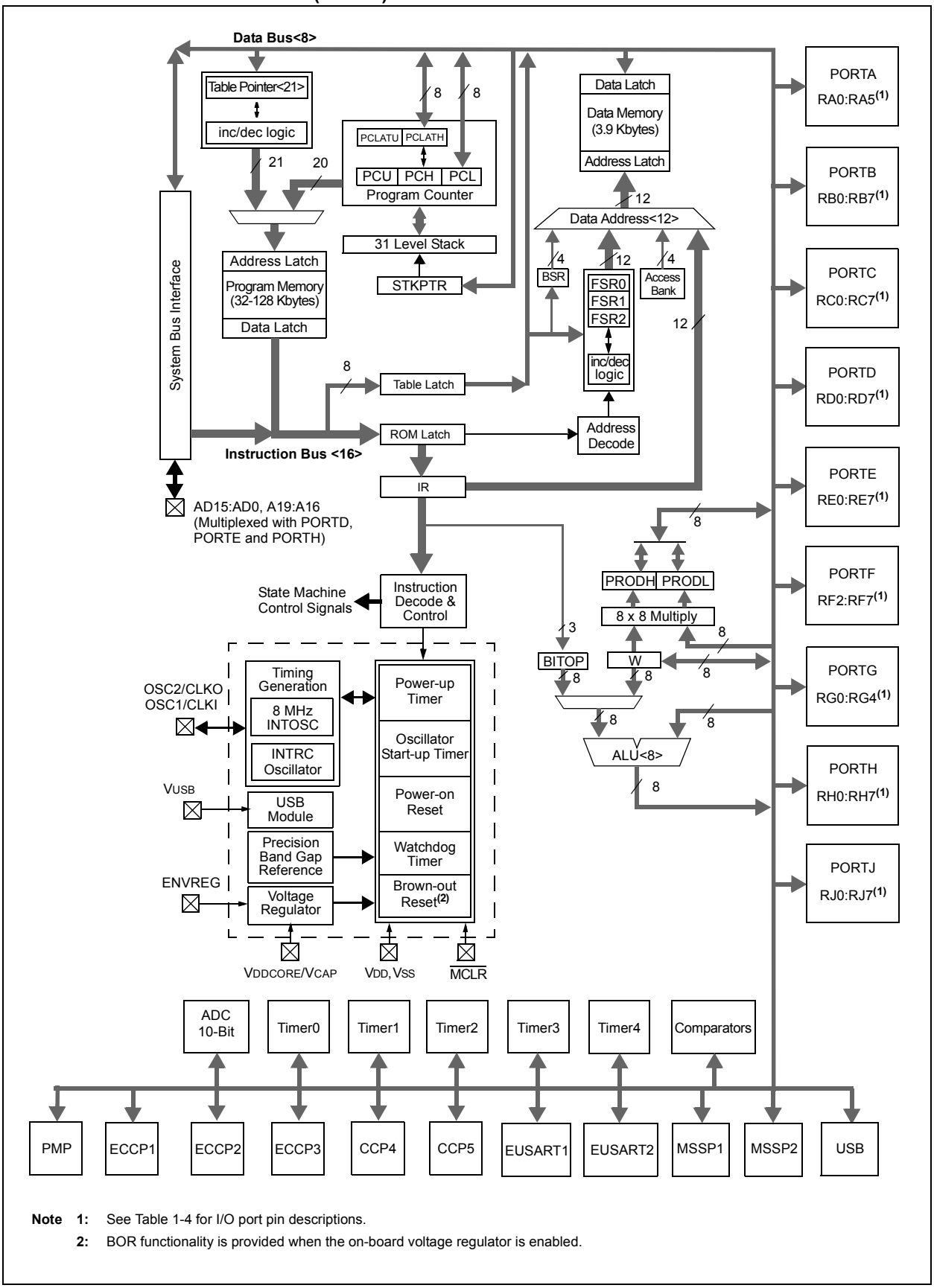
FIGURE 1-1: PIC18F6XJ5X (64-PIN) BLOCK DIAGRAM



Note 1: See Table 1-3 for I/O port pin descriptions.

2: BOR functionality is provided when the on-board voltage regulator is enabled.

FIGURE 1-2: PIC18F8XJ5X (80-PIN) BLOCK DIAGRAM



Note 1: See Table 1-4 for I/O port pin descriptions.

2: BOR functionality is provided when the on-board voltage regulator is enabled.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
$\overline{MCLR}$	7	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OSC1/CLKI/RA7	39			Oscillator crystal or external clock input.
OSC1		I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise.
CLKI		I	CMOS	Main oscillator input connection. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7(3)		I/O	TTL	Main clock input connection. General purpose I/O pin.
OSC2/CLKO/RA6	40			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	Main oscillator feedback output connection. In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6(3)		I/O	TTL	System cycle clock output (FOSC/4). General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTA is a bidirectional I/O port.
RA0/AN0	24			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	23			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/VREF-	22			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
RA3/AN3/VREF+	21			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI	28			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
RA5/AN4/C2INA	27			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
C2INA		—	Analog	Comparator 2 input A
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.
RA7	—	—	—	See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/FLT0/INT0	48			
RB0		I/O	TTL	Digital I/O.
FLT0		I	ST	ECCP1/2/3 Fault input.
INT0		I	ST	External interrupt 0.
RB1/INT1/PMA4	47			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
PMA4		O	—	Parallel Master Port address.
RB2/INT2/PMA3	46			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
PMA3		O	—	Parallel Master Port address.
RB3/INT3/PMA2	45			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External interrupt 3.
PMA2		O	—	Parallel Master Port address.
RB4/KBI0/PMA1	44			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
PMA1		I/O	—	Parallel Master Port address.
RB5/KBI1/PMA0	43			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PMA0		I/O	—	Parallel Master Port address.
RB6/KBI2/PGC	42			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	37			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	30			
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/ECCP2/P2A	29			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
ECCP2(1)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A(1)		O	—	ECCP2 PWM output A.
RC2/ECCP1/P1A	33			
RC2		I/O	ST	Digital I/O.
ECCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A		O	—	ECCP1 PWM output A.
RC3/SCK1/SCL1	34			
RC3		I/O	ST	Digital I/O.
SCK1		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL1		I/O	ST	Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI1/SDA1	35			
RC4		I/O	ST	Digital I/O.
SDI1		I	ST	SPI data in.
SDA1		I/O	ST	I^2C data I/O.
RC5/SDO1/C2OUT	36			
RC5		I/O	ST	Digital I/O.
SDO1		O	—	SPI data out.
C2OUT		O	TTL	Comparator 2 output.
RC6/TX1/CK1	31			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	32			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTD is a bidirectional I/O port.
RD0/PMD0	58			
RD0		I/O	ST	Digital I/O.
PMD0		I/O	TTL	Parallel Master Port data.
RD1/PMD1	55			
RD1		I/O	ST	Digital I/O.
PMD1		I/O	TTL	Parallel Master Port data.
RD2/PMD2	54			
RD2		I/O	ST	Digital I/O.
PMD2		I/O	TTL	Parallel Master Port data.
RD3/PMD3	53			
RD3		I/O	ST	Digital I/O.
PMD3		I/O	TTL	Parallel Master Port data.
RD4/PMD4/SDO2	52			
RD4		I/O	ST	Digital I/O.
PMD4		I/O	TTL	Parallel Master Port data.
SDO2		O	—	SPI data out.
RD5/PMD5/SDI2/SDA2	51			
RD5		I/O	ST	Digital I/O.
PMD5		I/O	TTL	Parallel Master Port data.
SDI2		I	ST	SPI data in.
SDA2		I/O	ST	I^2C™ data I/O.
RD6/PMD6/SCK2/SCL2	50			
RD6		I/O	ST	Digital I/O.
PMD6		I/O	TTL	Parallel Master Port data.
SCK2		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL2		I/O	ST	Synchronous serial clock input/output for I^2C mode.
RD7/PMD7/$\overline{SS2}$	49			
RD7		I/O	ST	Digital I/O.
PMD7		I/O	TTL	Parallel Master Port data.
$\overline{SS2}$		I	TTL	SPI slave select input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTE is a bidirectional I/O port.
RE0/PMRD/P2D	2			
RE0		I/O	ST	Digital I/O.
PMRD		I/O	—	Parallel Master Port read strobe.
P2D		O	—	ECCP2 PWM output D.
RE1/PMWR/P2C	1			
RE1		I/O	ST	Digital I/O.
PMWR		I/O	—	Parallel Master Port write strobe.
P2C		O	—	ECCP2 PWM output C.
RE2/PMBE/P2B	64			
RE2		I/O	ST	Digital I/O.
PMBE		O	—	Parallel Master Port byte enable
P2B		O	—	ECCP2 PWM output B.
RE3/PMA13/P3C/REFO	63			
RE3		I/O	ST	Digital I/O.
PMA13		O	—	Parallel Master Port address.
P3C		O	—	ECCP3 PWM output C.
REFO		O	—	Reference clock out.
RE4/PMA12/P3B	62			
RE4		I/O	ST	Digital I/O.
PMA12		O	—	Parallel Master Port address.
P3B		O	—	ECCP3 PWM output B.
RE5/PMA11/P1C	61			
RE5		I/O	ST	Digital I/O.
PMA11		O	—	Parallel Master Port address.
P1C		O	—	ECCP1 PWM output C.
RE6/PMA10/P1B	60			
RE6		I/O	ST	Digital I/O.
PMA10		O	—	Parallel Master Port address.
P1B		O	—	ECCP1 PWM output B.
RE7/PMA9/ECCP2/P2A	59			
RE7		I/O	ST	Digital I/O.
PMA9		O	—	Parallel Master Port address.
ECCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A(2)		O	—	ECCP2 PWM output A.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTF is a bidirectional I/O port.
RF2/PMA5/AN7/C2INB	16			
RF2		I/O	ST	Digital I/O.
PMA5		O	—	Parallel Master Port address.
AN7		I	Analog	Analog input 7.
C2INB		I	Analog	Comparator 2 input B.
RF3/D-	15			
RF3		I	ST	Digital input.
D-		I/O	—	USB differential minus line (input/output).
RF4/D+	14			
RF4		I	ST	Digital input.
D+		I/O	—	USB differential plus line (input/output).
RF5/AN10/C1INB/CVREF	13			
RF5		I	ST	Digital input.
AN10		I	Analog	Analog input 10.
C1INB		I	Analog	Comparator 1 input B.
CVREF		O	Analog	Comparator reference voltage output.
RF6/AN11/C1INA	12			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog input 11.
C1INA		I	Analog	Comparator 1 input A.
RF7/$\overline{SS1}$/C1OUT	11			
RF7		I/O	ST	Digital I/O.
$\overline{SS1}$		I	TTL	SPI slave select input.
C1OUT		O	TTL	Comparator 1 output.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTG is a bidirectional I/O port.
RG0/PMA8/ECCP3/P3A	3			
RG0		I/O	ST	Digital I/O.
PMA8		O	—	Parallel Master Port address.
ECCP3		I/O	—	Capture 3 input/Compare 3 output/PWM3 output.
P3A		O	—	ECCP3 PWM output A.
RG1/PMA7/TX2/CK2	4			
RG1		I/O	ST	Digital I/O.
PMA7		O	—	Parallel Master Port address.
TX2		O	—	EUSART2 asynchronous transmit.
CK2		I/O	ST	EUSART2 synchronous clock (see related RX2/DT2).
RG2/PMA6/RX2/DT2	5			
RG2		I/O	ST	Digital I/O.
PMA6		O	—	Parallel Master Port address.
RX2		I	ST	EUSART2 asynchronous receive.
DT2		I/O	ST	EUSART2 synchronous data (see related TX2/CK2).
RG3/PMCS1/CCP4/P3D	6			
RG3		I/O	ST	Digital I/O.
PMCS1		O	—	Parallel Master Port chip select 1.
CCP4		I/O	ST	Capture 4 input/Compare 4 output/PWM4 output.
P3D		O	—	ECCP3 PWM output D.
RG4/PMCS2/CCP5/P1D	8			
RG4		I/O	ST	Digital I/O.
PMCS2		O	—	Parallel Master Port chip select 2.
CCP5		I/O	ST	Capture 5 input/Compare 5 output/PWM5 output.
P1D		O	—	ECCP1 PWM output D.
VSS	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	26, 38, 57	P	—	Positive supply for peripheral digital logic and I/O pins.
AVSS	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.
ENVREG	18	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP	10			Core logic power or external filter capacitor connection.
VDDCORE		P	—	Positive supply for microcontroller core logic (regulator disabled).
VCAP		P	—	External filter capacitor connection (regulator enabled).
VUSB	17	P	—	USB voltage input pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-4: PIC18F8XJ5X PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	80-TQFP			
$\overline{MCLR}$	9	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OSC1/CLKI/RA7	49			Oscillator crystal or external clock input.
OSC1		I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise.
CLKI		I	CMOS	Main oscillator input connection. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7(8)		I/O	TTL	Main clock input connection. General purpose I/O pin.
OSC2/CLKO/RA6	50			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	Main oscillator feedback output connection. In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6(8)		I/O	TTL	System cycle clock output (FOSC/4). General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (Extended Microcontroller mode).

2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

4: Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

6: Pin placement when PMPMX = 1.

7: Pin placement when PMPMX = 0.

8: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-4: PIC18F8XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	80-TQFP			
				PORTA is a bidirectional I/O port.
RA0/AN0	30			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	29			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/VREF-	28			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
RA3/AN3/VREF+	27			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/PMD5/T0CKI	34			
RA4		I/O	ST	Digital I/O.
PMD5(7)		I/O	TTL	Parallel Master Port data.
T0CKI		I	ST	Timer0 external clock input.
RA5/PMD4/AN4/C2INA	33			
RA5		I/O	TTL	Digital I/O.
PMD4(7)		I/O	TTL	Parallel Master Port data.
AN4		I	Analog	Analog input 4.
C2INA		I	Analog	Comparator 2 input A.
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.
RA7	—	—	—	See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (Extended Microcontroller mode).

2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

4: Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

6: Pin placement when PMPMX = 1.

7: Pin placement when PMPMX = 0.

8: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-4: PIC18F8XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	80-TQFP			
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/FLT0/INT0	58			
RB0		I/O	TTL	Digital I/O.
FLT0		I	ST	ECCP1/2/3 Fault input.
INT0		I	ST	External interrupt 0.
RB1/INT1/PMA4	57			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
PMA4		O	—	Parallel Master Port address.
RB2/INT2/PMA3	56			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
PMA3		O	—	Parallel Master Port address.
RB3/INT3/ECCP2/ P2A/PMA2	55			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External interrupt 3.
ECCP2(1)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A(1)		O	—	ECCP2 PWM output A.
PMA2		O	—	Parallel Master Port address.
RB4/KBI0/PMA1	54			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
PMA1		I/O	—	Parallel Master Port address.
RB5/KBI1/PMA0	53			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PMA0		I/O	—	Parallel Master Port address.
RB6/KBI2/PGC	52			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	47			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (Extended Microcontroller mode).

2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

4: Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

6: Pin placement when PMPMX = 1.

7: Pin placement when PMPMX = 0.

8: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-4: PIC18F8XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	80-TQFP			
				PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	36			
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/ECCP2/P2A	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
ECCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A(2)		O	—	ECCP2 PWM output A.
RC2/ECCP1/P1A	43			
RC2		I/O	ST	Digital I/O.
ECCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A		O	—	ECCP1 PWM output A.
RC3/SCK1/SCL1	44			
RC3		I/O	ST	Digital I/O.
SCK1		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL1		I/O	ST	Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI1/SDA1	45			
RC4		I/O	ST	Digital I/O.
SDI1		I	ST	SPI data in.
SDA1		I/O	ST	I^2C data I/O.
RC5/SDO1/C2OUT	46			
RC5		I/O	ST	Digital I/O.
SDO1		O	—	SPI data out.
C2OUT		O	TTL	Comparator 2 output.
RC6/TX1/CK1	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (Extended Microcontroller mode).

2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

4: Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

6: Pin placement when PMPMX = 1.

7: Pin placement when PMPMX = 0.

8: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.