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PIC18CXX8

High-Performance Microcontrollers with CAN Module

High Performance RISC CPU:

- C-compiler optimized architecture instruction set
- Linear program memory addressing to 32 Kbytes
- Linear data memory addressing to 4 Kbytes

Device	Program Memory			On-Chip RAM (bytes)
	On-Chip		Off-Chip	
	EPROM (bytes)	# Single Word Instructions	Maximum Addressing (bytes)	
PIC18C658	32 K	16384	N/A	1536
PIC18C858	32 K	16384	N/A	1536

- Up to 10 MIPS operation:
  - DC - 40 MHz clock input
  - 4 MHz - 10 MHz osc./clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 8 x 8 Single Cycle Hardware Multiplier

Peripheral Features:

- High current sink/source 25 mA/25 mA
- Up to 76 I/O with individual direction control
- Four external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter with 8-bit programmable prescaler
- Timer1 module: 16-bit timer/counter
- Timer2 module: 8-bit timer/counter with 8-bit period register (time base for PWM)
- Timer3 module: 16-bit timer/counter
- Secondary oscillator clock option - Timer1/Timer3
- Two Capture/Compare/PWM (CCP) modules
  CCP pins can be configured as:
  - Capture input: 16-bit, max resolution 6.25 ns
  - Compare is 16-bit, max resolution 100 ns (TCY)
  - PWM output: PWM resolution is 1- to 10-bit.
    Max. PWM freq. @:8-bit resolution = 156 kHz
    10-bit resolution = 39 kHz
- Master Synchronous Serial Port (MSSP) with two modes of operation:
  - 3-wire SPI™ (Supports all 4 SPI modes)
  - I^2C™ Master and Slave mode
- Addressable USART module: Supports Interrupt on Address bit

Advanced Analog Features:

- 10-bit Analog-to-Digital Converter module (A/D) with:
  - Fast sampling rate
  - Conversion available during SLEEP
  - DNL = ±1 LSb, INL = ±1 LSb
  - Up to 16 channels available
- Analog Comparator Module:
  - 2 Comparators
  - Programmable input and output multiplexing
- Comparator Voltage Reference Module
- Programmable Low Voltage Detection (LVD) module
  - Supports interrupt on low voltage detection
- Programmable Brown-out Reset (BOR)

CAN BUS Module Features:

- Message bit rates up to 1 Mbps
- Conforms to CAN 2.0B ACTIVE Spec with:
  - 29-bit Identifier Fields
  - 8 byte message length
- 3 Transmit Message Buffers with prioritization
- 2 Receive Message Buffers
- 6 full 29-bit Acceptance Filters
- Prioritization of Acceptance Filters
- Multiple Receive Buffers for High Priority Messages to prevent loss due to overflow
- Advanced Error Management Features

Special Microcontroller Features:

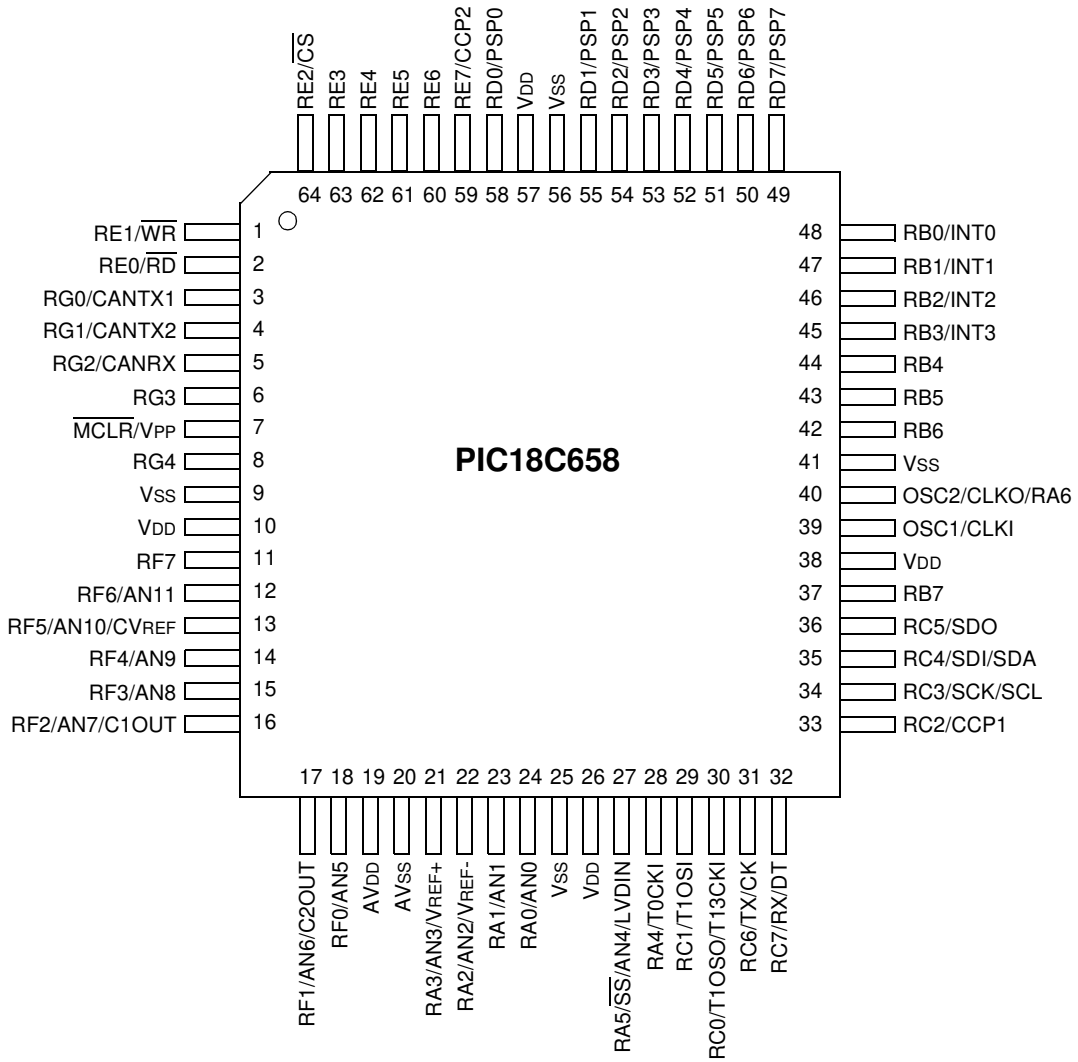
- Power-on Reset (POR), Power-up Timer (PWRT), and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options, including:
  - 4X Phase Lock Loop (of primary oscillator)
  - Secondary Oscillator (32 kHz) clock input
- In-Circuit Serial Programming (ICSP™) via two pins

CMOS Technology:

- Low power, high speed EPROM technology
- Fully static design
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and Extended temperature ranges
- Low power consumption

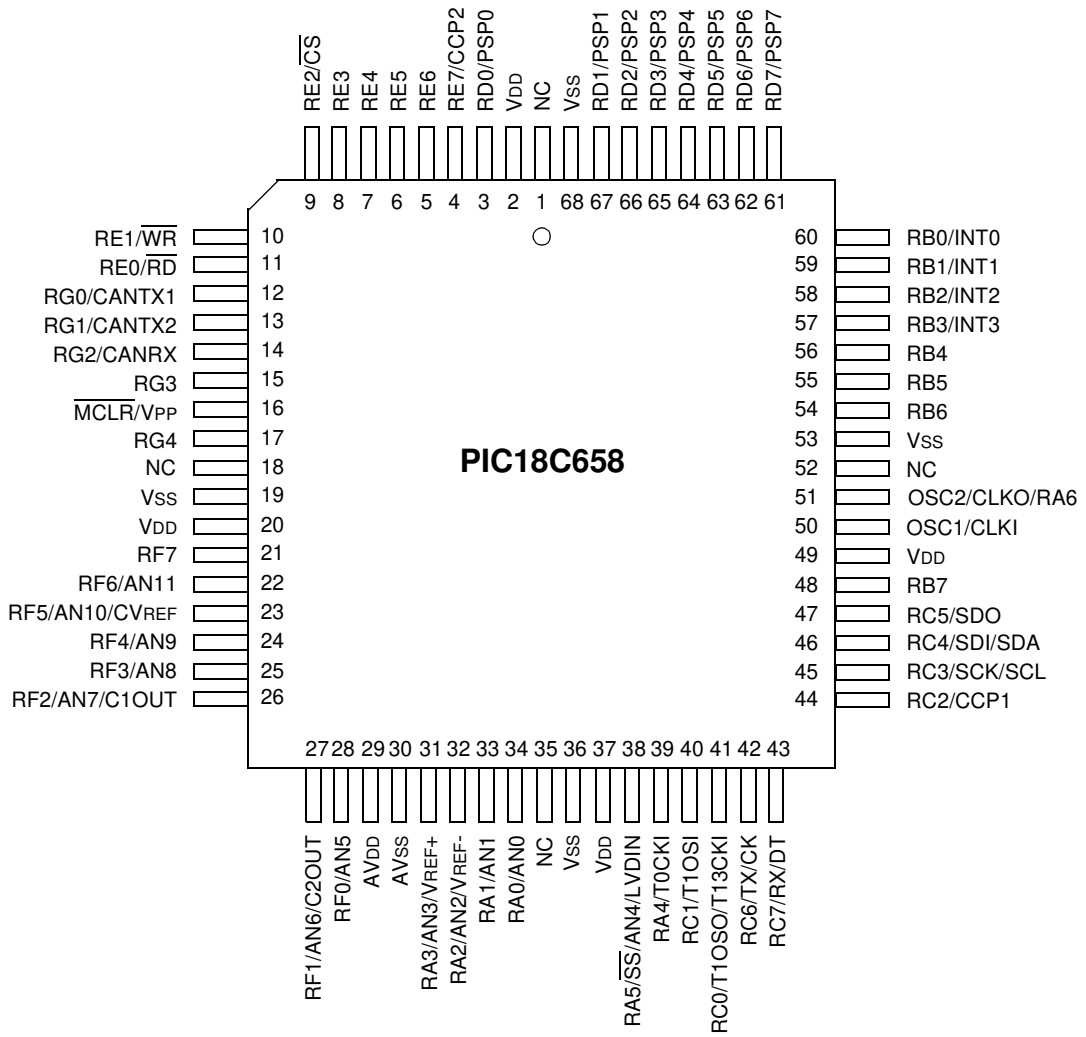
Pin Diagrams

64-Pin TQFP



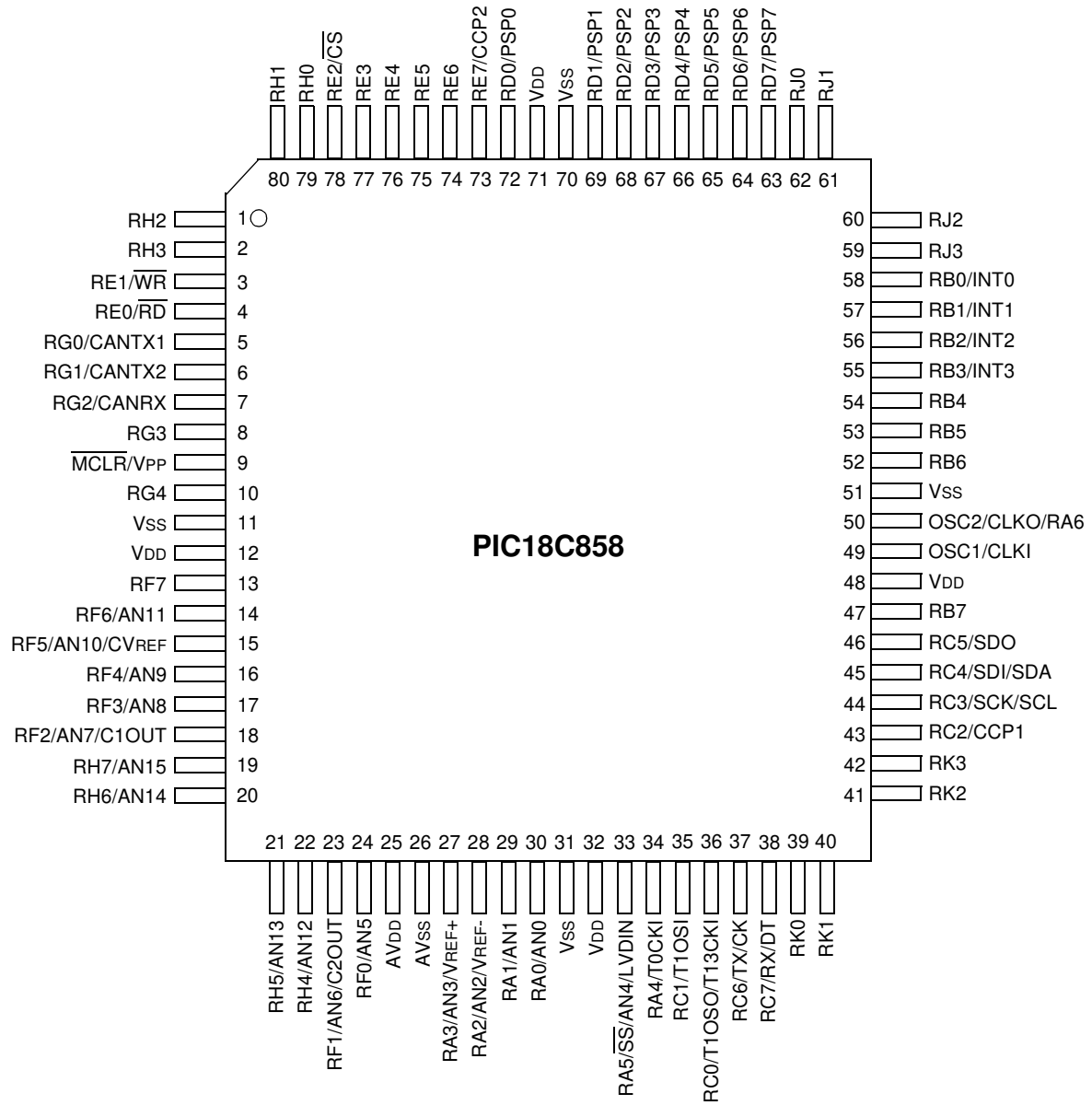
Pin Diagrams (Cont.'d)

68-Pin PLCC



Pin Diagrams (Cont.'d)

80-Pin TQFP



Pin Diagrams (Cont.'d)

84-Pin PLCC

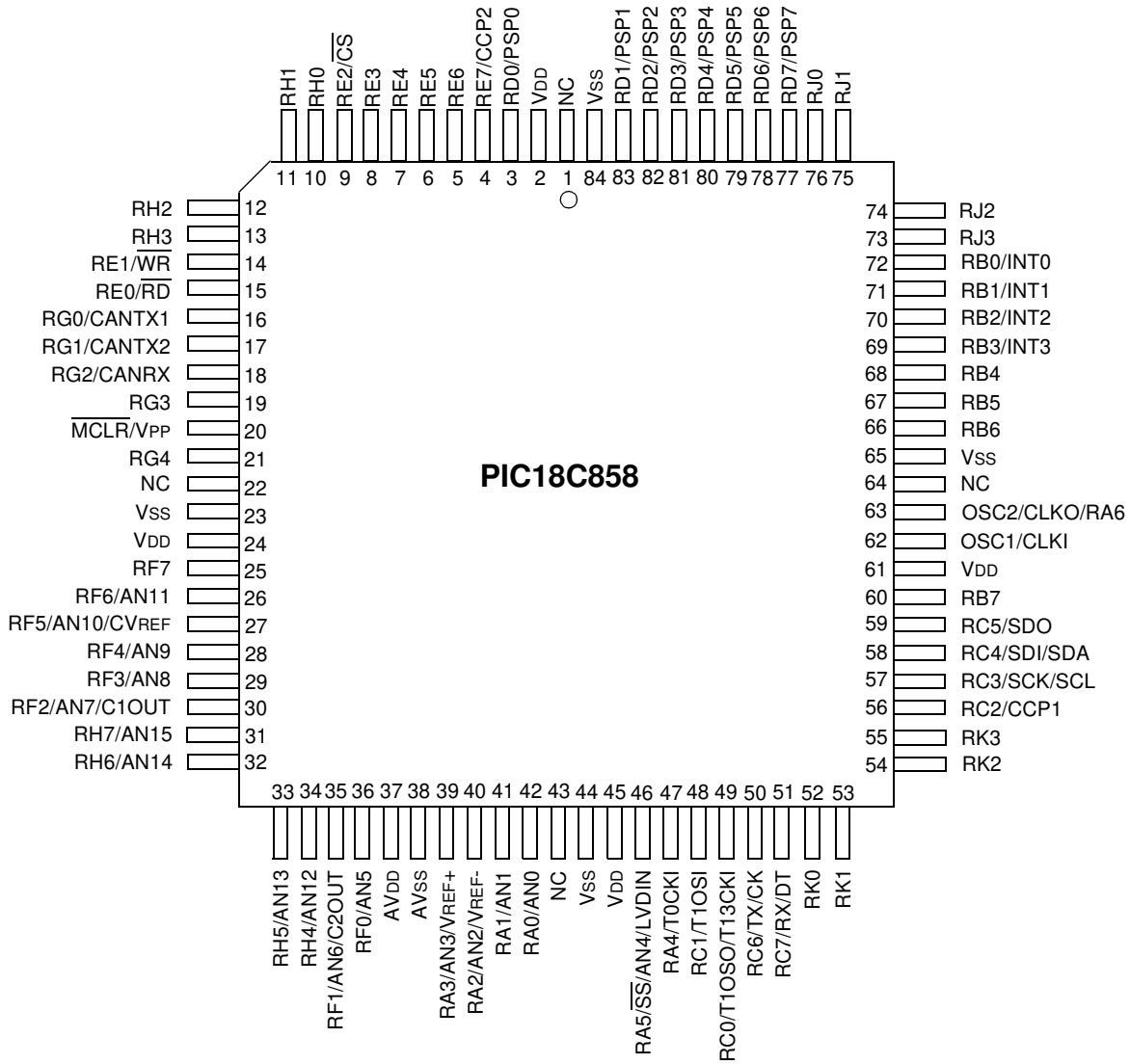


Table of Contents

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device specific information for the following three devices:

1. PIC18C658
2. PIC18C858

The PIC18C658 is available in 64-pin TQFP and 68-pin PLCC packages. The PIC18C858 is available in 80-pin TQFP and 84-pin PLCC packages.

An overview of features is shown in Table 1-1.

The following two figures are device block diagrams sorted by pin count; 64/68-pin for Figure 1-1 and 80/84-pin for Figure 1-2. The 64/68-pin and 80/84-pin pinouts are listed in Table 1-2.

TABLE 1-1: DEVICE FEATURES

Features			PIC18C658	PIC18C858
Operating Frequency			DC - 40 MHz	DC - 40 MHz
Program Memory	Internal	Bytes	32 K	32 K
		# of Single word Instructions	16384	16384
Data Memory (Bytes)			1536	1536
Interrupt sources			21	21
I/O Ports			Ports A – G	Ports A – H, J, K
Timers			4	4
Capture/Compare/PWM modules			2	2
Serial Communications			MSSP, CAN Addressable USART	MSSP, CAN Addressable USART
Parallel Communications			PSP	PSP
10-bit Analog-to-Digital Module			12 input channels	16 input channels
Analog Comparators			2	2
RESETS (and Delays)			POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)
Programmable Low Voltage Detect			Yes	Yes
Programmable Brown-out Reset			Yes	Yes
CAN Module			Yes	Yes
In-Circuit Serial Programming (ICSP™)			Yes	Yes
Instruction Set			75 Instructions	75 Instructions
Packages			64-pin TQFP 68-pin CERQUAD (Windowed) 68-pin PLCC	80-pin TQFP 84-pin CERQUAD (Windowed) 84-pin PLCC

FIGURE 1-1: PIC18C658 BLOCK DIAGRAM

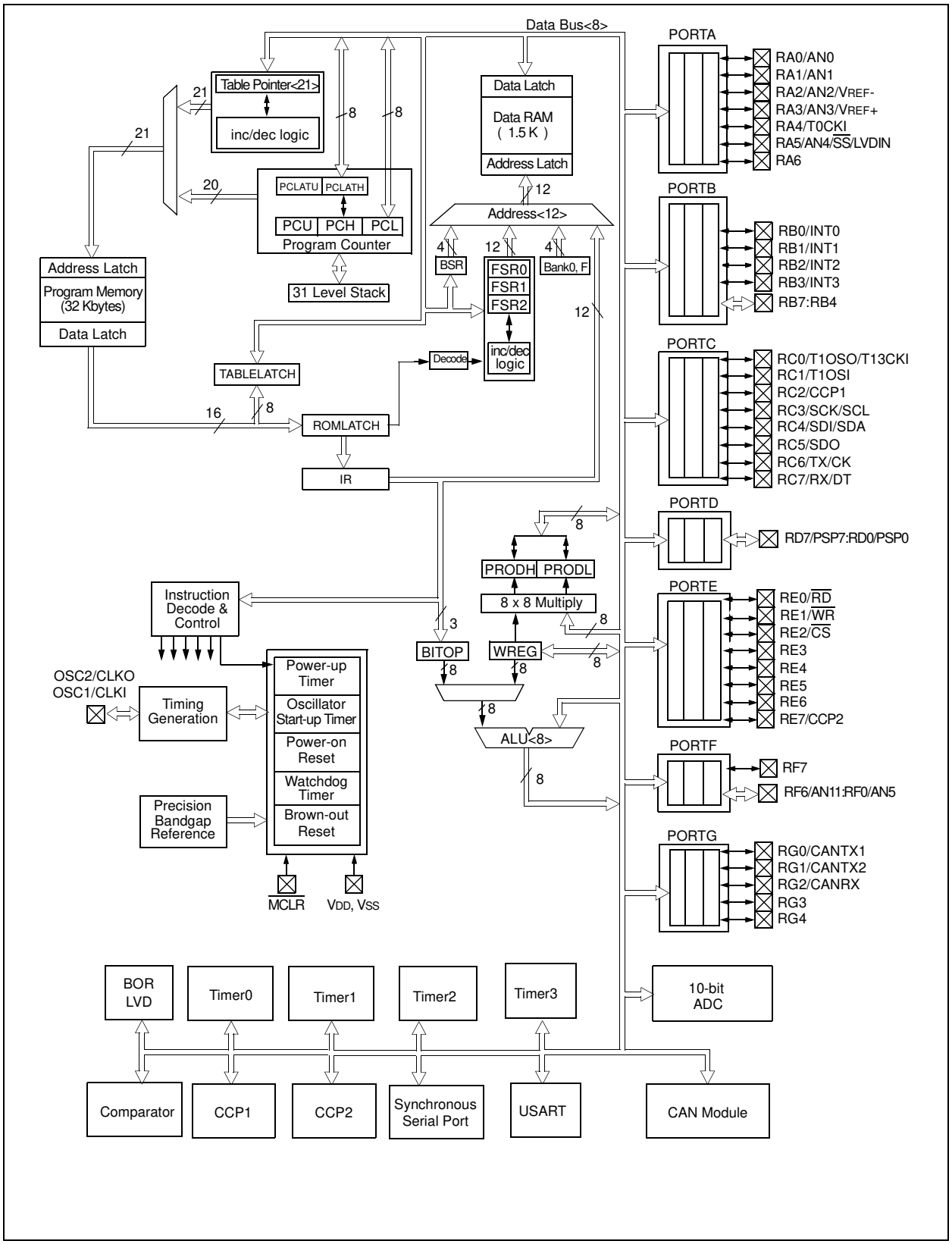


FIGURE 1-2: PIC18C858 BLOCK DIAGRAM

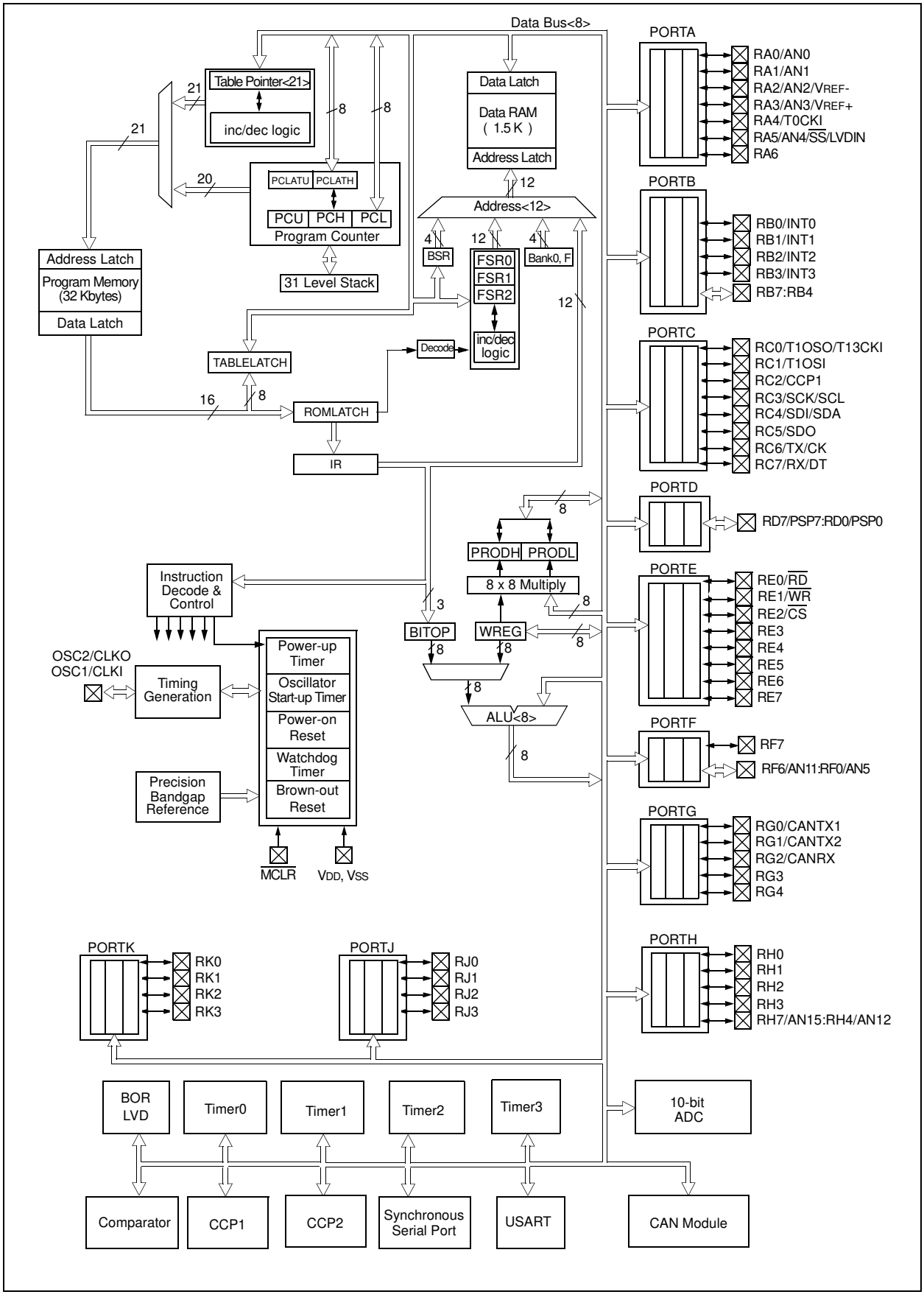


TABLE 1-2: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
$\overline{MCLR}$/VPP	7	16	9	20			
$\overline{MCLR}$					I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
VPP					P		Programming voltage input
NC	—	1, 18, 35, 52	—	1, 22, 43, 64	—	—	These pins should be left unconnected
OSC1/CLKI	39	50	49	62			
OSC1					I	CMOS/ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
CLKI					I	CMOS	External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO/RA6	40	51	50	63			
OSC2					O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO					O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate
RA6					I/O	TTL	General purpose I/O pin

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTA is a bi-directional I/O port
RA0/AN0	24	34	30	42			
RA0					I/O	TTL	Digital I/O
AN0					I	Analog	Analog input 0
RA1/AN1	23	33	29	41			
RA1					I/O	TTL	Digital I/O
AN1					I	Analog	Analog input 1
RA2/AN2/VREF-	22	32	28	40			
RA2					I/O	TTL	Digital I/O
AN2					I	Analog	Analog input 2
VREF-					I	Analog	A/D reference voltage (Low) input
RA3/AN3/VREF+	21	31	27	39			
RA3					I/O	TTL	Digital I/O
AN3					I	Analog	Analog input 3
VREF+					I	Analog	A/D reference voltage (High) input
RA4/T0CKI	28	39	34	47			
RA4					I/O	ST/OD	Digital I/O – Open drain when configured as output
T0CKI					I	ST	Timer0 external clock input
RA5/AN4/$\overline{SS}$/LVDIN	27	38	33	46			
RA5					I/O	TTL	Digital I/O
AN4					I	Analog	Analog input 4
$\overline{SS}$					I	ST	SPI slave select input
LVDIN					I	Analog	Low voltage detect input
RA6							See the OSC2/CLKO/RA6 pin

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0	48	60	58	72			
RB0					I/O	TTL	Digital I/O
INT0					I	ST	External interrupt 0
RB1/INT1	47	59	57	71			
RB1					I/O	TTL	Digital I/O
INT1					I	ST	External interrupt 1
RB2/INT2	46	58	56	70			
RB2					I/O	TTL	Digital I/O
INT2					I	ST	External interrupt 2
RB3/INT3	45	57	55	69			
RB3					I/O	TTL	Digital I/O
INT3					I/O	ST	External interrupt 3
RB4	44	56	54	68	I/O	TTL	Digital I/O Interrupt on change pin
RB5	43	55	53	67	I/O	TTL	Digital I/O Interrupt-on-change pin
RB6	42	54	52	66	I/O	TTL	Digital I/O Interrupt-on-change pin
					I	ST	ICSP programming clock
RB7	37	48	47	60	I/O	TTL	Digital I/O Interrupt-on-change pin
					I/O	ST	ICSP programming data

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to V_{DD})

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTC is a bi-directional I/O port
RC0/T1OSO/T13CKI	30	41	36	49			
RC0					I/O	ST	Digital I/O
T1OSO					O	—	Timer1 oscillator output
T13CKI					I	ST	Timer1/Timer3 external clock input
RC1/T1OSI	29	40	35	48			
RC1					I/O	ST	Digital I/O
T1OSI					I	CMOS	Timer1 oscillator input
RC2/CCP1	33	44	43	56			
RC2					I/O	ST	Digital I/O
CCP1					I/O	ST	Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	34	45	44	57			
RC3					I/O	ST	Digital I/O
SCK					I/O	ST	Synchronous serial clock input/output for SPI mode
SCL					I/O	ST	Synchronous serial clock input/output for I^2C mode
RC4/SDI/SDA	35	46	45	58			
RC4					I/O	ST	Digital I/O
SDI					I	ST	SPI data in
SDA					I/O	ST	I^2C data I/O
RC5/SDO	36	47	46	59			
RC5					I/O	ST	Digital I/O
SDO					O	—	SPI data out
RC6/TX/CK	31	42	37	50			
RC6					I/O	ST	Digital I/O
TX					O	—	USART asynchronous transmit
CK					I/O	ST	USART synchronous clock (See RX/DT)
RC7/RX/DT	32	43	38	51			
RC7					I/O	ST	Digital I/O
RX					I	ST	USART asynchronous receive
DT					I/O	ST	USART synchronous data (See TX/CK)

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to V_{DD})

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTD is a bi-directional I/O port. These pins have TTL input buffers when external memory is enabled.
RD0/PSP0	58	3	72	3			
RD0					I/O	ST	Digital I/O
PSP0					I/O	TTL	Parallel slave port data
RD1/PSP1	55	67	69	83			
RD1					I/O	ST	Digital I/O
PSP1					I/O	TTL	Parallel slave port data
RD2/PSP2	54	66	68	82			
RD2					I/O	ST	Digital I/O
PSP2					I/O	TTL	Parallel slave port data
RD3/PSP3	53	65	67	81			
RD3					I/O	ST	Digital I/O
PSP3					I/O	TTL	Parallel slave port data
RD4/PSP4	52	64	66	80			
RD4					I/O	ST	Digital I/O
PSP4					I/O	TTL	Parallel slave port data
RD5/PSP5	51	63	65	79			
RD5					I/O	ST	Digital I/O
PSP5					I/O	TTL	Parallel slave port data
RD6/PSP6	50	62	64	78			
RD6					I/O	ST	Digital I/O
PSP6					I/O	TTL	Parallel slave port data
RD7/PSP7	49	61	63	77			
RD7					I/O	ST	Digital I/O
PSP7					I/O	TTL	Parallel slave port data

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to V_{DD})

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTE is a bi-directional I/O port
RE0/$\overline{RD}$	2	11	4	15			
RE0					I/O	ST	Digital I/O
$\overline{RD}$					I	TTL	Read control for parallel slave port (See $\overline{WR}$ and $\overline{CS}$ pins)
RE1/$\overline{WR}$	1	10	3	14			
RE1					I/O	ST	Digital I/O
$\overline{WR}$					I	TTL	Write control for parallel slave port (See $\overline{CS}$ and $\overline{RD}$ pins)
RE2/$\overline{CS}$	64	9	78	9			
RE2					I/O	ST	Digital I/O
$\overline{CS}$					I	TTL	Chip select control for parallel slave port (See $\overline{RD}$ and $\overline{WR}$)
RE3	63	8	77	8	I/O	ST	Digital I/O
RE4	62	7	76	7	I/O	ST	Digital I/O
RE5	61	6	75	6	I/O	ST	Digital I/O
RE6	60	5	74	5	I/O	ST	Digital I/O
RE7/CCP2	59	4	73	4			
RE7					I/O	ST	Digital I/O
CCP2					I/O	ST	Capture2 input, Compare2 output, PWM2 output

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to V_{DD})

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTF is a bi-directional I/O port
RF0/AN5	18	28	24	36			
RF0					I/O	ST	Digital I/O
AN5					I	Analog	Analog input 5
RF1/AN6/C2OUT	17	27	23	35			
RF1					I/O	ST	Digital I/O
AN6					I	Analog	Analog input 6
C2OUT					O	ST	Comparator 2 output
RF2/AN7/C1OUT	16	26	18	30			
RF2					I/O	ST	Digital I/O
AN7					I	Analog	Analog input 7
C1OUT					O	ST	Comparator 1 output
RF3/AN8	15	25	17	29			
RF1					I/O	ST	Digital I/O
AN8					I	Analog	Analog input 8
RF4/AN9	14	24	16	28			
RF1					I/O	ST	Digital I/O
AN9					I	Analog	Analog input 9
RF5/AN10/CVREF	13	23	15	27			
RF1					I/O	ST	Digital I/O
AN10					I	Analog	Analog input 10
CVREF					O	Analog	Comparator VREF output
RF6/AN11	12	22	14	26			
RF6					I/O	ST	Digital I/O
AN11					I	Analog	Analog input 11
RF7	11	21	13	25	I/O	ST	Digital I/O

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTG is a bi-directional I/O port
RG0/CANTX1	3	12	5	16			
RG0					I/O	ST	Digital I/O
CANTX1					O	CAN Bus	CAN bus output
RG1/CANTX2	4	13	6	17			
RG1					I/O	ST	Digital I/O
CANTX2					O	CAN Bus	Complimentary CAN bus output or CAN bus bit time clock
RG2/CANRX	5	14	7	18			
RG2					I/O	ST	Digital I/O
CANRX					I	CAN Bus	CAN bus input
RG3	6	15	8	19	I/O	ST	Digital I/O
RG4	8	17	10	21	I/O	ST	Digital I/O
							PORTH is a bi-directional I/O port.
RH0	—	—	79	10	I/O	ST	Digital I/O
RH1	—	—	80	11	I/O	ST	Digital I/O
RH2	—	—	1	12	I/O	ST	Digital I/O
RH3	—	—	2	13	I/O	ST	Digital I/O
RH4/AN12	—	—	22	34			
RH4					I/O	ST	Digital I/O
AN12					I	Analog	Analog input 12
RH5/AN13	—	—	21	33			
RH5					I/O	ST	Digital I/O
AN13					I	Analog	Analog input 13
RH6/AN14	—	—	20	32			
RH6					I/O	ST	Digital I/O
AN14					I	Analog	Analog input 14
RH7/AN15	—	—	19	31			
RH7					I/O	ST	Digital I/O
AN15					I	Analog	Analog input 15

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to V_{DD})

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C658		PIC18C858				
	TQFP	PLCC	TQFP	PLCC			
							PORTJ is a bi-directional I/O port
RJ0	—	—	62	76			
RJ0	—	—	—	—			
RJ0					I/O	ST	Digital I/O
RJ1	—	—	61	75			
RJ1	—	—	—	—			
RJ1					I/O	ST	Digital I/O
RJ2	—	—	60	74			
RJ2	—	—	—	—			
RJ2					I/O	ST	Digital I/O
RJ3	—	—	59	73			
RJ3	—	—	—	—			
RJ3					I/O	ST	Digital I/O
							PORTK is a bi-directional I/O port
RK0	—	—	39	52	I/O	ST	Digital I/O
RK1	—	—	40	53	I/O	ST	Digital I/O
RK2	—	—	41	54	I/O	ST	Digital I/O
RK3	—	—	42	55	I/O	ST	Digital I/O
VSS	9, 25, 41, 56	19, 36, 53, 68	11, 31, 51, 70	23, 44, 65, 84	P	—	Ground reference for logic and I/O pins
VDD	10, 26, 38, 57	2, 20, 37, 49	12, 32, 48, 71	2, 24, 45, 61	P	—	Positive supply for logic and I/O pins
AVSS	20	30	26	38	P	—	Ground reference for analog modules
AVDD	19	29	25	37	P	—	Positive supply for analog modules

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open Drain (no P diode to VDD)

2.0 OSCILLATOR CONFIGURATIONS

2.1 Oscillator Types

The PIC18CXX8 can be operated in one of eight oscillator modes, programmable by three configuration bits (FOSC2, FOSC1, and FOSC0).

1. LP Low Power Crystal
2. XT Crystal/Resonator
3. HS High Speed Crystal/Resonator
4. HS4 High Speed Crystal/Resonator with PLL enabled
5. RC External Resistor/Capacitor
6. RCIO External Resistor/Capacitor with I/O pin enabled
7. EC External Clock
8. ECIO External Clock with I/O pin enabled

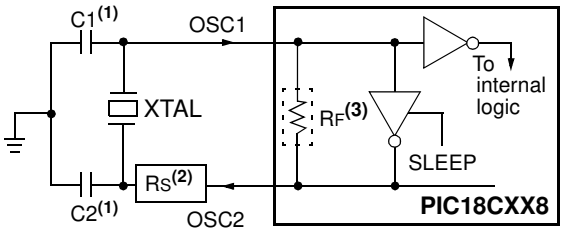
2.2 Crystal Oscillator/Ceramic Resonators

In XT, LP, HS or HS4 (PLL) oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-1 shows the pin connections. An external clock source may also be connected to the OSC1 pin, as shown in Figure 2-3 and Figure 2-4.

The PIC18CXX8 oscillator design requires the use of a parallel cut crystal.

Note:	Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for recommended values of C1 and C2.

2: A series resistor (R_S) may be required for AT strip cut crystals.

3: R_F varies with the crystal chosen.

TABLE 2-1: CERAMIC RESONATORS

Ranges Tested:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz 20.0 MHz 25.0 MHz	10 - 68 pF 10 - 22 pF TBD TBD	10 - 68 pF 10 - 22 pF TBD TBD
HS+PLL	4.0 MHz 8.0 MHz 10.0 MHz	TBD 10 - 68 pF TBD	TBD 10 - 68 pF TBD
These values are for design guidance only. See notes on this page.			
Resonators Used:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%	
All resonators used did not have built-in capacitors.			

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32.0 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1.0 MHz	15 pF	15 pF
	4.0 MHz	15 pF	15 pF
HS	4.0 MHz	15 pF	15 pF
	8.0 MHz	15-33 pF	15-33 pF
	20.0 MHz	15-33 pF	15-33 pF
	25.0 MHz	TBD	TBD
HS+PLL	4.0 MHz	15 pF	15 pF
	8.0 MHz	15-33 pF	15-33 pF
	10.0 MHz	TBD	TBD
These values are for design guidance only. See notes on this page.			
Crystals Used			
32.0 kHz	Epson C-001R32.768K-A	± 20 PPM	
200 kHz	STD XTL 200.000KHz	± 20 PPM	
1.0 MHz	ECS ECS-10-13-1	± 50 PPM	
4.0 MHz	ECS ECS-40-20-1	± 50 PPM	
8.0 MHz	EPSON CA-301 8.000M-C	± 30 PPM	
20.0 MHz	EPSON CA-301 20.000M-C	± 30 PPM	

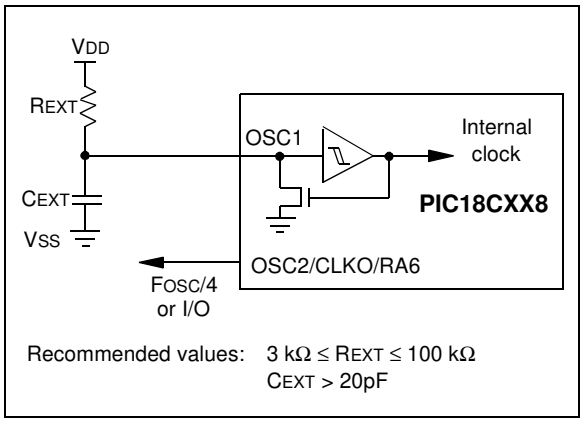
Note 1: Recommended values of C1 and C2 are identical to the ranges tested (Table 2-1).
2: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
4: Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

2.3 RC Oscillator

For timing insensitive applications, the “RC” and "RCIO" device options offer additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 2-2 shows how the R/C combination is connected.

In the RC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic.

FIGURE 2-2: RC OSCILLATOR MODE



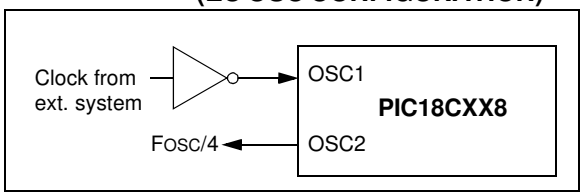
The RCIO oscillator mode functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).

2.4 External Clock Input

The EC and ECIO oscillator modes require an external clock source to be connected to the OSC1 pin. The feedback device between OSC1 and OSC2 is turned off in these modes to save current. There is no oscillator start-up time required after a Power-on Reset or after a recovery from SLEEP mode.

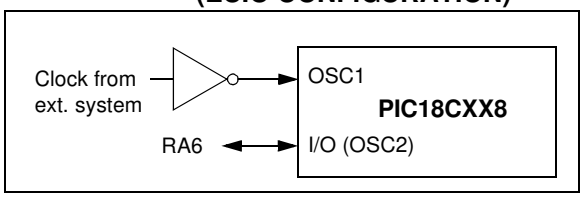
In the EC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-3 shows the pin connections for the EC oscillator mode.

FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (EC OSC CONFIGURATION)



The ECIO oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-4 shows the pin connections for the ECIO oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)



2.5 HS4 (PLL)

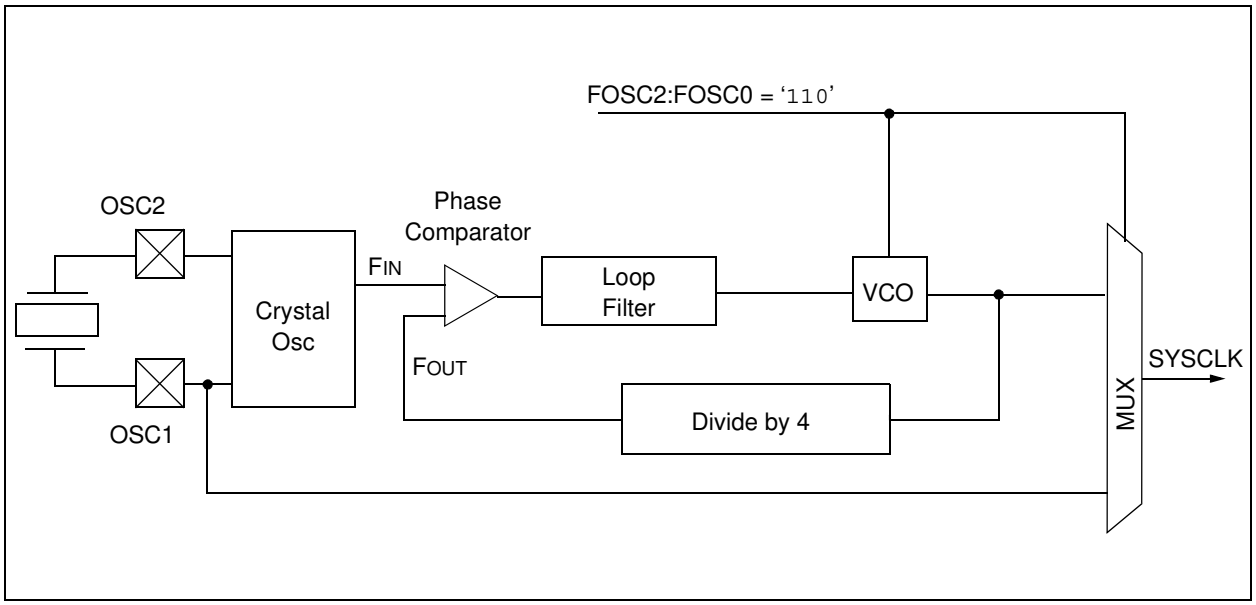
A Phase Locked Loop circuit is provided as a programmable option for users that want to multiply the frequency of the incoming crystal oscillator signal by 4. For an input clock frequency of 10 MHz, the internal clock frequency will be multiplied to 40 MHz. This is useful for customers who are concerned with EMI due to high frequency crystals.

The PLL can only be enabled when the oscillator configuration bits are programmed for HS mode. If they are programmed for any other mode, the PLL is not enabled and the system clock will come directly from OSC1.

The PLL is one of the modes of the FOSC2:FOSC0 configuration bits. The oscillator mode is specified during device programming.

A PLL lock timer is used to ensure that the PLL has locked before device execution starts. The PLL lock timer has a time-out referred to as TPLL.

FIGURE 2-5: PLL BLOCK DIAGRAM



2.6 Oscillator Switching Feature

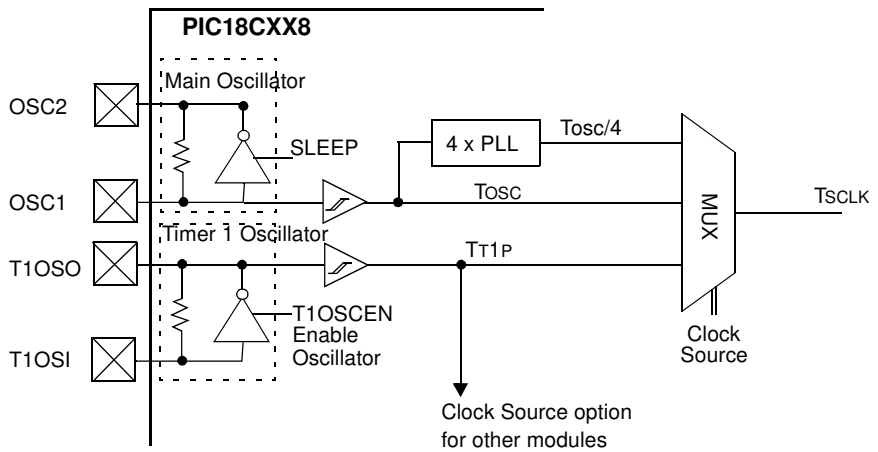
The PIC18CXX8 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low frequency clock source. For the PIC18CXX8 devices, this alternate clock source is the Timer1 oscillator. If a low frequency crystal (32 kHz, for example) has been attached to the Timer1 oscillator pins and the Timer1 oscillator has been enabled, the device can switch to a low power execution mode. Figure 2-6 shows a block diagram of the system clock sources. The clock switching feature is enabled by programming the Oscillator Switching Enable ($\overline{\text{OSCSEN}}$) bit in Configuration register CONFIG1H to a '0'. Clock switching is disabled in an erased device. See Section 9 for further details of the Timer1 oscillator. See Section 22.0 for Configuration Register details.

2.6.1 SYSTEM CLOCK SWITCH BIT

The system clock source switching is performed under software control. The system clock switch bit, SCS (OSCCON register), controls the clock switching. When the SCS bit is '0', the system clock source comes from the main oscillator selected by the FOSC2:FOSC0 configuration bits. When the SCS bit is set, the system clock source will come from the Timer1 oscillator. The SCS bit is cleared on all forms of RESET.

Note:	The Timer1 oscillator must be enabled to switch the system clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 control register (T1CON). If the Timer1 oscillator is not enabled, any write to the SCS bit will be ignored (SCS bit forced cleared) and the main oscillator will continue to be the system clock source.

FIGURE 2-6: DEVICE CLOCK SOURCES



Note: I/O pins have diode protection to VDD and VSS.

REGISTER 2-1: OSCCON REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
—	—	—	—	—	—	—	SCS
bit 7							bit 0

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SCS:** System Clock Switch bit
when $\overline{\text{OSCSEN}}$ configuration bit = '0' and T1OSCEN bit is set:
1 = Switch to Timer1 Oscillator/Clock pin
0 = Use primary Oscillator/Clock input pin
when $\overline{\text{OSCSEN}}$ is clear or T1OSCEN is clear:
bit is forced clear

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown