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18/20/28-Pin High-Performance, Enhanced Flash MCUs with 10-bit A/D

Low-Power Features

- Power Managed modes:
  - Run: CPU on, peripherals on
  - Idle: CPU off, peripherals on
  - Sleep: CPU off, peripherals off
- Power Consumption modes:
  - PRI_RUN: 150 µA, 1 MHz, 2V
  - PRI_IDLE: 37 µA, 1 MHz, 2V
  - SEC_RUN: 14 µA, 32 kHz, 2V
  - SEC_IDLE: 5.8 µA, 32 kHz, 2V
  - RC_RUN: 110 µA, 1 MHz, 2V
  - RC_IDLE: 52 µA, 1 MHz, 2V
  - Sleep: 0.1 µA, 1 MHz, 2V
- Timer1 Oscillator: 1.1 µA, 32 kHz, 2V
- Watchdog Timer: 2.1 µA
- Two-Speed Oscillator Start-up

Oscillators

- Four Crystal modes:
  - LP, XT, HS: up to 25 MHz
  - HSPLL: 4-10 MHz (16-40 MHz internal)
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies: 31 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 4 MHz, 8 MHz
  - 125 kHz to 8 MHz calibrated to 1%
  - Two modes select one or two I/O pins
  - OSCTUNE – Allows user to shift frequency
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripheral clock stops

Peripheral Highlights

- High Current Sink/Source 25 mA/25 mA
- Three External Interrupts
- Enhanced Capture/Compare/PWM (ECCP) module:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-Shutdown and Auto-Restart
  - Capture is 16-bit, max resolution 6.25 ns ($T_{CY}/16$)
  - Compare is 16-bit, max resolution 100 ns (T_{CY})
- Compatible 10-bit, up to 13-Channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Enhanced USART module:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-Wake-up on Start bit
  - Auto-Baud Detect

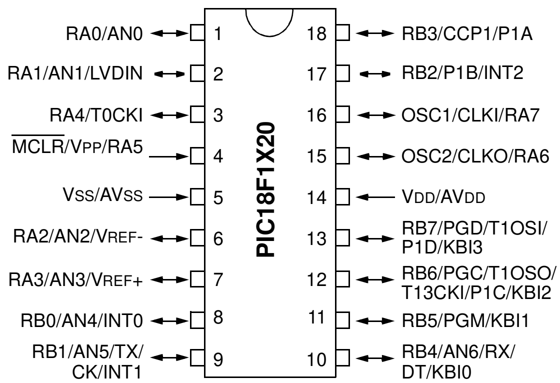
Special Microcontroller Features

- 100,000 Erase/Write Cycle Enhanced Flash Program Memory, typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory, typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
  - 2% stability over V_{DD} and Temperature
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V

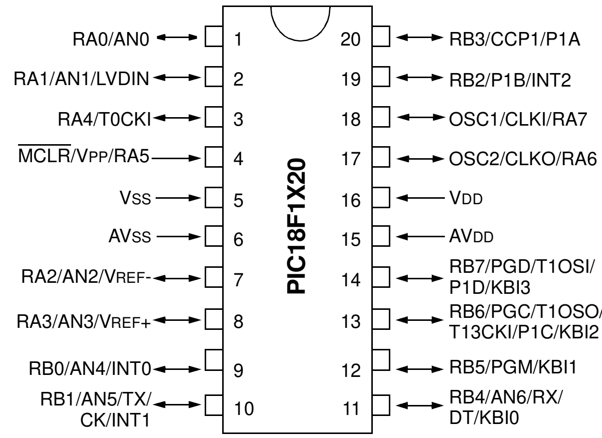
Device	Program Memory		Data Memory		I/O	10-bit A/D (ch)	ECCP (PWM)	EUSART	Timers 8/16-bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					
PIC18F1220	4K	2048	256	256	16	7	1	Y	1/3
PIC18F1320	8K	4096	256	256	16	7	1	Y	1/3

Pin Diagrams

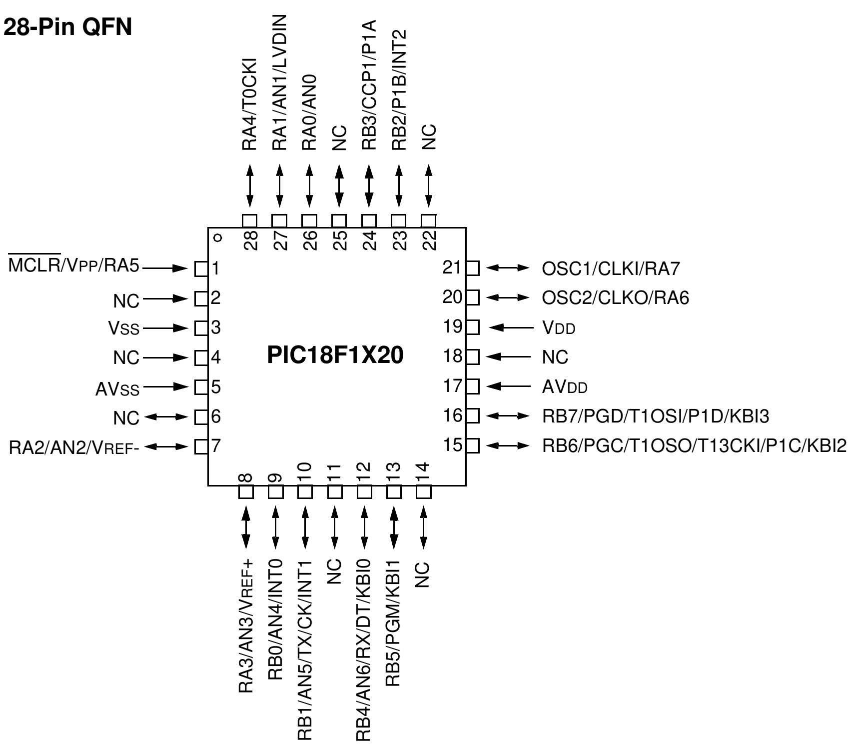
18-Pin PDIP, SOIC



20-Pin SSOP



28-Pin QFN



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1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F1220
- PIC18F1320

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high endurance Enhanced Flash program memory. On top of these features, the PIC18F1220/1320 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 POWER MODES

All of the devices in the PIC18F1220/1320 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled, but the peripherals are still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Lower Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer have been reduced by up to 80%, with typical values of 1.1 and 2.1 μA, respectively.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F1220/1320 family offer nine different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output), or one pin (oscillator input, with the second pin reassigned as general I/O).
- Two External RC Oscillator modes, with the same pin options as the External Clock modes.
- An internal oscillator block, which provides an 8 MHz clock (±2% accuracy) and an INTRC source (approximately 31 kHz, stable over temperature and V_{DD}), as well as a range of six user-selectable clock frequencies (from 125 kHz to 4 MHz) for a total of 8 clock frequencies.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued low-speed operation, or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available. This allows for code execution during what would otherwise be the clock start-up interval and can even allow an application to perform routine background activities and return to Sleep without returning to full-power operation.

1.2 Other Special Features

- **Memory Endurance:** The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- **Enhanced CCP module:** In PWM mode, this module provides 1, 2 or 4 modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown, for disabling PWM outputs on interrupt or other select conditions and auto-restart, to reactivate outputs once the condition has cleared.
- **Enhanced USART:** This serial communication module features automatic wake-up on Start bit and automatic baud rate detection and supports RS-232, RS-485 and LIN 1.2 protocols, making it ideally suited for use in Local Interconnect Network (LIN) bus applications.
- **10-bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing a time-out range from 4 ms to over two minutes that is stable across operating voltage and temperature.

1.3 Details on Individual Family Members

Devices in the PIC18F1220/1320 family are available in 18-pin, 20-pin and 28-pin packages. A block diagram for this device family is shown in Figure 1-1.

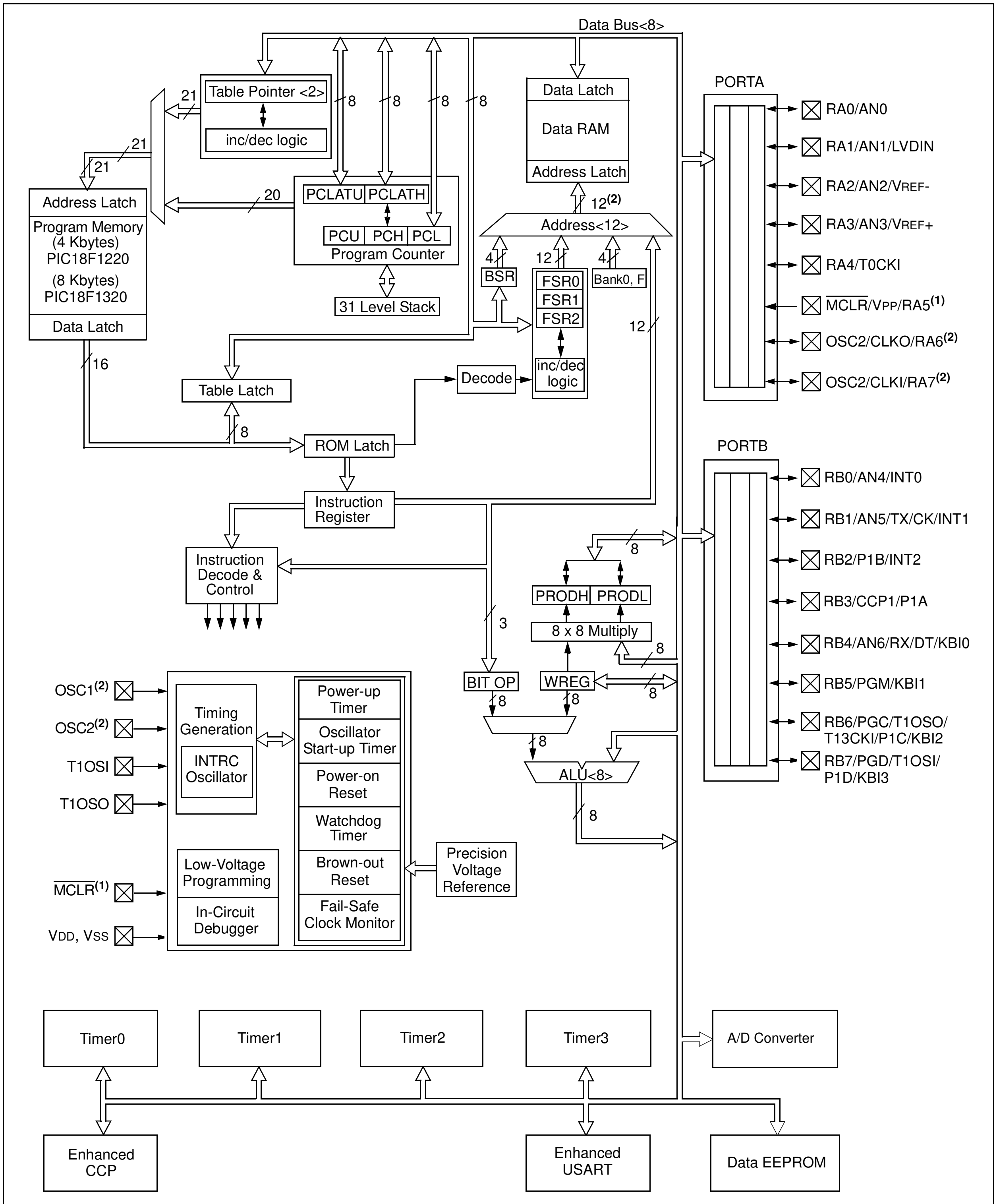
The devices are differentiated from each other only in the amount of on-chip Flash program memory (4 Kbytes for the PIC18F1220 device, 8 Kbytes for the PIC18F1320 device). These and other features are summarized in Table 1-1.

A block diagram of the PIC18F1220/1320 device architecture is provided in Figure 1-1. The pinouts for this device family are listed in Table 1-2.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F1220	PIC18F1320
Operating Frequency	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	4096	8192
Program Memory (Instructions)	2048	4096
Data Memory (Bytes)	256	256
Data EEPROM Memory (Bytes)	256	256
Interrupt Sources	15	15
I/O Ports	Ports A, B	Ports A, B
Timers	4	4
Enhanced Capture/Compare/PWM Modules	1	1
Serial Communications	Enhanced USART	Enhanced USART
10-bit Analog-to-Digital Module	7 input channels	7 input channels
Resets (and Delays)	POR, BOR, `RESET` Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{\text{MCLR}}$ (optional), WDT	POR, BOR, `RESET` Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{\text{MCLR}}$ (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes
Programmable Brown-out Reset	Yes	Yes
Instruction Set	75 Instructions	75 Instructions
Packages	18-pin SDIP 18-pin SOIC 20-pin SSOP 28-pin QFN	18-pin SDIP 18-pin SOIC 20-pin SSOP 28-pin QFN

FIGURE 1-1: PIC18F1220/1320 BLOCK DIAGRAM



Note 1: RA5 is available only when the MCLR Reset is disabled.

2: OSC1, OSC2, CLKI and CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Configurations"** for additional information.

TABLE 1-2: PIC18F1220/1320 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP/ SOIC	SSOP	QFN			
$\overline{\text{MCLR}}$/VPP/RA5	4	4	1			Master Clear (input) or programming voltage (input).
$\overline{\text{MCLR}}$				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				P	—	Programming voltage input.
RA5				I	ST	Digital input.
OSC1/CLKI/RA7	16	18	21			Oscillator crystal or external clock input.
OSC1				I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise.
CLKI				I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7				I/O	ST	General purpose I/O pin.
OSC2/CLKO/RA6	15	17	20			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC, EC and INTRC modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes instruction cycle rate.
RA6				I/O	ST	General purpose I/O pin.
						PORTA is a bidirectional I/O port.
RA0/AN0	1	1	26			
RA0				I/O	ST	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1/LVDIN	2	2	27			
RA1				I/O	ST	Digital I/O.
AN1				I	Analog	Analog input 1.
LVDIN				I	Analog	Low-Voltage Detect input.
RA2/AN2/VREF-	6	7	7			
RA2				I/O	ST	Digital I/O.
AN2				I	Analog	Analog input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
RA3/AN3/VREF+	7	8	8			
RA3				I/O	ST	Digital I/O.
AN3				I	Analog	Analog input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI	3	3	28			
RA4				I/O	ST/OD	Digital I/O. Open-drain when configured as output.
T0CKI				I	ST	Timer0 external clock input.
RA5						See the $\overline{\text{MCLR}}$/VPP/RA5 pin.
RA6						See the OSC2/CLKO/RA6 pin.
RA7						See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power; OD = Open-drain (no P diode to VDD)

TABLE 1-2: PIC18F1220/1320 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP/ SOIC	SSOP	QFN			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN4/INT0	8	9	9			
RB0				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
INT0				I	ST	External interrupt 0.
RB1/AN5/TX/CK/INT1	9	10	10			
RB1				I/O	TTL	Digital I/O.
AN5				I	Analog	Analog input 5.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see related RX/DT).
INT1				I	ST	External interrupt 1.
RB2/P1B/INT2	17	19	23			
RB2				I/O	TTL	Digital I/O.
P1B				O	—	Enhanced CCP1/PWM output.
INT2				I	ST	External interrupt 2.
RB3/CCP1/P1A	18	20	24			
RB3				I/O	TTL	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
P1A				O	—	Enhanced CCP1/PWM output.
RB4/AN6/RX/DT/KBI0	10	11	12			
RB4				I/O	TTL	Digital I/O.
AN6				I	Analog	Analog input 6.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see related TX/CK).
KBI0				I	TTL	Interrupt-on-change pin.
RB5/PGM/KBI1	11	12	13			
RB5				I/O	TTL	Digital I/O.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
KBI1				I	TTL	Interrupt-on-change pin.
RB6/PGC/T1OSO/ T13CKI/P1C/KBI2	12	13	15			
RB6				I/O	TTL	Digital I/O.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock output.
P1C				O	—	Enhanced CCP1/PWM output.
KBI2				I	TTL	Interrupt-on-change pin.
RB7/PGD/T1OSI/ P1D/KBI3	13	14	16			
RB7				I/O	TTL	Digital I/O.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.
T1OSI				I	CMOS	Timer1 oscillator input.
P1D				O	—	Enhanced CCP1/PWM output.
KBI3				I	TTL	Interrupt-on-change pin.
VSS	5	5, 6	3, 5	P	—	Ground reference for logic and I/O pins.
VDD	14	15, 16	17, 19	P	—	Positive supply for logic and I/O pins.
NC	—	—	18	—	—	No connect.

Legend: TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; O = Output; OD = Open-drain (no P diode to VDD); CMOS = CMOS compatible input or output; I = Input; P = Power

2.0 OSCILLATOR CONFIGURATIONS

2.1 Oscillator Types

The PIC18F1220 and PIC18F1320 devices can be operated in ten different oscillator modes. The user can program the Configuration bits, FOSC3:FOSC0, in Configuration Register 1H to select one of these ten modes:

1. LP — Low-Power Crystal
2. XT — Crystal/Resonator
3. HS — High-Speed Crystal/Resonator
4. HSPLL — High-Speed Crystal/Resonator with PLL enabled
5. RC — External Resistor/Capacitor with FOSC/4 output on RA6
6. RCIO — External Resistor/Capacitor with I/O on RA6
7. INTIO1 — Internal Oscillator with FOSC/4 output on RA6 and I/O on RA7
8. INTIO2 — Internal Oscillator with I/O on RA6 and RA7
9. EC — External Clock with FOSC/4 output
10. ECIO — External Clock with I/O on RA6

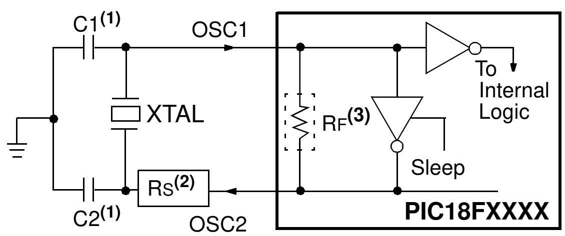
2.2 Crystal Oscillator/Ceramic Resonators

In XT, LP, HS or HSPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-1 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

Note:	Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-1: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, LP, HS OR HSPLL CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for initial values of C1 and C2.

2: A series resistor (RS) may be required for AT strip cut crystals.

3: RF varies with the oscillator mode chosen.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Typical Capacitor Values Used:			
Mode	**Freq.**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	56 pF 47 pF 33 pF	56 pF 47 pF 33 pF
HS	8.0 MHz 16.0 MHz	27 pF 22 pF	27 pF 22 pF

Capacitor values are for design guidance only.

These capacitors were tested with the resonators listed below for basic start-up and operation. **These values are not optimized**.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following Table 2-2 for additional information.

Resonators Used:	
455 kHz	4.0 MHz
2.0 MHz	8.0 MHz
16.0 MHz	

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq.	Typical Capacitor Values Tested: C1	C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	1 MHz	33 pF	33 pF
	4 MHz	27 pF	27 pF
HS	4 MHz	27 pF	27 pF
	8 MHz	22 pF	22 pF
	20 MHz	15 pF	15 pF

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.**

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

Crystals Used:	
32 kHz	4 MHz
200 kHz	8 MHz
1 MHz	20 MHz

Note 1: Higher capacitance increases the stability of oscillator, but also increases the start-up time.

2: When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.

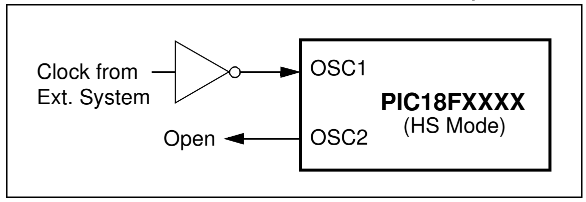
3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: RS may be required to avoid overdriving crystals with low drive level specification.

5: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An external clock source may also be connected to the OSC1 pin in the HS mode, as shown in Figure 2-2.

FIGURE 2-2: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)



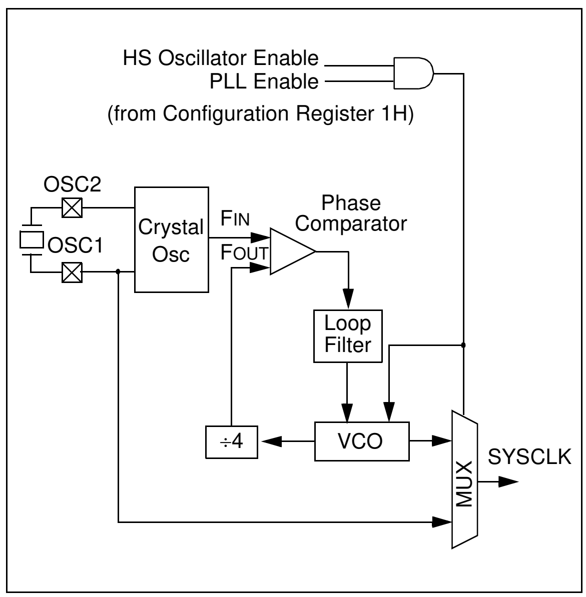
2.3 HSPLL

A Phase Locked Loop (PLL) circuit is provided as an option for users who wish to use a lower frequency crystal oscillator circuit, or to clock the device up to its highest rated frequency from a crystal oscillator. This may be useful for customers who are concerned with EMI due to high-frequency crystals.

The HSPLL mode makes use of the HS mode oscillator for frequencies up to 10 MHz. A PLL then multiplies the oscillator output frequency by 4 to produce an internal clock frequency up to 40 MHz.

The PLL is enabled only when the oscillator Configuration bits are programmed for HSPLL mode. If programmed for any other mode, the PLL is not enabled.

FIGURE 2-3: PLL BLOCK DIAGRAM

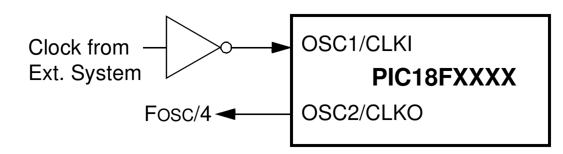


2.4 External Clock Input

The EC and ECIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset, or after an exit from Sleep mode.

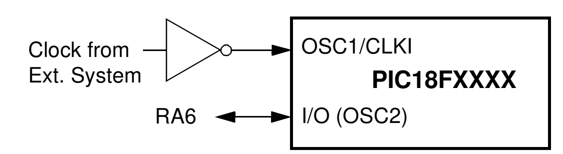
In the EC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes, or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC CONFIGURATION)



The ECIO Oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)

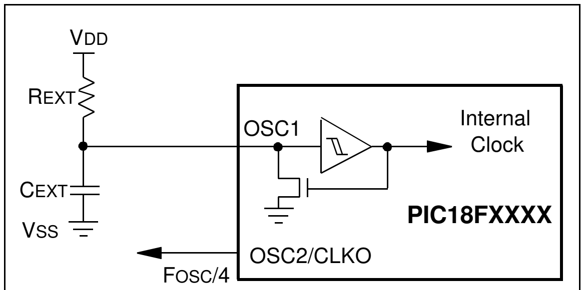


2.5 RC Oscillator

For timing insensitive applications, the "RC" and "RCIO" device options offer additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal manufacturing variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation, due to tolerance of external R and C components used. Figure 2-6 shows how the R/C combination is connected.

In the RC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes, or to synchronize other logic.

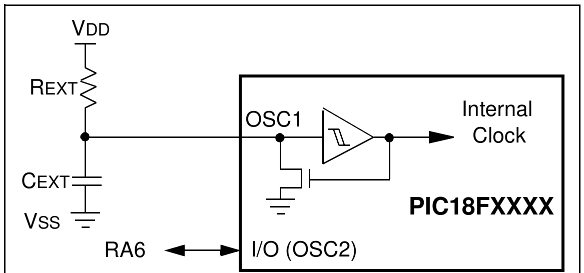
FIGURE 2-6: RC OSCILLATOR MODE



Recommended values: 3 kΩ ≤ REXT ≤ 100 kΩ
CEXT > 20 pF

The RCIO Oscillator mode (Figure 2-7) functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).

FIGURE 2-7: RCIO OSCILLATOR MODE



Recommended values: 3 kΩ ≤ REXT ≤ 100 kΩ
CEXT > 20 pF

2.6 Internal Oscillator Block

The PIC18F1220/1320 devices include an internal oscillator block, which generates two different clock signals; either can be used as the system's clock source. This can eliminate the need for external oscillator circuits on the OSC1 and/or OSC2 pins.

The main output (INTOSC) is an 8 MHz clock source, which can be used to directly drive the system clock. It also drives a postscaler, which can provide a range of clock frequencies from 125 kHz to 4 MHz. The INTOSC output is enabled when a system clock frequency from 125 kHz to 8 MHz is selected.

The other clock source is the internal RC oscillator (INTRC), which provides a 31 kHz output. The INTRC oscillator is enabled by selecting the internal oscillator block as the system clock source, or when any of the following are enabled:

- Power-up Timer
- Fail-Safe Clock Monitor
- Watchdog Timer
- Two-Speed Start-up

These features are discussed in greater detail in **Section 19.0 "Special Features of the CPU"**.

The clock source frequency (INTOSC direct, INTRC direct or INTOSC postscaler) is selected by configuring the IRCF bits of the OSCCON register (Register 2-2).

2.6.1 INTIO MODES

Using the internal oscillator as the clock source can eliminate the need for up to two external oscillator pins, which can then be used for digital I/O. Two distinct configurations are available:

- In INTIO1 mode, the OSC2 pin outputs FOSC/4, while OSC1 functions as RA7 for digital input and output.
- In INTIO2 mode, OSC1 functions as RA7 and OSC2 functions as RA6, both for digital input and output.

2.6.2 INTRC OUTPUT FREQUENCY

The internal oscillator block is calibrated at the factory to produce an INTOSC output frequency of 8.0 MHz (see Table 22-6). This changes the frequency of the INTRC source from its nominal 31.25 kHz. Peripherals and features that depend on the INTRC source will be affected by this shift in frequency.

Once set during factory calibration, the INTRC frequency will remain within ±2% as temperature and VDD change across their full specified operating ranges.

2.6.3 OSCTUNE REGISTER

The internal oscillator's output has been calibrated at the factory, but can be adjusted in the user's application. This is done by writing to the OSCTUNE register (Register 2-1). The tuning sensitivity is constant throughout the tuning range.

When the OSCTUNE register is modified, the INTOSC and INTRC frequencies will begin shifting to the new frequency. The INTRC clock will reach the new frequency within 8 clock cycles (approximately 8 * 32 μs = 256 μs). The INTOSC clock will stabilize within 1 ms. Code execution continues during this shift. There is no indication that the shift has occurred. Operation of features that depend on the INTRC clock source frequency, such as the WDT, Fail-Safe Clock Monitor and peripherals, will also be affected by the change in frequency.

REGISTER 2-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	TUN<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** Frequency Tuning bits
`100000` = Minimum frequency
•
•
•
`111111` =
`000000` = Oscillator module is running at the factory-calibrated frequency
`000001` =
•
•
•
`011110` =
`011111` = Maximum frequency

2.7 Clock Sources and Oscillator Switching

Like previous PIC18 devices, the PIC18F1220/1320 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low-frequency clock source. PIC18F1220/1320 devices offer two alternate clock sources. When enabled, these give additional options for switching to the various power managed operating modes.

Essentially, there are three clock sources for these devices:

- Primary oscillators
- Secondary oscillators
- Internal oscillator block

The **primary oscillators** include the External Crystal and Resonator modes, the External RC modes, the External Clock modes and the internal oscillator block. The particular mode is defined on POR by the contents of Configuration Register 1H. The details of these modes are covered earlier in this chapter.

The **secondary oscillators** are those external sources not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power managed mode.

PIC18F1220/1320 devices offer only the Timer1 oscillator as a secondary oscillator. This oscillator, in all power managed modes, is often the time base for functions such as a real-time clock.

Most often, a 32.768 kHz watch crystal is connected between the RB6/T1OSO and RB7/T1OSI pins. Like the LP mode oscillator circuit, loading capacitors are also connected from each pin to ground. These pins are also used during ICSP operations.

The Timer1 oscillator is discussed in greater detail in **Section 12.2 "Timer1 Oscillator"**.

In addition to being a primary clock source, the **internal oscillator block** is available as a power managed mode clock source. The INTRC source is also used as the clock source for several special features, such as the WDT and Fail-Safe Clock Monitor.

The clock sources for the PIC18F1220/1320 devices are shown in Figure 2-8. See **Section 12.0 "Timer1 Module"** for further details of the Timer1 oscillator. See **Section 19.1 "Configuration Bits"** for Configuration register details.

2.7.1 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 2-2) controls several aspects of the system clock's operation, both in full-power operation and in power managed modes.

The System Clock Select bits, SCS1:SCS0, select the clock source that is used when the device is operating in power managed modes. The available clock sources are the primary clock (defined in Configuration Register 1H), the secondary clock (Timer1 oscillator) and the internal oscillator block. The clock selection has no effect until a `SLEEP` instruction is executed and the device enters a power managed mode of operation. The SCS bits are cleared on all forms of Reset.

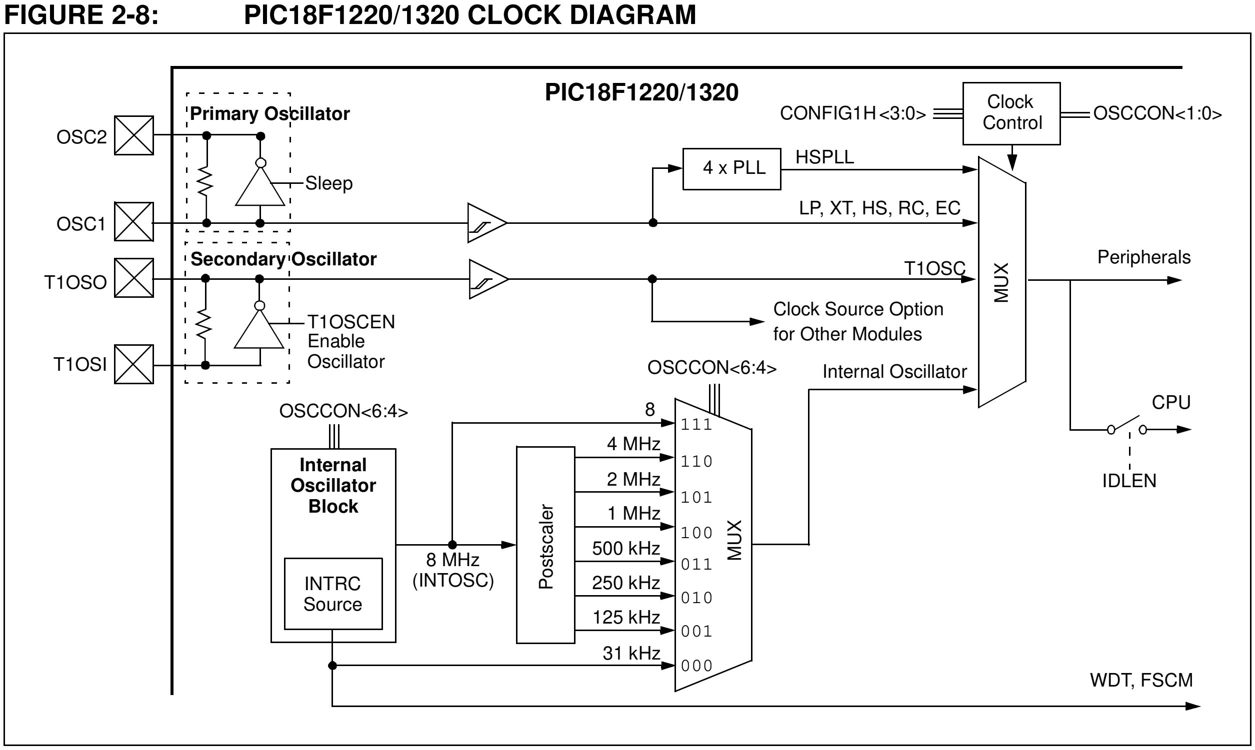
The Internal Oscillator Select bits, IRCF2:IRCF0, select the frequency output of the internal oscillator block that is used to drive the system clock. The choices are the INTRC source, the INTOSC source (8 MHz), or one of the six frequencies derived from the INTOSC postscaler (125 kHz to 4 MHz). If the internal oscillator block is supplying the system clock, changing the states of these bits will have an immediate change on the internal oscillator's output.

The OSTS, IOFS and T1RUN bits indicate which clock source is currently providing the system clock. The OSTS indicates that the Oscillator Start-up Timer has timed out and the primary clock is providing the system clock in Primary Clock modes. The IOFS bit indicates when the internal oscillator block has stabilized and is providing the system clock in RC Clock modes or during Two-Speed Start-ups. The T1RUN bit (T1CON<6>) indicates when the Timer1 oscillator is providing the system clock in Secondary Clock modes. In power managed modes, only one of these three bits will be set at any time. If none of these bits are set, the INTRC is providing the system clock, or the internal oscillator block has just started and is not yet stable.

The IDLEN bit controls the selective shutdown of the controller's CPU in power managed modes. The uses of these bits are discussed in more detail in **Section 3.0 "Power Managed Modes"**.

> **Note 1:** The Timer1 oscillator must be enabled to select the secondary clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 Control register (T1CON<3>). If the Timer1 oscillator is not enabled, then any attempt to select a secondary clock source when executing a `SLEEP` instruction will be ignored.
>
> **2:** It is recommended that the Timer1 oscillator be operating and stable before executing the `SLEEP` instruction or a very long delay may occur while the Timer1 oscillator starts.

FIGURE 2-8: PIC18F1220/1320 CLOCK DIAGRAM



REGISTER 2-2: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R[(1)]	R-0/0	R/W-0/0	R/W-0/0
IDLEN	IRCF<2:0>			OSTS	IOFS	SCS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **IDLEN:** Idle Enable bits
1 = Idle mode enabled; CPU core is not clocked in power managed modes
0 = Run mode enabled; CPU core is clocked in Run modes, but not Sleep mode

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits
111 = 8 MHz (8 MHz source drives clock directly)
110 = 4 MHz
101 = 2 MHz
100 = 1 MHz
011 = 500 kHz
010 = 250 kHz
001 = 125 kHz
000 = 31 kHz (INTRC source drives clock directly)

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit
1 = Oscillator Start-up Timer time-out has expired; primary oscillator is running
0 = Oscillator Start-up Timer time-out is running; primary oscillator is not ready

bit 2 **IOFS:** INTOSC Frequency Stable bit
1 = INTOSC frequency is stable
0 = INTOSC frequency is not stable

bit 1-0 **SCS<1:0>:** System Clock Select bits[(1)]
1x = Internal oscillator block (RC modes)
01 =Timer1 oscillator (Secondary modes)
00 = Primary oscillator (Sleep and PRI_IDLE modes)

Note 1: Depends on state of the IESO bit in Configuration Register 1H.

2.7.2 OSCILLATOR TRANSITIONS

The PIC18F1220/1320 devices contain circuitry to prevent clocking "glitches" when switching between clock sources. A short pause in the system clock occurs during the clock switch. The length of this pause is between eight and nine clock periods of the new clock source. This ensures that the new clock source is stable and that its pulse width will not be less than the shortest pulse width of the two clock sources.

Clock transitions are discussed in greater detail in **Section 3.1.2 "Entering Power Managed Modes"**.

2.8 Effects of Power Managed Modes on the Various Clock Sources

When the device executes a `SLEEP` instruction, the system is switched to one of the power managed modes, depending on the state of the IDLEN and SCS1:SCS0 bits of the OSCCON register. See **Section 3.0 "Power Managed Modes"** for details.

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin, if used by the oscillator) will stop oscillating.

In Secondary Clock modes (SEC_RUN and SEC_IDLE), the Timer1 oscillator is operating and providing the system clock. The Timer1 oscillator may also run in all power managed modes if required to clock Timer1 or Timer3.

In Internal Oscillator modes (RC_RUN and RC_IDLE), the internal oscillator block provides the system clock source. The INTRC output can be used directly to provide the system clock and may be enabled to support various special features, regardless of the power managed mode (see **Section 19.2 "Watchdog Timer (WDT)"** through **Section 19.4 "Fail-Safe Clock Monitor"**). The INTOSC output at 8 MHz may be used directly to clock the system, or may be divided down first. The INTOSC output is disabled if the system clock is provided directly from the INTRC output.

If the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The INTRC is required to support WDT operation. The Timer1 oscillator may be operating to support a real-time clock. Other features may be operating that do not require a system clock source (i.e., INTn pins, A/D conversions and others).

2.9 Power-up Delays

Power-up delays are controlled by two timers, so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see Sections 4.1 through 4.5.

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on power-up (parameter 33, Table 22-8) if enabled in Configuration Register 2L. The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (LP, XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the HSPLL Oscillator mode is selected, the device is kept in Reset for an additional 2 ms following the HS mode OST delay, so the PLL can lock to the incoming clock frequency.

There is a delay of 5 to 10 μs following POR while the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC, RC or INTIO modes are used as the primary clock source.

TABLE 2-3: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

Oscillator Mode	OSC1 Pin	OSC2 Pin
RC, INTIO1	Floating, external resistor should pull high	At logic low (clock/4 output)
RCIO, INTIO2	Floating, external resistor should pull high	Configured as PORTA, bit 6
ECIO	Floating, pulled by external clock	Configured as PORTA, bit 6
EC	Floating, pulled by external clock	At logic low (clock/4 output)
LP, XT and HS	Feedback inverter disabled at quiescent voltage level	Feedback inverter disabled at quiescent voltage level

Note: See Table 4-1 in **Section 4.0 "Reset"** for time-outs due to Sleep and $\overline{\text{MCLR}}$ Reset.

3.0 POWER MANAGED MODES

The PIC18F1220/1320 devices offer a total of six operating modes for more efficient power management (see Table 3-1). These provide a variety of options for selective power conservation in applications where resources may be limited (i.e., battery powered devices).

There are three categories of power managed modes:

- Sleep mode
- Idle modes
- Run modes

These categories define which portions of the device are clocked and sometimes, what speed. The Run and Idle modes may use any of the three available clock sources (primary, secondary or INTOSC multiplexer); the Sleep mode does not use a clock source.

The clock switching feature offered in other PIC18 devices (i.e., using the Timer1 oscillator in place of the primary oscillator) and the Sleep mode offered by all PIC® devices (where all system clocks are stopped) are both offered in the PIC18F1220/1320 devices (SEC_RUN and Sleep modes, respectively). However, additional power managed modes are available that allow the user greater flexibility in determining what portions of the device are operating. The power managed modes are event driven; that is, some specific event must occur for the device to enter or (more particularly) exit these operating modes.

For PIC18F1220/1320 devices, the power managed modes are invoked by using the existing `SLEEP` instruction. All modes exit to PRI_RUN mode when triggered by an interrupt, a Reset or a WDT time-out (PRI_RUN mode is the normal full-power execution mode; the CPU and peripherals are clocked by the primary oscillator source). In addition, power managed Run modes may also exit to Sleep mode, or their corresponding Idle mode.

3.1 Selecting Power Managed Modes

Selecting a power managed mode requires deciding if the CPU is to be clocked or not and selecting a clock source. The IDLEN bit controls CPU clocking, while the SCS1:SCS0 bits select a clock source. The individual modes, bit settings, clock sources and affected modules are summarized in Table 3-1.

3.1.1 CLOCK SOURCES

The clock source is selected by setting the SCS bits of the OSCCON register (Register 2-2). Three clock sources are available for use in power managed Idle modes: the primary clock (as configured in Configuration Register 1H), the secondary clock (Timer1 oscillator) and the internal oscillator block. The secondary and internal oscillator block sources are available for the power managed modes (PRI_RUN mode is the normal full-power execution mode; the CPU and peripherals are clocked by the primary oscillator source).

TABLE 3-1: POWER MANAGED MODES

Mode	OSCCON Bits		Module Clocking		Available Clock and Oscillator Source
	IDLEN <7>	SCS1:SCS0 <1:0>	CPU	Peripherals	
Sleep	0	00	Off	Off	None – All clocks are disabled
PRI_RUN	0	00	Clocked	Clocked	Primary – LP, XT, HS, HSPLL, RC, EC, INTRC(1) This is the normal full-power execution mode.
SEC_RUN	0	01	Clocked	Clocked	Secondary – Timer1 Oscillator
RC_RUN	0	1x	Clocked	Clocked	Internal Oscillator Block(1)
PRI_IDLE	1	00	Off	Clocked	Primary – LP, XT, HS, HSPLL, RC, EC
SEC_IDLE	1	01	Off	Clocked	Secondary – Timer1 Oscillator
RC_IDLE	1	1x	Off	Clocked	Internal Oscillator Block(1)

Note 1: Includes INTOSC and INTOSC postscaler, as well as the INTRC source.

3.1.2 ENTERING POWER MANAGED MODES

In general, entry, exit and switching between power managed clock sources requires clock source switching. In each case, the sequence of events is the same.

Any change in the power managed mode begins with loading the OSCCON register and executing a `SLEEP` instruction. The SCS1:SCS0 bits select one of three power managed clock sources; the primary clock (as defined in Configuration Register 1H), the secondary clock (the Timer1 oscillator) and the internal oscillator block (used in RC modes). Modifying the SCS bits will have no effect until a `SLEEP` instruction is executed. Entry to the power managed mode is triggered by the execution of a `SLEEP` instruction.

Figure 3-5 shows how the system is clocked while switching from the primary clock to the Timer1 oscillator. When the `SLEEP` instruction is executed, clocks to the device are stopped at the beginning of the next instruction cycle. Eight clock cycles from the new clock source are counted to synchronize with the new clock source. After eight clock pulses from the new clock source are counted, clocks from the new clock source resume clocking the system. The actual length of the pause is between eight and nine clock periods from the new clock source. This ensures that the new clock source is stable and that its pulse width will not be less than the shortest pulse width of the two clock sources.

Three bits indicate the current clock source: OSTS and IOFS in the OSCCON register and T1RUN in the T1CON register. Only one of these bits will be set while in a power managed mode. When the OSTS bit is set, the primary clock is providing the system clock. When the IOFS bit is set, the INTOSC output is providing a stable 8 MHz clock source and is providing the system clock. When the T1RUN bit is set, the Timer1 oscillator is providing the system clock. If none of these bits are set, then either the INTRC clock source is clocking the system, or the INTOSC source is not yet stable.

If the internal oscillator block is configured as the primary clock source in Configuration Register 1H, then both the OSTS and IOFS bits may be set when in PRI_RUN or PRI_IDLE modes. This indicates that the primary clock (INTOSC output) is generating a stable 8 MHz output. Entering an RC power managed mode (same frequency) would clear the OSTS bit.

> **Note 1:** Caution should be used when modifying a single IRCF bit. If VDD is less than 3V, it is possible to select a higher clock speed than is supported by the low VDD. Improper device operation may result if the VDD/FOSC specifications are violated.
>
> **2:** Executing a `SLEEP` instruction does not necessarily place the device into Sleep mode; executing a `SLEEP` instruction is simply a trigger to place the controller into a power managed mode selected by the OSCCON register, one of which is Sleep mode.

3.1.3 MULTIPLE SLEEP COMMANDS

The power managed mode that is invoked with the `SLEEP` instruction is determined by the settings of the IDLEN and SCS bits at the time the instruction is executed. If another `SLEEP` instruction is executed, the device will enter the power managed mode specified by these same bits at that time. If the bits have changed, the device will enter the new power managed mode specified by the new bit settings.

3.1.4 COMPARISONS BETWEEN RUN AND IDLE MODES

Clock source selection for the Run modes is identical to the corresponding Idle modes. When a `SLEEP` instruction is executed, the SCS bits in the OSCCON register are used to switch to a different clock source. As a result, if there is a change of clock source at the time a `SLEEP` instruction is executed, a clock switch will occur.

In Idle modes, the CPU is not clocked and is not running. In Run modes, the CPU is clocked and executing code. This difference modifies the operation of the WDT when it times out. In Idle modes, a WDT time-out results in a wake from power managed modes. In Run modes, a WDT time-out results in a WDT Reset (see Table 3-2).

During a wake-up from an Idle mode, the CPU starts executing code by entering the corresponding Run mode until the primary clock becomes ready. When the primary clock becomes ready, the clock source is automatically switched to the primary clock. The IDLEN and SCS bits are unchanged during and after the wake-up.

Figure 3-2 shows how the system is clocked during the clock source switch. The example assumes the device was in SEC_IDLE or SEC_RUN mode when a wake is triggered (the primary clock was configured in HSPLL mode).

TABLE 3-2: COMPARISON BETWEEN POWER MANAGED MODES

Power Managed Mode	CPU is Clocked by ...	WDT Time-out causes a ...	Peripherals are Clocked by ...	Clock during Wake-up (while primary becomes ready)
Sleep	Not clocked (not running)	Wake-up	Not clocked	None or INTOSC multiplexer if Two-Speed Start-up or Fail-Safe Clock Monitor are enabled
Any Idle mode	Not clocked (not running)	Wake-up	Primary, Secondary or INTOSC multiplexer	Unchanged from Idle mode (CPU operates as in corresponding Run mode)
Any Run mode	Primary or secondary clocks or INTOSC multiplexer	Reset	Primary or secondary clocks or INTOSC multiplexer	Unchanged from Run mode

3.2 Sleep Mode

The power managed Sleep mode in the PIC18F1220/1320 devices is identical to that offered in all other PIC microcontrollers. It is entered by clearing the IDLEN and SCS1:SCS0 bits (this is the Reset state) and executing the `SLEEP` instruction. This shuts down the primary oscillator and the OSTS bit is cleared (see Figure 3-1).

When a wake event occurs in Sleep mode (by interrupt, Reset or WDT time-out), the system will not be clocked until the primary clock source becomes ready (see Figure 3-2), or it will be clocked from the internal oscillator block if either the Two-Speed Start-up or the Fail-Safe Clock Monitor are enabled (see **Section 19.0 "Special Features of the CPU"**). In either case, the OSTS bit is set when the primary clock is providing the system clocks. The IDLEN and SCS bits are not affected by the wake-up.

3.3 Idle Modes

The IDLEN bit allows the microcontroller's CPU to be selectively shut down while the peripherals continue to operate. Clearing IDLEN allows the CPU to be clocked. Setting IDLEN disables clocks to the CPU, effectively stopping program execution (see Register 2-2). The peripherals continue to be clocked regardless of the setting of the IDLEN bit.

There is one exception to how the IDLEN bit functions. When all the low-power OSCCON bits are cleared (IDLEN:SCS1:SCS0 = `000`), the device enters Sleep mode upon the execution of the `SLEEP` instruction. This is both the Reset state of the OSCCON register and the setting that selects Sleep mode. This maintains compatibility with other PIC devices that do not offer power managed modes.

If the Idle Enable bit, IDLEN (OSCCON<7>), is set to a '`1`' when a `SLEEP` instruction is executed, the peripherals will be clocked from the clock source selected using the SCS1:SCS0 bits; however, the CPU will not be clocked. Since the CPU is not executing instructions, the only exits from any of the Idle modes are by interrupt, WDT time-out or a Reset.

When a wake event occurs, CPU execution is delayed approximately 10 μs while it becomes ready to execute code. When the CPU begins executing code, it is clocked by the same clock source as was selected in the power managed mode (i.e., when waking from RC_IDLE mode, the internal oscillator block will clock the CPU and peripherals until the primary clock source becomes ready – this is essentially RC_RUN mode). This continues until the primary clock source becomes ready. When the primary clock becomes ready, the OSTS bit is set and the system clock source is switched to the primary clock (see Figure 3-4). The IDLEN and SCS bits are not affected by the wake-up.

While in any Idle mode or the Sleep mode, a WDT time-out will result in a WDT wake-up to full-power operation.

FIGURE 3-1: TIMING TRANSITION FOR ENTRY TO SLEEP MODE

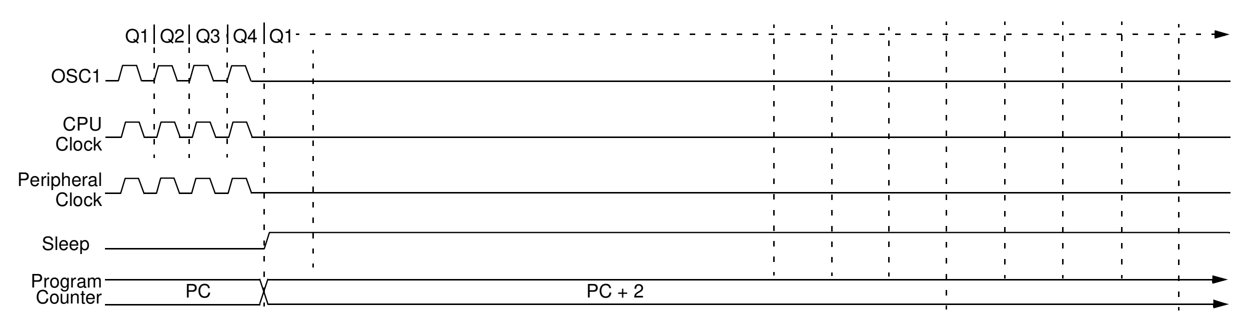
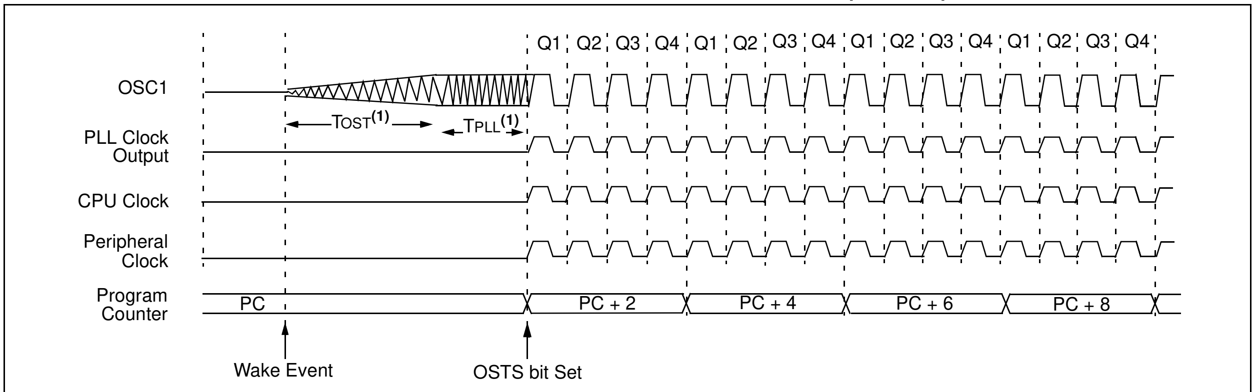


FIGURE 3-2: TRANSITION TIMING FOR WAKE FROM SLEEP (HSPLL)



Note 1: TOST = 1024 TOSC; TPLL = 2 ms (approx). These intervals are not shown to scale.

3.3.1 PRI_IDLE MODE

This mode is unique among the three Low-Power Idle modes, in that it does not disable the primary system clock. For timing sensitive applications, this allows for the fastest resumption of device operation with its more accurate primary clock source, since the clock source does not have to "warm up" or transition from another oscillator.

PRI_IDLE mode is entered by setting the IDLEN bit, clearing the SCS bits and executing a `SLEEP` instruction. Although the CPU is disabled, the peripherals continue to be clocked from the primary clock source specified in Configuration Register 1H. The OSTS bit remains set in PRI_IDLE mode (see Figure 3-3).

When a wake event occurs, the CPU is clocked from the primary clock source. A delay of approximately 10 μs is required between the wake event and code execution starts. This is required to allow the CPU to become ready to execute instructions. After the wake-up, the OSTS bit remains set. The IDLEN and SCS bits are not affected by the wake-up (see Figure 3-4).

FIGURE 3-3: TRANSITION TIMING TO PRI_IDLE MODE

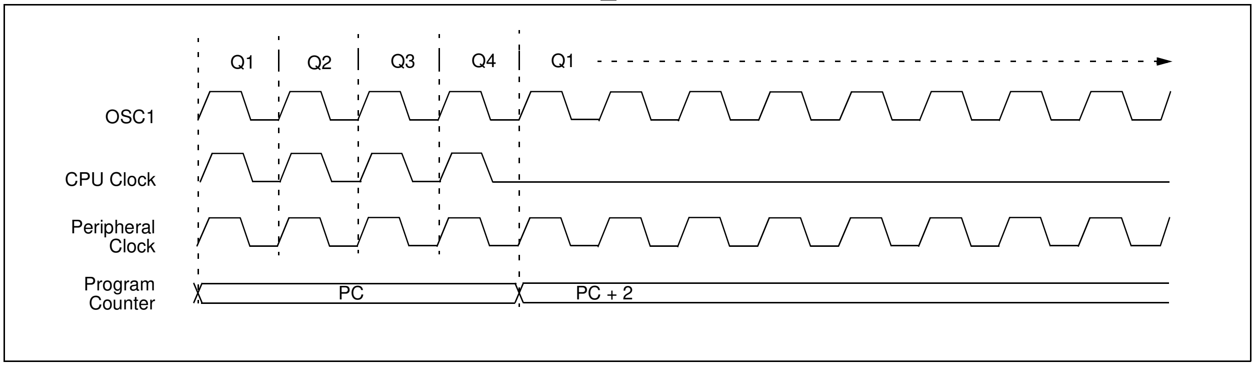
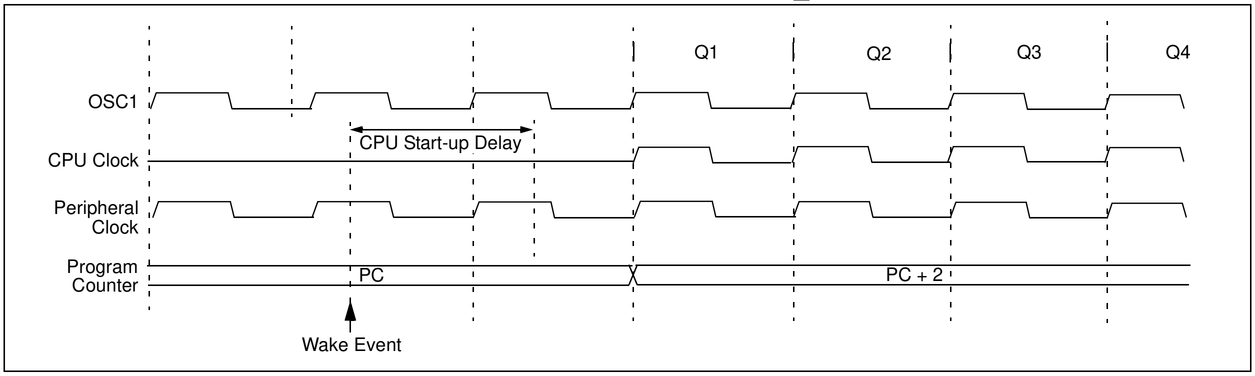


FIGURE 3-4: TRANSITION TIMING FOR WAKE FROM PRI_IDLE MODE



3.3.2 SEC_IDLE MODE

In SEC_IDLE mode, the CPU is disabled, but the peripherals continue to be clocked from the Timer1 oscillator. This mode is entered by setting the Idle bit, modifying bits, SCS1:SCS0 = `01` and executing a `SLEEP` instruction. When the clock source is switched (see Figure 3-5) to the Timer1 oscillator, the primary oscillator is shut down, the OSTS bit is cleared and the T1RUN bit is set.

Note:	The Timer1 oscillator should already be running prior to entering SEC_IDLE mode. If the T1OSCEN bit is not set when the `SLEEP` instruction is executed, the `SLEEP` instruction will be ignored and entry to SEC_IDLE mode will not occur. If the Timer1 oscillator is enabled, but not yet running, peripheral clocks will be delayed until the oscillator has started; in such situations, initial oscillator operation is far from stable and unpredictable operation may result.

When a wake event occurs, the peripherals continue to be clocked from the Timer1 oscillator. After a 10 μs delay following the wake event, the CPU begins executing code, being clocked by the Timer1 oscillator. The microcontroller operates in SEC_RUN mode until the primary clock becomes ready. When the primary clock becomes ready, a clock switchback to the primary clock occurs (see Figure 3-6). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the system clock. The IDLEN and SCS bits are not affected by the wake-up. The Timer1 oscillator continues to run.

FIGURE 3-5: TIMING TRANSITION FOR ENTRY TO SEC_IDLE MODE

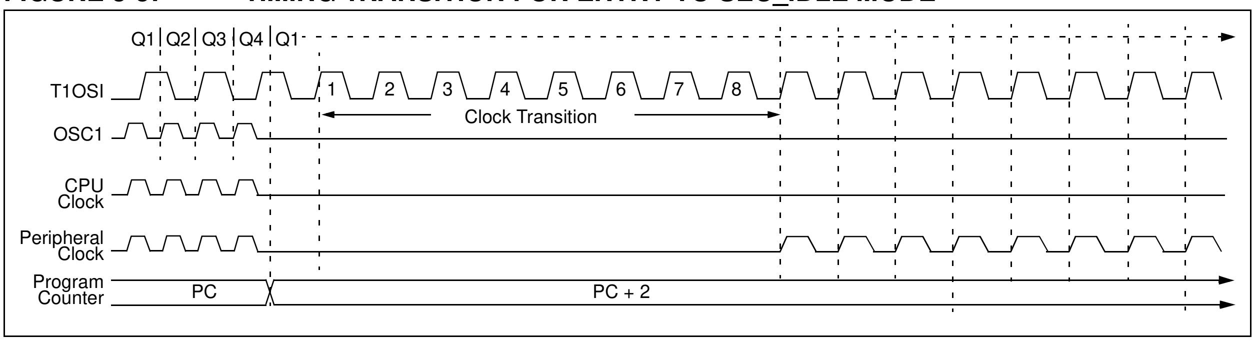
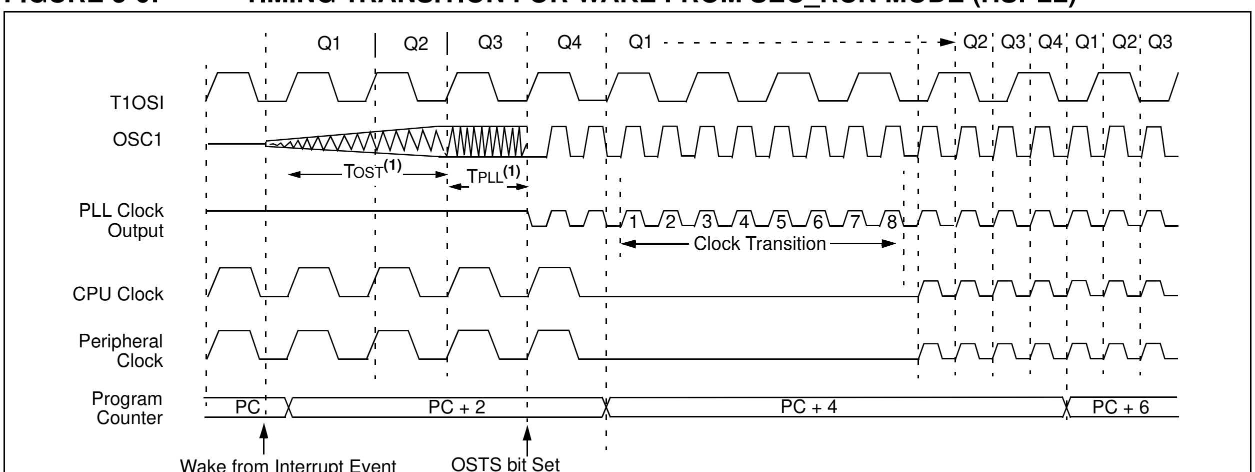


FIGURE 3-6: TIMING TRANSITION FOR WAKE FROM SEC_RUN MODE (HSPLL)



Note 1: T_{OST} = 1024 T_{OSC}; T_{PLL} = 2 ms (approx). These intervals are not shown to scale.

3.3.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled, but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode allows for controllable power conservation during Idle periods.

This mode is entered by setting the IDLEN bit, setting SCS1 (SCS0 is ignored) and executing a `SLEEP` instruction. The INTOSC multiplexer may be used to select a higher clock frequency by modifying the IRCF bits before executing the `SLEEP` instruction. When the clock source is switched to the INTOSC multiplexer (see Figure 3-7), the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to a non-zero value (thus, enabling the INTOSC output), the IOFS bit becomes set after the INTOSC output becomes stable, in about 1 ms. Clocks to the peripherals continue while the INTOSC source stabilizes. If the IRCF bits were previously at a non-zero value before the `SLEEP` instruction was executed and the INTOSC source was already stable, the IOFS bit will remain set. If the IRCF bits are all clear, the INTOSC output is not enabled and the IOFS bit will remain clear; there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a 10 μs delay following the wake event, the CPU begins executing code, being clocked by the INTOSC multiplexer. The microcontroller operates in RC_RUN mode until the primary clock becomes ready. When the primary clock becomes ready, a clock switchback to the primary clock occurs (see Figure 3-8). When the clock switch is complete, the IOFS bit is cleared, the OSTS bit is set and the primary clock is providing the system clock. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

FIGURE 3-7: TIMING TRANSITION TO RC_IDLE MODE

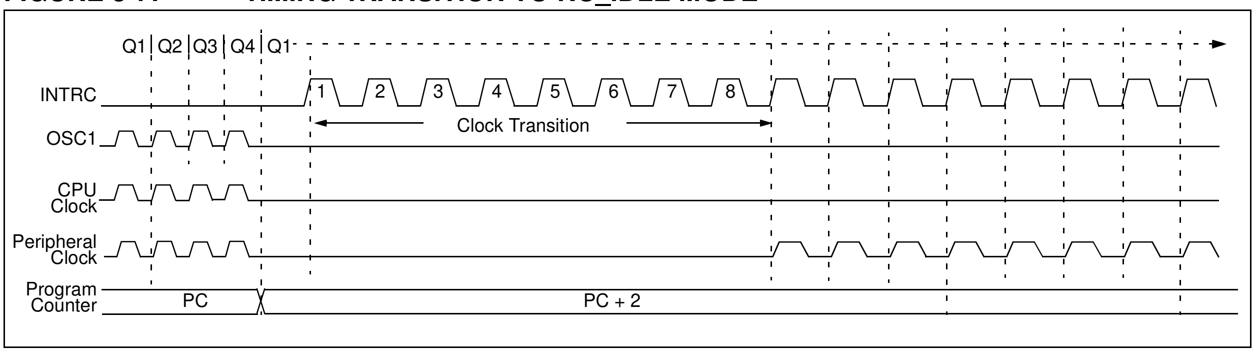
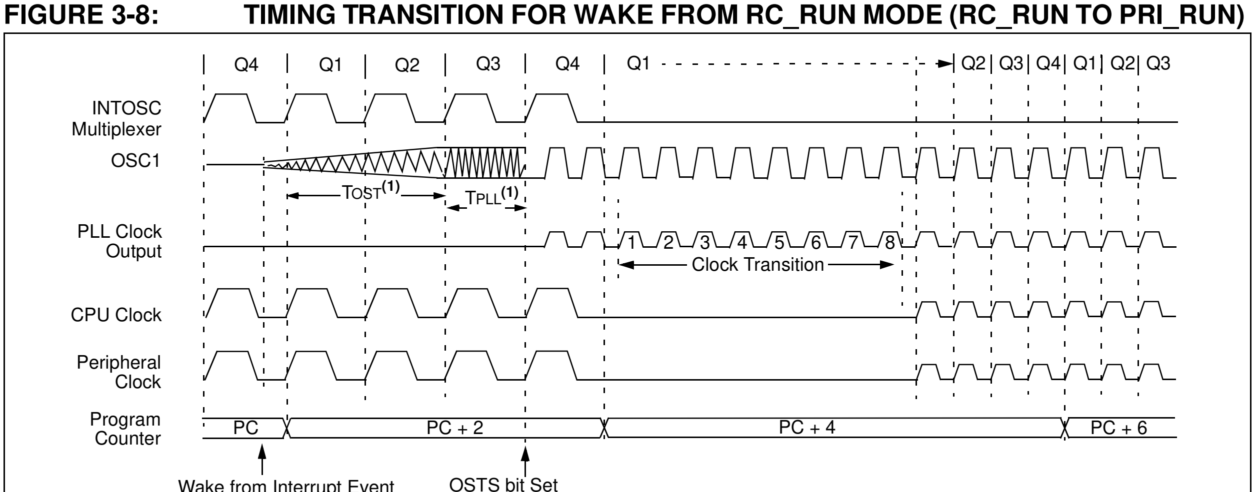


FIGURE 3-8: TIMING TRANSITION FOR WAKE FROM RC_RUN MODE (RC_RUN TO PRI_RUN)



Note 1: T_{OST} = 1024 T_{OSC}; T_{PLL} = 2 ms (approx). These intervals are not shown to scale.

3.4 Run Modes

If the IDLEN bit is clear when a `SLEEP` instruction is executed, the CPU and peripherals are both clocked from the source selected using the SCS1:SCS0 bits. While these operating modes may not afford the power conservation of Idle or Sleep modes, they do allow the device to continue executing instructions by using a lower frequency clock source. RC_RUN mode also offers the possibility of executing code at a frequency greater than the primary clock.

Wake-up from a power managed Run mode can be triggered by an interrupt, or any Reset, to return to full-power operation. As the CPU is executing code in Run modes, several additional exits from Run modes are possible. They include exit to Sleep mode, exit to a corresponding Idle mode and exit by executing a `RESET` instruction. While the device is in any of the power managed Run modes, a WDT time-out will result in a WDT Reset.

3.4.1 PRI_RUN MODE

The PRI_RUN mode is the normal full-power execution mode. If the `SLEEP` instruction is never executed, the microcontroller operates in this mode (a `SLEEP` instruction is executed to enter all other power managed modes). All other power managed modes exit to PRI_RUN mode when an interrupt or WDT time-out occur.

There is no entry to PRI_RUN mode. The OSTS bit is set. The IOFS bit may be set if the internal oscillator block is the primary clock source (see **Section 2.7.1 "Oscillator Control Register"**).

3.4.2 SEC_RUN MODE

The SEC_RUN mode is the compatible mode to the "clock switching" feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high accuracy clock source.

SEC_RUN mode is entered by clearing the IDLEN bit, setting SCS1:SCS0 = `01` and executing a `SLEEP` instruction. The system clock source is switched to the Timer1 oscillator (see Figure 3-9), the primary oscillator is shut down, the T1RUN bit (T1CON<6>) is set and the OSTS bit is cleared.

Note:	The Timer1 oscillator should already be running prior to entering SEC_RUN mode. If the T1OSCEN bit is not set when the `SLEEP` instruction is executed, the `SLEEP` instruction will be ignored and entry to SEC_RUN mode will not occur. If the Timer1 oscillator is enabled, but not yet running, system clocks will be delayed until the oscillator has started; in such situations, initial oscillator operation is far from stable and unpredictable operation may result.

When a wake event occurs, the peripherals and CPU continue to be clocked from the Timer1 oscillator while the primary clock is started. When the primary clock becomes ready, a clock switchback to the primary clock occurs (see Figure 3-6). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the system clock. The IDLEN and SCS bits are not affected by the wake-up. The Timer1 oscillator continues to run.

Firmware can force an exit from SEC_RUN mode. By clearing the T1OSCEN bit (T1CON<3>), an exit from SEC_RUN back to normal full-power operation is triggered. The Timer1 oscillator will continue to run and provide the system clock, even though the T1OSCEN bit is cleared. The primary clock is started. When the primary clock becomes ready, a clock switchback to the primary clock occurs (see Figure 3-6). When the clock switch is complete, the Timer1 oscillator is disabled, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the system clock. The IDLEN and SCS bits are not affected by the wake-up.

FIGURE 3-9: TIMING TRANSITION FOR ENTRY TO SEC_RUN MODE