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PIC18(L)F1XK50

20-Pin USB Flash Microcontrollers with XLP Technology

Universal Serial Bus Features

- USB V2.0 Compliant SIE
- Full Speed (12 Mb/s) and Low Speed (1.5 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 16 Endpoints (8 bidirectional)
- 256-byte Dual Access RAM for USB
- Input-Change Interrupt on D+/D- for Detecting Physical Connection to USB Host

High-Performance RISC CPU

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
  - 256 bytes, data EEPROM
  - Up to 16 Kbytes linear program memory addressing
  - Up to 768 bytes linear data memory addressing
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier

Flexible Oscillator Structure

- CPU Divider to Run the Core Slower than the USB Peripheral
- 16 MHz Internal Oscillator Block:
  - Software selectable frequencies, 31 kHz to 16 MHz
  - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
  - User tunable to compensate for frequency drift
- Four Crystal modes, up to 48 MHz
- External Clock modes, up to 48 MHz
- 4X Phase Lock Loop (PLL)
- Secondary Oscillator using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if primary or secondary oscillator stops
- Two-Speed Oscillator Start-Up

Special Microcontroller Features

- Full 5.5V Operation – PIC18F1XK50
- 1.8V-3.6V Operation – PIC18LF1XK50
- Self-Programmable under Software Control
- Programmable Brown-out Reset (BOR):
  - With software enable option
- Extended Watchdog Timer (WDT):
  - Programmable period from 4ms to 131s
- Single-Supply 3V In-Circuit Serial Programming™ (ICSP™) via Two Pins

Extreme Low-Power Management PIC18LF1XK50 with XLP Technology

- Sleep mode: 24 nA
- Watchdog Timer: 450 nA
- Timer1 Oscillator: 790 nA @ 32 kHz

Analog Features

- Analog-to-Digital Converter (ADC) module:
  - 10-bit resolution, nine external channels
  - Auto acquisition capability
  - Conversion available during Sleep
  - Internal 1.024V Fixed Voltage Reference (FVR) channel
  - Independent input multiplexing
- Dual Analog Comparators:
  - Rail-to-rail operation
  - Independent input multiplexing
- Voltage Reference module:
  - Programmable (% of V_{DD}), 16 steps
  - Two 16-level voltage ranges using V_{REF} pins
  - Programmable Fixed Voltage Reference (FVR), 3 levels
- On-Chip 3.2V LDO Regulator – PIC18F1XK50

Peripheral Highlights

- 14 I/O Pins plus 1 Input-Only Pin:
  - High-current sink/source 25 mA/25 mA
  - Seven programmable weak pull-ups
  - Seven programmable interrupt-on-change pins
  - Three programmable external interrupts
  - Programmable slew rate
- Enhanced Capture/Compare/PWM (ECCP) module:
  - One, two, three, or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and Auto-restart
- Master Synchronous Serial Port (MSSP) module:
  - 3-wire SPI (supports all four modes)
  - I^2C™ Master and Slave modes (Slave mode address masking)
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module:
  - Supports RS-485, RS-232 and LIN 2.0
  - RS-232 operation using internal oscillator
  - Auto-Baud Detect
  - Auto-Wake-up on Break
- SR Latch mode

PIC18(L)F1XK50 Family Types

Device	Data Sheet Index	Program Memory		Data Memory		I/O(1)	10-bit A/D (ch)(2)	ECCP (PWM)	MSSP		EUSART	Comp.	Timers 8/16-bit	USB
		Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I²C™				
PIC18F13K50/ PIC18LF13K50	(A)	8K	4096	512(3)	256	15	11	1	Y	Y	1	2	1/3	Y
PIC18F14K50/ PIC18LF14K50	(A)	16K	8192	768(3)	256	15	11	1	Y	Y	1	2	1/3	Y

Note 1: One pin is input only.

2: Channel count includes internal Fixed Voltage Reference (FVR) and Programmable Voltage Reference (CV_{REF}) channels.

3: Includes the dual port RAM used by the USB module which is shared with the data memory.

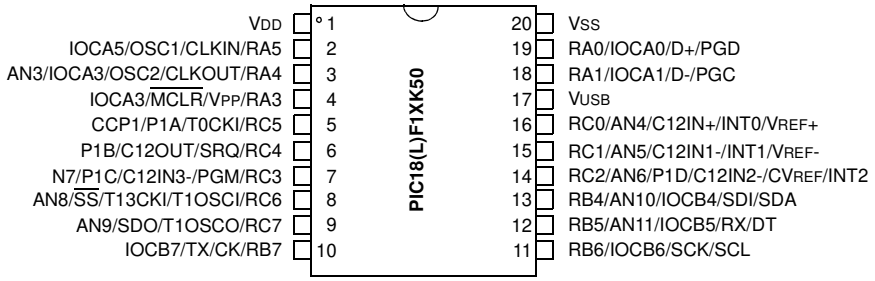
Data Sheet Index: (Unshaded devices are described in this document)

A. DS40001350 PIC18(L)F1XK50 Data Sheet, 20-Pin USB Flash Microcontrollers with XLP Technology.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

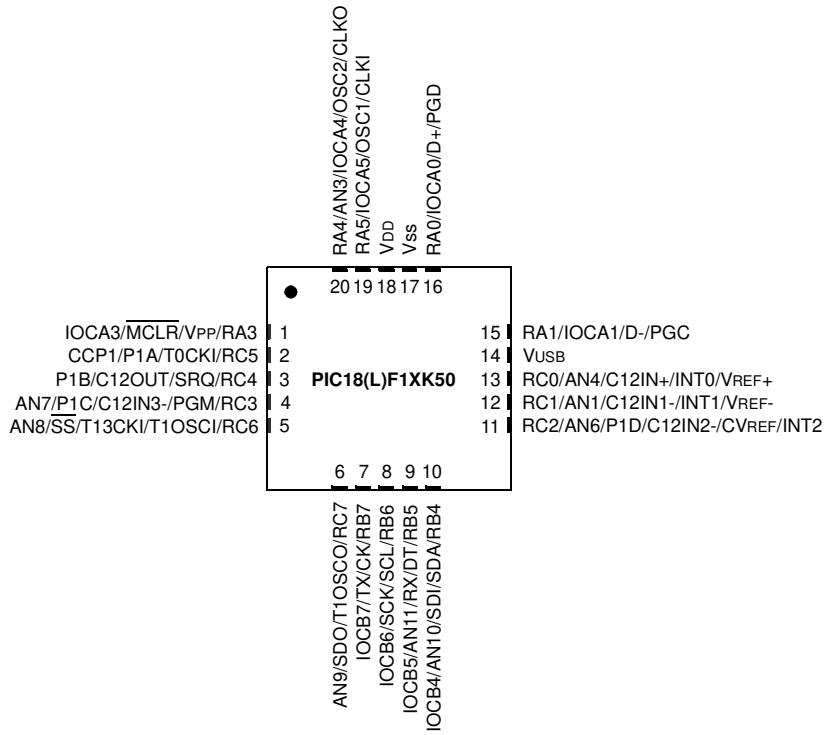
Pin Diagrams

FIGURE 1: 20-PIN PDIP, SSOP, SOIC (300 MIL)



Note: See Table 1 for location of all peripheral functions.

FIGURE 2: 20-PIN QFN (5X5)



Note: See Table 1 for location of all peripheral functions.

TABLE 1: 20-PIN ALLOCATION TABLE (PIC18(L)F1XK50)

I/O	20-Pin PDIP/SSOP/SOIC	20-Pin QFN	Analog	Comparator	Reference	ECCP	EUSART	MSSP	Timers	Interrupts	Pull-up	USB	Basic
RA0	19	16	—	—	—	—	—	—	—	IOCA0	—	D+	PGD
RA1	18	15	—	—	—	—	—	—	—	IOCA1	—	D-	PGC
RA3(1)	4	1	—	—	—	—	—	—	—	IOCA3	Y	—	$\overline{MCLR}$/VPP
RA4	3	20	AN3	—	—	—	—	—	—	IOCA4	Y	—	OSC2/CLKOUT
RA5	2	19	—	—	—	—	—	—	—	IOCA5	Y	—	OSC1/CLKIN
RB4	13	10	AN10	—	—	—	—	SDI/SDA	—	IOCB4	Y	—	—
RB5	12	9	AN11	—	—	—	RX/DT	—	—	IOCB5	Y	—	—
RB6	11	8	—	—	—	—	—	SCL/SCK	—	IOCB6	Y	—	—
RB7	10	7	—	—	—	—	TX/CK	—	—	IOCB7	Y	—	—
RC0	16	13	AN4	C12IN+	VREF+	—	—	—	—	INT0	—	—	—
RC1	15	12	AN5	C12IN1-	VREF-	—	—	—	—	INT1		—	—
RC2	14	11	AN6	C12IN2-	CVREF	P1D	—	—	—	INT2	—	—	—
RC3	7	4	AN7	C12IN3-	—	P1C	—	—	—	—	—	—	PGM
RC4	6	3	—	C12OUT	—	P1B	—	—	—	—	—	—	SRQ
RC5	5	2	—	—	—	CCP1/P1A	—	—	T0CKI	—	—	—	—
RC6	8	5	AN8	—	—	—	—	$\overline{SS}$	T13CKI/T1OSCI	—	—	—	—
RC7	9	6	AN9	—	—	—	—	SDO	T1OSCO	—	—	—	—
VUSB	17	14	—	—	—	—	—	—	—	—	—	VUSB	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

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1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F13K50
- PIC18F14K50
- PIC18LF13K50
- PIC18LF14K50

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Flash program memory. On top of these features, the PIC18(L)F1XK50 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 XLP TECHNOLOGY

All of the devices in the PIC18(L)F1XK50 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 27.0 "Electrical Specifications"** for values.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18(L)F1XK50 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators
- External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O)
- External RC Oscillator modes with the same pin options as the External Clock modes
- An internal oscillator block which contains a 16 MHz HFINTOSC oscillator and a 31 kHz LFINTOSC oscillator which together provide 8 user selectable clock frequencies, from 31 kHz to 16 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the high-speed crystal and internal oscillator modes, which allows clock speeds of up to 48 MHz. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 32 MHz – all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the LFINTOSC. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.2 Other Special Features

- **Memory Endurance:** The Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 1K for program memory and 100K for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-programmability:** These devices can write to their own program memory spaces under internal software control. Using a bootloader routine located in the code protected Boot Block, it is possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18(L)F1XK50 family introduces an optional extension to the PIC18 instruction set, which adds eight new instructions and an Indexed Addressing mode. This extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- **Enhanced CCP module:** In PWM mode, this module provides 1, 2 or 4 modulated outputs for controlling half-bridge and full-bridge drivers. Other features include:
  - Auto-Shutdown, for disabling PWM outputs on interrupt or other select conditions
  - Auto-Restart, to reactivate outputs once the condition has cleared
  - Output steering to selectively enable one or more of four outputs to provide the PWM signal.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution.
- **10-bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit postscaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 27.0 "Electrical Specifications"** for time-out periods.

1.3 Details on Individual Family Members

Devices in the PIC18(L)F1XK50 family are available in 20-pin packages. Block diagrams for the two groups are shown in Figure 1-1.

The devices are differentiated from each other in the following ways:

1. Flash program memory:
   - 8 Kbytes for PIC18F13K50/PIC18LF13K50
   - 16 Kbytes for PIC18F14K50/PIC18LF14K50
2. On-chip 3.2V LDO regulator for PIC18F13K50 and PIC18F14K50.

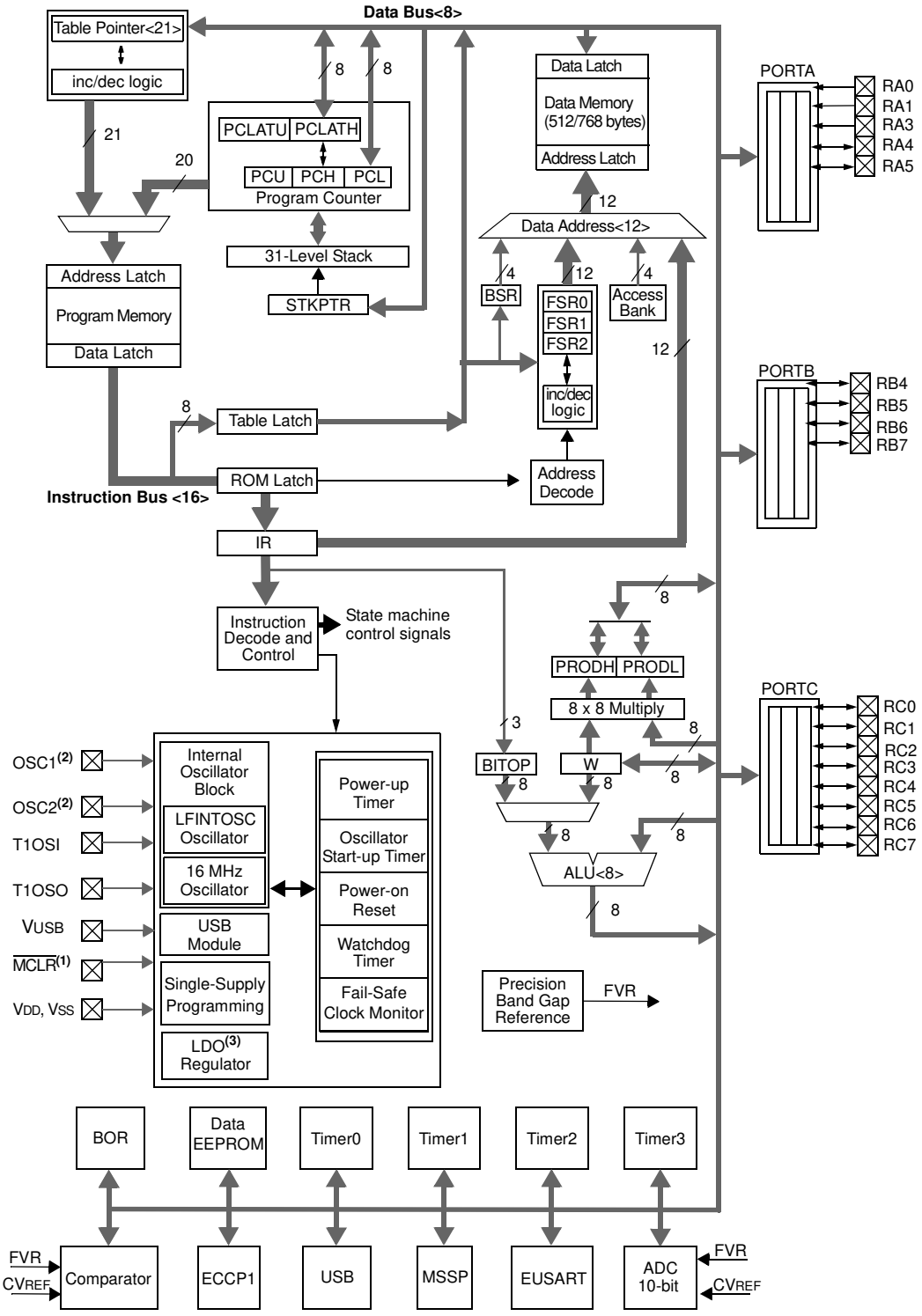
All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1 and I/O description are in Table 1-2.

TABLE 1-1: DEVICE FEATURES FOR THE PIC18(L)F1XK50 (20-PIN DEVICES)

Features	PIC18F13K50	PIC18LF13K50	PIC18F14K50	PIC18LF14K50
LDO Regulator	Yes	No	Yes	No
Program Memory (Bytes)	8K		16K	
Program Memory (Instructions)	4096		8192	
Data Memory (Bytes)	512		768	
Operating Frequency	DC – 48 MHz			
Interrupt Sources	30			
I/O Ports	Ports A, B, C			
Timers	4			
Enhanced Capture/ Compare/PWM Modules	1			
Serial Communications	MSSP, Enhanced USART, USB			
10-Bit Analog-to-Digital Module	9 Input Channels			
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)			
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled			
Packages	20-Pin PDIP, SSOP, SOIC (300 mil) and QFN (5x5)			

FIGURE 1-1: PIC18(L)F1XK50 BLOCK DIAGRAM



Note 1: RA3 is only available when $\overline{MCLR}$ functionality is disabled.

2: OSC1/CLKIN and OSC2/CLKOUT are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Module"** for additional information.

3: PIC18F13K50/PIC18F14K50 only.

TABLE 1-2: PIC18(L)F1XK50 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
RA0/D+/PGD	19			
RA0		I	TTL	Digital input
D+		I/O	XCVR	USB differential plus line (input/output)
PGD		I/O	ST	ICSP™ programming data pin
RA1/D-/PGC	18			
RA1		I	TTL	Digital input
D-		I/O	XCVR	USB differential minus line (input/output)
PGC		I/O	ST	ICSP™ programming clock pin
RA3/$\overline{MCLR}$/VPP	4			Master Clear (input) or programming voltage (input)
RA3		I	ST	Digital input
$\overline{MCLR}$		I	ST	Active-low Master Clear with internal pull-up
VPP		P	—	High voltage programming input
RA4/AN3/OSC2/CLKOUT	3			
RA4		I/O	TTL	Digital I/O
AN3		I	Analog	ADC channel 3
OSC2		O	XTAL	Oscillator crystal output. Connect to crystal or resonator in Crystal Oscillator mode
CLKOUT		O	CMOS	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate
RA5/OSC1/CLKIN	2			
RA5		I/O	TTL	Digital I/O
OSC1		I	XTAL	Oscillator crystal input or external clock input ST buffer when configured in RC mode; analog other wise
CLKIN		I	CMOS	External clock source input. Always associated with the pin function OSC1 (See related OSC1/CLKIN, OSC2, CLKOUT pins
RB4/AN10/SDI/SDA	13			
RB4		I/O	TTL	Digital I/O
AN10		I	Analog	ADC channel 10
SDI		I	ST	SPI data in
SDA		I/O	ST	I^2C™ data I/O
RB5/AN11/RX/DT	12			
RB5		I/O	TLL	Digital I/O
AN11		I	Analog	ADC channel 11
RX		I	ST	EUSART asynchronous receive
DT		I/O	ST	EUSART synchronous data (see related RX/TX)
RB6/SCK/SCI	11			
RB6		I/O	TLL	Digital I/O
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode
SCI		I/O	ST	Synchronous serial clock input/output for I^2C™ mode
RB7/TX/CK	10			
RB7		I/O	TLL	Digital I/O
TX		O	CMOS	EUSART asynchronous transmit
CK		I/O	ST	EUSART synchronous clock (see related RX/DT)

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input
O = Output
XTAL= Crystal Oscillator
CMOS = CMOS compatible input or output
I = Input
P = Power
XCVR = USB Differential Transceiver

TABLE 1-2: PIC18(L)F1XK50 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
RC0/AN4/C12IN+/INT0/VREF+	16			
RC0		I/O	ST	Digital I/O
AN4		I	Analog	ADC channel 4
C12IN+		I	Analog	Comparator C1 and C2 non-inverting input
INT0		I	ST	External interrupt 0
VREF+		I	Analog	Comparator reference voltage (high) input
RC1/AN5/C12IN-/INT1/VREF-	15			
RC1		I/O	ST	Digital I/O
AN5		I	Analog	ADC channel 5
C12IN-		I	Analog	Comparator C1 and C2 non-inverting input
INT1		I	ST	External interrupt 0
VREF-		I	Analog	Comparator reference voltage (low) input
RC2/AN6/P1D/C12IN2-/CVREF/INT2	14			
RC2		I/O	ST	Digital I/O
AN6		I	Analog	ADC channel 6
P1D		O	CMOS	Enhanced CCP1 PWM output
C12IN2-		I	Analog	Comparator C1 and C2 inverting input
CVREF		O	Analog	Comparator reference voltage output
INT2		I	ST	External interrupt 0
RC3/AN7/P1C/C12IN3-/PGM	7			
RC3		I/O	ST	Digital I/O
AN7		I	Analog	ADC channel 7
P1C		O	CMOS	Enhanced CCP1 PWM output
C12IN3-		I	Analog	Comparator C1 and C2 inverting input
PGM		I/O	ST	Low-Voltage ICSP Programming enable pin
RC4/P1B/C12OUT/SRQ	6			
RC4		I/O	ST	Digital I/O
P1B		O	CMOS	Enhanced CCP1 PWM output
C12OUT		O	CMOS	Comparator C1 and C2 output
SRQ		O	CMOS	SR Latch output
RC5/CCP1/P1A/T0CKI	5			
RC5		I/O	ST	Digital I/O
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output
P1A		O	CMOS	Enhanced CCP1 PWM output
T0CKI		I	ST	Timer0 external clock input
RC6/AN8/$\overline{SS}$/T13CKI/T1OSCI	8			
RC6		I/O	ST	Digital I/O
AN8		I	Analog	ADC channel 8
$\overline{SS}$		I	TTL	SPI slave select input
T13CKI		I	ST	Timer0 and Timer3 external clock input
T1OSCI		I	XTAL	Timer1 oscillator input
RC7/AN9/SDO/T1OSCO	9			
RC7		I/O	ST	Digital I/O
AN9		I	Analog	ADC channel 9
SDO		O	CMOS	SPI data out
T1OSCO		O	XTAL	Timer1 oscillator output
VSS	20	P	—	Ground reference for logic and I/O pins
VDD	1	P	—	Positive supply for logic and I/O pins
VUSB	17	P	—	Positive supply for USB transceiver

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input
O = Output
XTAL= Crystal Oscillator
CMOS = CMOS compatible input or output
I = Input
P = Power
XCVR = USB Differential Transceiver

2.0 OSCILLATOR MODULE

2.1 Overview

The oscillator module has a variety of clock sources and features that allow it to be used in a wide range of applications, maximizing performance and minimizing power consumption. Figure 2-1 illustrates a block diagram of the oscillator module.

Key features of the oscillator module include:

- System Clock Selection
  - Primary External Oscillator
  - Secondary External Oscillator
  - Internal Oscillator
- Oscillator Start-up Timer
- System Clock Selection
- Clock Switching
- 4x Phase Lock Loop Frequency Multiplier
- CPU Clock Divider
- USB Operation
  - Low-Speed
  - Full-Speed
- Two-Speed Start-up Mode
- Fail-Safe Clock Monitoring

2.2 System Clock Selection

The SCS bits of the OSCCON register select between the following clock sources:

- Primary External Oscillator
- Secondary External Oscillator
- Internal Oscillator

Note: The frequency of the system clock will be referred to as FOSC throughout this document.

TABLE 2-1: SYSTEM CLOCK SELECTION

Configuration	Selection
SCS <1:0>	System Clock
1x	Internal Oscillator
01	Secondary External Oscillator
00 (Default after Reset)	Oscillator defined by FOSC<3:0>

The default state of the SCS bits sets the system clock to be the oscillator defined by the FOSC bits of the CONFIG1H Configuration register. The system clock will always be defined by the FOSC bits until the SCS bits are modified in software.

When the Internal Oscillator is selected as the system clock, the IRCF bits of the OSCCON register and the INTSRC bit of the OSCTUNE register will select either the LFINTOSC or the HFINTOSC. The LFINTOSC is selected when the IRCF<2:0> = 000 and the INTSRC bit is clear. All other combinations of the IRCF bits and the INTSRC bit will select the HFINTOSC as the system clock.

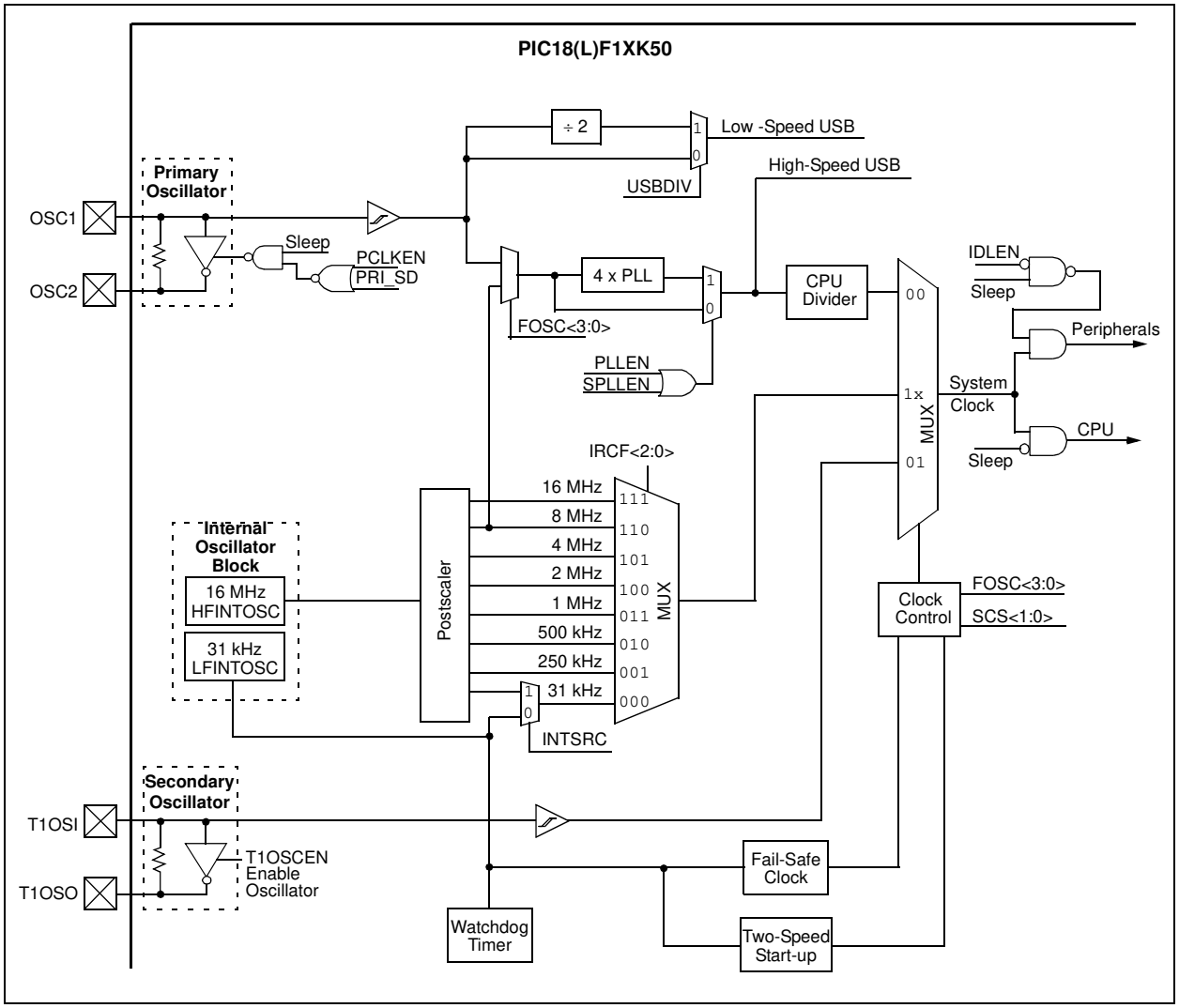
2.3 Primary External Oscillator

The Primary External Oscillator's mode of operation is selected by setting the FOSC<3:0> bits of the CONFIG1H Configuration register. The oscillator can be set to the following modes:

- LP: Low-Power Crystal
- XT: Crystal/Ceramic Resonator
- HS: High-Speed Crystal Resonator
- RC: External RC Oscillator
- EC: External Clock

Additionally, the Primary External Oscillator may be shut down under firmware control to save power.

FIGURE 2-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



2.3.1 PRIMARY EXTERNAL OSCILLATOR SHUTDOWN

The Primary External Oscillator can be enabled or disabled via software. To enable software control of the Primary External Oscillator, the PCLKEN bit of the CONFIG1H Configuration register must be set. With the PCLKEN bit set, the Primary External Oscillator is controlled by the PRI_SD bit of the OSCCON2 register. The Primary External Oscillator will be enabled when the PRI_SD bit is set, and disabled when the PRI_SD bit is clear.

Note:	The Primary External Oscillator cannot be shut down when it is selected as the System Clock. To shut down the oscillator, the system clock source must be either the Secondary Oscillator or the Internal Oscillator.

2.3.2 LP, XT AND HS OSCILLATOR MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 2-2). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

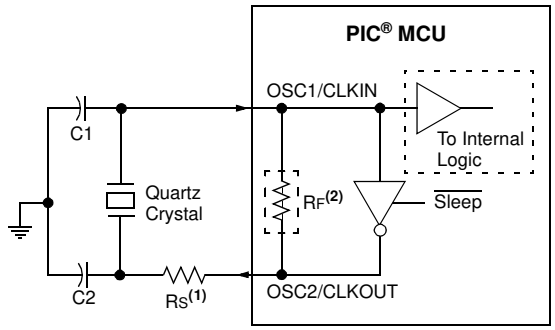
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 2-2 and Figure 2-3 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 2-2: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)

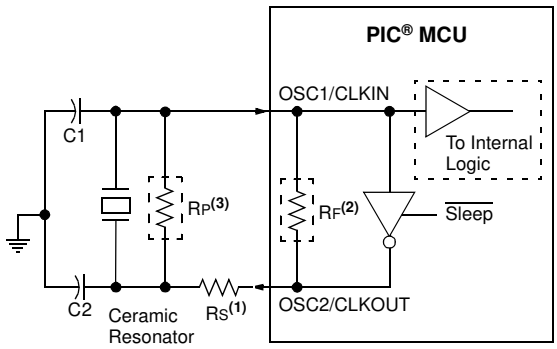


Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Note 1:	Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
2:	Always verify oscillator performance over the VDD and temperature range that is expected for the application.
3:	For oscillator design assistance, reference the following Microchip Applications Notes: • AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826) • AN849, "*Basic PIC® Oscillator Design*" (DS00849) • AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943) • AN949, "*Making Your Oscillator Work*" (DS00949)

FIGURE 2-3: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

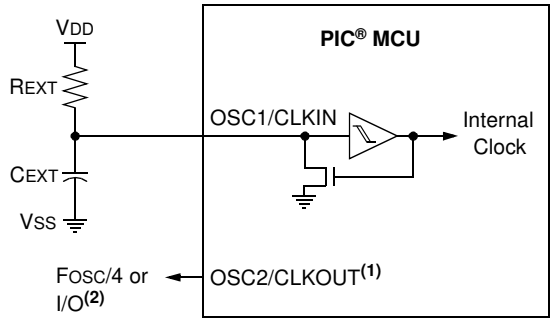
2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

2.3.3 EXTERNAL RC

The External Resistor-Capacitor (RC) mode supports the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. In RC mode, the RC circuit connects to OSC1, allowing OSC2 to be configured as an IO or as CLKOUT. The CLKOUT function is selected by the FOSC bits of the CONFIG1H Configuration register. When OSC2 is configured as CLKOUT, the frequency at the pin is the frequency of the RC oscillator divided by 4. Figure 2-4 shows the external RC mode connections.

FIGURE 2-4: EXTERNAL RC MODES



Recommended values: 10 kΩ ≤ REXT ≤ 100 kΩ
CEXT > 20 pF

Note 1: Alternate pin functions are listed in **Section 1.0 "Device Overview"**.

2: Output depends upon RC or RCIO clock mode.

The RC oscillator frequency is a function of the supply voltage, the resistor REXT, the capacitor CEXT and the operating temperature. Other factors affecting the oscillator frequency are:

- Input threshold voltage variation
- Component tolerances
- Variation in capacitance due to packaging

2.3.4 EXTERNAL CLOCK

The External Clock (EC) mode allows an externally generated logic level clock to be used as the system's clock source. When operating in this mode, the external clock source is connected to the OSC1 allowing OSC2 to be configured as an I/O or as CLKOUT. The CLKOUT function is selected by the FOSC bits of the CONFIG1H Configuration register. When OSC2 is configured as CLKOUT, the frequency at the pin is the frequency of the EC oscillator divided by 4.

Three different power settings are available for EC mode. The power settings allow for a reduced IDD of the device, if the EC clock is known to be in a specific range. If there is an expected range of frequencies for the EC clock, select the power mode for the highest frequency.

EC	Low power	0 – 250 kHz
EC	Medium power	250 kHz – 4 MHz
EC	High power	4 – 48 MHz

2.4 Secondary External Oscillator

The Secondary External Oscillator is designed to drive an external 32.768 kHz crystal. This oscillator is enabled or disabled by the T1OSCEN bit of the T1CON register. See **Section 11.0 "Timer1 Module"** for more information.

2.5 Internal Oscillator

The internal oscillator module contains two independent oscillators which are:

- LFINTOSC: Low-Frequency Internal Oscillator
- HFINTOSC: High-Frequency Internal Oscillator

When operating with either oscillator, OSC1 will be an I/O and OSC2 will be either an I/O or CLKOUT. The CLKOUT function is selected by the FOSC bits of the CONFIG1H Configuration register. When OSC2 is configured as CLKOUT, the frequency at the pin is the frequency of the Internal Oscillator divided by 4.

2.5.1 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is a 31 kHz internal clock source. The LFINTOSC oscillator is the clock source for:

- Power-up Timer
- Watchdog Timer
- Fail-Safe Clock Monitor

The LFINTOSC is enabled when any of the following conditions are true:

- Power-up Timer is enabled (PWRTEN = 0)
- Watchdog Timer is enabled (WDTEN = 1)
- Watchdog Timer is enabled by software (WDTEN = 0 and SWDTEN = 1)
- Fail-Safe Clock Monitor is enabled (FCMEM = 1)
- SCS1 = 1 and IRCF<2:0> = 000 and INTSRC = 0
- FOSC<3:0> selects the internal oscillator as the primary clock and IRCF<2:0> = 000 and INTSRC = 0
- IESO = 1 (Two-Speed Start-up) and IRCF<2:0> = 000 and INTSRC = 0

2.5.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a precision oscillator that is factory-calibrated to operate at 16 MHz. The output of the HFINTOSC connects to a postscaler and a multiplexer (see Figure 2-1). One of eight frequencies can be selected using the IRCF<2:0> bits of the OSCCON register. The following frequencies are available from the HFINTOSC:

- 16 MHZ
- 8 MHZ
- 4 MHZ
- 2 MHZ
- 1 MHZ (Default after Reset)
- 500 kHz
- 250 kHz
- 31 kHz

The HFIOFS bit of the OSCCON register indicates whether the HFINTOSC is stable.

Note 1: Selecting 31 kHz from the HFINTOSC oscillator requires IRCF<2:0> = 000 and the INTSRC bit of the OSCTUNE register to be set. If the INTSRC bit is clear, the system clock will come from the LFINTOSC.

2: Additional adjustments to the frequency of the HFINTOSC can made via the OSCTUNE registers. See Register 2-3 for more details

The HFINTOSC is enabled if any of the following conditions are true:

- SCS1 = 1 and IRCF<2:0> ≠ 000
- SCS1 = 1 and IRCF<2:0> = 000 and INTSRC = 1
- FOSC<3:0> selects the internal oscillator as the primary clock and
  - IRCF<2:0> ≠ 000 or
  - IRCF<2:0> = 000 and INTSRC = 1
- IESO = 1 (Two-Speed Start-up) and
  - IRCF<2:0> ≠ 000 or
  - IRCF<2:0> = 000 and INTSRC = 1
- FCMEM = 1 (Fail Safe Clock Monitoring) and
  - IRCF<2:0> ≠ 000 or
  - IRCF<2:0> = 000 and INTSRC = 1

2.6 Oscillator Control

The Oscillator Control (OSCCON) (Register 2-1) and the Oscillator Control 2 (OSCCON2) (Register 2-2) registers control the system clock and frequency selection options.

REGISTER 2-1: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R-q	R-0	R/W-0	R/W-0
IDLEN	IRCF2	IRCF1	IRCF0	OSTS(1)	HFIOFS	SCS1	SCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	q = depends on condition
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IDLEN:** Idle Enable bit
1 = Device enters Idle mode on SLEEP instruction
0 = Device enters Sleep mode on SLEEP instruction

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits
111 = 16 MHz
110 = 8 MHz
101 = 4 MHz
100 = 2 MHz
011 = 1 MHz(3)
010 = 500 kHz
001 = 250 kHz
000 = 31 kHz(2)

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit(1)
1 = Device is running from the clock defined by FOSC<2:0> of the CONFIG1 register
0 = Device is running from the internal oscillator (HFINTOSC or LFINTOSC)

bit 2 **HFIOFS:** HFINTOSC Frequency Stable bit
1 = HFINTOSC frequency is stable
0 = HFINTOSC frequency is not stable

bit 1-0 **SCS<1:0>:** System Clock Select bits
1x = Internal oscillator block
01 = Secondary (Timer1) oscillator
00 = Primary clock (determined by CONFIG1H[FOSC<3:0>]).

Note 1: Reset state depends on state of the IESO Configuration bit.
2: Source selected by the INTSRC bit of the OSCTUNE register, see text.
3: Default output frequency of HFINTOSC on Reset.

REGISTER 2-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R-x
—	—	—	—	—	PRI_SD	HFIOFL	LFIOFS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	q = depends on condition
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **PRI_SD:** Primary Oscillator Drive Circuit shutdown bit
1 = Oscillator drive circuit on
0 = Oscillator drive circuit off (zero power)

bit 1 **HFIOFL:** HFINTOSC Frequency Locked bit
1 = HFINTOSC is in lock
0 = HFINTOSC has not yet locked

bit 0 **LFIOFS:** LFINTOSC Frequency Stable bit
1 = LFINTOSC is stable
0 = LFINTOSC is not stable

2.6.1 OSCTUNE REGISTER

The HFINTOSC is factory calibrated, but can be adjusted in software by writing to the TUN<5:0> bits of the OSCTUNE register (Register 2-3).

The default value of the TUN<5:0> is '000000'. The value is a 6-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift, while giving no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. The operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

The OSCTUNE register also implements the INTSRC and SPLLEN bits, which control certain features of the internal oscillator block.

The INTSRC bit allows users to select which internal oscillator provides the clock source when the 31 kHz frequency option is selected. This is covered in greater detail in **Section 2.5.1 "LFINTOSC"**.

The SPLLEN bit controls the operation of the frequency multiplier. For more details about the function of the SPLLEN bit see **Section 2.9 "4x Phase Lock Loop Frequency Multiplier"**.

REGISTER 2-3: OSCTUNE: OSCILLATOR TUNING REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTSRC	SPLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **INTSRC:** Internal Oscillator Low-Frequency Source Select bit
1 = 31.25 kHz device clock derived from 16 MHz HFINTOSC source (divide-by-512 enabled)
0 = 31 kHz device clock derived directly from LFINTOSC internal oscillator

bit 6 **SPLLEN:** Software Controlled Frequency Multiplier PLL bit
1 = PLL enabled (for HFINTOSC 8 MHz only)
0 = PLL disabled

bit 5-0 **TUN<5:0>:** Frequency Tuning bits
011111 = Maximum frequency
011110 =
• • •
000001 =
000000 = Oscillator module is running at the factory calibrated frequency.
111111 =
• • •
100000 = Minimum frequency

2.7 Oscillator Start-up Timer

The Primary External Oscillator, when configured for LP, XT or HS modes, incorporates an Oscillator Start-up Timer (OST). The OST ensures that the oscillator starts and provides a stable clock to the oscillator module. The OST times out when 1024 oscillations on OSC1 have occurred. During the OST period, with the system clock set to the Primary External Oscillator, the program counter does not increment suspending program execution. The OST period will occur following:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Wake-up from Sleep
- Oscillator being enabled
- Expiration of Power-up Timer (PWRT)

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Start-up mode can be selected. See **Section 2.12 "Two-Speed Start-up Mode"** for more information.

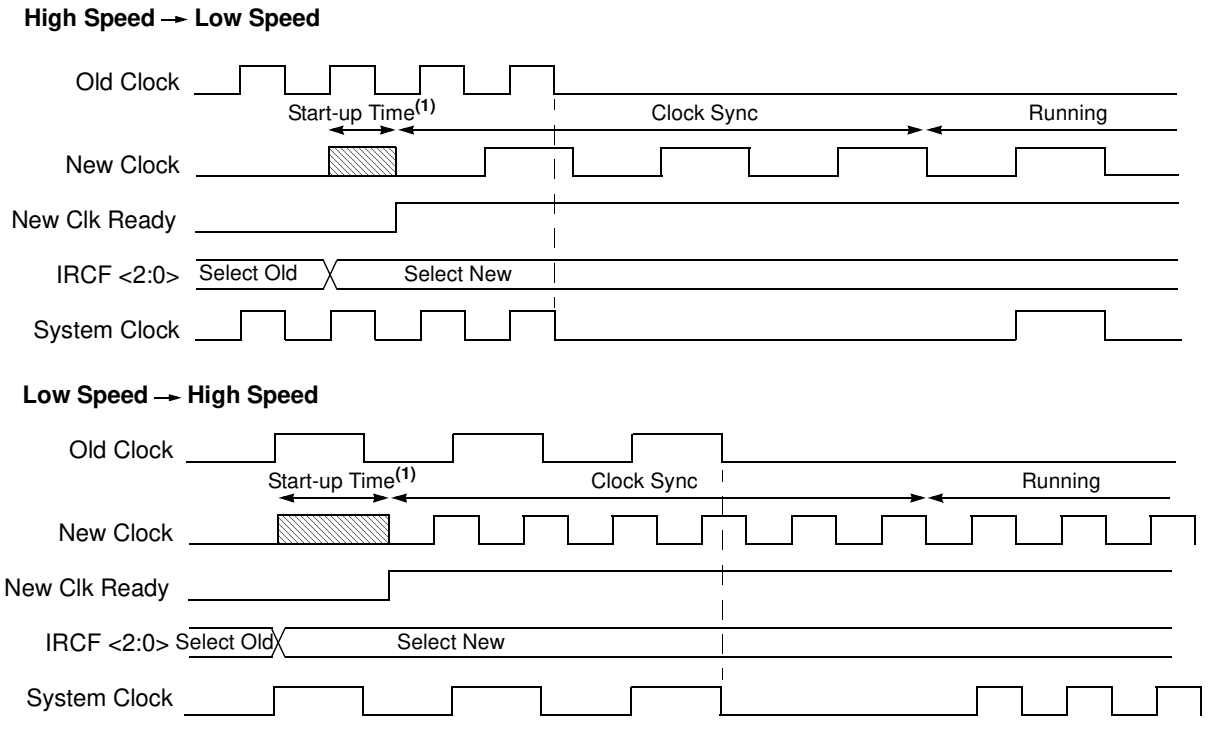
2.8 Clock Switching

The device contains circuitry to prevent clock "glitches" due to a change of the system clock source. To accomplish this, a short pause in the system clock occurs during the clock switch. If the new clock source is not stable (e.g., OST is active), the device will continue to execute from the old clock source until the new clock source becomes stable. The timing of a clock switch is as follows:

1. SCS<1:0> bits of the OSCCON register are modified.
2. The system clock will continue to operate from the old clock until the new clock is ready.
3. Clock switch circuitry waits for two consecutive rising edges of the old clock after the new clock is ready.
4. The system clock is held low, starting at the next falling edge of the old clock.
5. Clock switch circuitry waits for an additional two rising edges of the new clock.
6. On the next falling edge of the new clock, the low hold on the system clock is release and the new clock is switched in as the system clock.
7. Clock switch is complete.

Refer to Figure 2-5 for more details.

FIGURE 2-5: CLOCK SWITCH TIMING



Note 1: Start-up time includes TOST (1024 TOSC) for external clocks, plus TPLL (approx. 2 ms) for HSPLL mode.

TABLE 2-2: EXAMPLES OF DELAYS DUE TO CLOCK SWITCHING

Switch From	Switch To	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	Oscillator Warm-up Delay (TWARM)
Sleep/POR	LP, XT, HS	1024 clock cycles
Sleep/POR	EC, RC	8 clock cycles

2.9 4x Phase Lock Loop Frequency Multiplier

A Phase-Locked Loop (PLL) circuit is provided as an option for users who wish to use a lower frequency external oscillator or to operate at 32 MHz with the HFINTOSC. The PLL is designed for an input frequency from 4 MHz to 12 MHz. The PLL multiplies its input frequency by a factor of four when the PLL is enabled. This may be useful for customers who are concerned with EMI, due to high-frequency crystals.

Two bits control the PLL: the PLLEN bit of the CONFIG1H Configuration register and the SPLLEN bit of the OSCTUNE register. The PLL is enabled when the PLLEN bit is set and it is under software control when the PLLEN bit is cleared.

TABLE 2-3: PLL CONFIGURATION

PLLEN	SPLLEN	PLL Status
1	x	PLL enabled
0	1	PLL enabled
0	0	PLL disabled

2.9.1 32 MHZ INTERNAL OSCILLATOR FREQUENCY SELECTION

The Internal Oscillator Block can be used with the 4X PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in CONFIG1H must be set to use the INTOSC source as the device system clock (FOSC<3:0> = 1000 or 1001).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<3:0> in CONFIG1H (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to the 8 MHz HFINTOSC set to use (IRCF<2:0> = 110).
- The SPLLEN bit in the OSCTUNE register must be set to enable the 4xPLL, or the PLLEN bit of CONFIG1H must be programmed to a '1'.

Note:	When using the PLLEN bit of CONFIG1H, the 4xPLL cannot be disabled by software and the 8 MHz HFINTOSC option will no longer be available.

The 4xPLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4xPLL with the internal oscillator.

2.10 CPU Clock Divider

The CPU Clock Divider allows the system clock to run at a slower speed than the Low/Full Speed USB module clock while sharing the same clock source. Only the oscillator defined by the settings of the FOSC bits of the CONFIG1H Configuration register may be used with the CPU Clock Divider. The CPU Clock Divider is controlled by the CPUDIV bits of the CONFIG1L Configuration register. Setting the CPUDIV bits will set the system clock to:

- Equal the clock speed of the USB module
- Half the clock speed of the USB module
- One third the clock speed of the USB module
- One fourth the clock speed of the USB module

For more information on the CPU Clock Divider, see Figure 2-1 and Register 24-1 CONFIG1L.

2.11 USB Operation

The USB module is designed to operate in two different modes:

- Low Speed
- Full Speed

Because of timing requirements imposed by the USB specifications, the Primary External Oscillator is required for the USB module. The FOSC bits of the CONFIG1H Configuration register must be set to either External Clock (EC) High-Power or HS mode with a clock frequency of 6, 12 or 48 MHz.

2.11.1 LOW-SPEED OPERATION

For low-speed USB operation, a 6 MHz clock is required for the USB module. To generate the 6 MHz clock, only two oscillator modes are allowed:

- EC High-Power mode
- HS mode

Table 2-4 shows the recommended Clock mode for low-speed operation.

Note:	Users must run USB low-speed operation using a CPU clock frequency of 24 MHz or slower (6 MHz is optimal). If anything higher than 24 MHz is used, a firmware delay of at least 14 instruction cycles is required.

2.11.2 FULL-SPEED OPERATION

For full-speed USB operation, a 48 MHz clock is required for the USB module. To generate the 48 MHz clock, only two oscillator modes are allowed:

- EC High-Power mode
- HS mode

Table 2-5 shows the recommended Clock mode for full-speed operation.

TABLE 2-4: LOW-SPEED USB CLOCK SETTINGS

Clock Mode	Clock Frequency	USBDIV	4x PLL Enabled	CPUDIV<1:0>	System Clock Frequency (MHz)
EC High/HS	12 MHz	1	Yes	00	48
				01	24
				10	16
				11	12
			No	00	12
				01	6
				10	4
				11	3
	6 MHz	0	Yes	00	24
				01	12
				10	8
				11	6
			No	00	6
				01	3
				10	2
				11	1.5

Note: The system clock frequency in Table 2-4 only applies if the OSCCON register bits SCS<1:0> = 00. By changing these bits, the system clock can operate down to 31 kHz.

TABLE 2-5: FULL-SPEED USB CLOCK SETTINGS

Clock Mode	Clock Frequency	4x PLL Enabled	CPUDIV<1:0>	System Clock Frequency (MHz)
EC High	48 MHz	No	00	48
			01	24
			10	16
			11	12
EC High/HS	12 MHz	Yes	00	48
			01	24
			10	16
			11	12

Note: The system clock frequency in the above table only applies if the OSCCON register bits SCS<1:0> = 00. By changing these bits, the system clock can operate down to 31 kHz.

2.12 Two-Speed Start-up Mode

Two-Speed Start-Up mode provides additional power savings by minimizing the latency between external Oscillator Start-up Timer (OST) and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the OST period, which can reduce the overall power consumption of the device.

Two-Speed Start-Up mode is enabled by setting the IESO bit of the CONFIG1H Configuration register. With Two-Speed Start-up enabled, the device will execute instructions using the internal oscillator during the Primary External Oscillator OST period.

When the system clock is set to the Primary External Oscillator and the oscillator is configured for LP, XT or HS modes, the device will not execute code during the OST period. The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-Up mode minimizes the delay in code execution by operating from the internal oscillator while the OST is active. The system clock will switch back to the Primary External Oscillator after the OST period has expired.

Two-speed Start-up will become active after:

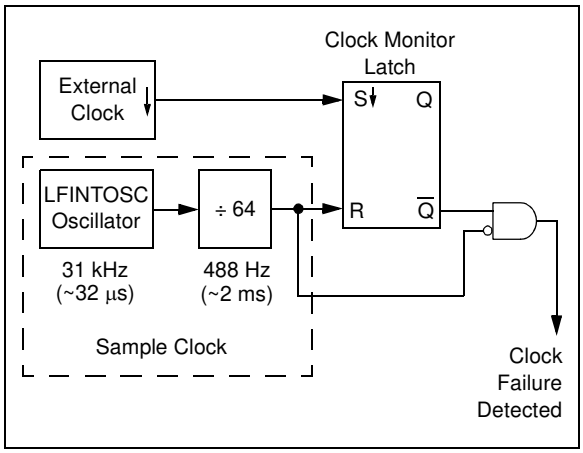
- Power-on Reset (POR)
- Power-up Timer (PWRT), if enabled
- Wake-up from Sleep

The OSTS bit of the OSCCON register reports which oscillator the device is currently using for operation. The device is running from the oscillator defined by the FOSC bits of the CONFIG1H Configuration register when the OSTS bit is set. The device is running from the internal oscillator when the OSTS bit is clear.

2.13 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the CONFIG1H Configuration register. The FSCM is applicable to all external oscillator modes (LP, XT, HS, EC and RC).

FIGURE 2-6: FSCM BLOCK DIAGRAM



2.13.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 2-6. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the primary clock goes low.

2.13.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSCFIF of the PIR2 register. The OSCFIF flag will generate an interrupt if the OSCFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation. An automatic transition back to the failed clock source will not occur.

The internal clock source chosen by the FSCM is determined by the IRCF<2:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.