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PIC18F2XXX/4XXX FAMILY

Flash Microcontroller Programming Specification

1.0 DEVICE OVERVIEW

This document includes the programming specifications for the following devices:

- PIC18F2221
- PIC18F2321
- PIC18F2410
- PIC18F2420
- PIC18F2423
- PIC18F2450
- PIC18F2455
- PIC18F2458
- PIC18F2480
- PIC18F2510
- PIC18F2515
- PIC18F2520
- PIC18F2523
- PIC18F2525
- PIC18F2550
- PIC18F2553
- PIC18F2580
- PIC18F2585
- PIC18F2610
- PIC18F2620
- PIC18F2680
- PIC18F2682
- PIC18F2685
- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4515
- PIC18F4520
- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

2.0 PROGRAMMING OVERVIEW

PIC18F2XXX/4XXX Family devices can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP method. Both methods can be done with the device in the user's system. The low-voltage ICSP method is slightly different than the high-voltage method and these differences are noted where applicable.

This programming specification applies to the PIC18F2XXX/4XXX Family devices in all package types.

2.1 Hardware Requirements

In High-Voltage ICSP mode, PIC18F2XXX/4XXX Family devices require two programmable power supplies: one for VDD and one for MCLR/VPP/RE3. Both supplies should have a minimum resolution of 0.25V. Refer to [Section 6.0 “AC/DC Characteristics Timing Requirements for Program/Verify Test Mode”](#) for additional hardware parameters.

2.1.1 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, PIC18F2XXX/4XXX Family devices can be programmed using a VDD source in the operating range. The MCLR/VPP/RE3 does not have to be brought to a different voltage, but can instead be left at the normal operating voltage. Refer to [Section 6.0 “AC/DC Characteristics Timing Requirements for Program/Verify Test Mode”](#) for additional hardware parameters.

2.2 Pin Diagrams

The pin diagrams for the PIC18F2XXX/4XXX Family are shown in [Figure 2-1](#), [Figure 2-2](#), [Figure 2-3](#), [Figure 2-4](#), [Figure 2-5](#).

PIC18F2XXX/4XXX FAMILY

TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F2XXX/4XXX FAMILY

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
MCLR/VPP/RE3	VPP	P	Programming Enable
VDD ⁽²⁾	VDD	P	Power Supply
VSS ⁽²⁾	VSS	P	Ground
RB5	PGM	I	Low-Voltage ICSP™ Input when LVP Configuration bit equals '1' ⁽¹⁾
RB6	PGC	I	Serial Clock
RB7	PGD	I/O	Serial Data

Legend: I = Input, O = Output, P = Power

Note 1: See Figure 5-1 for more information.

2: All power supply (VDD) and ground (VSS) pins must be connected.

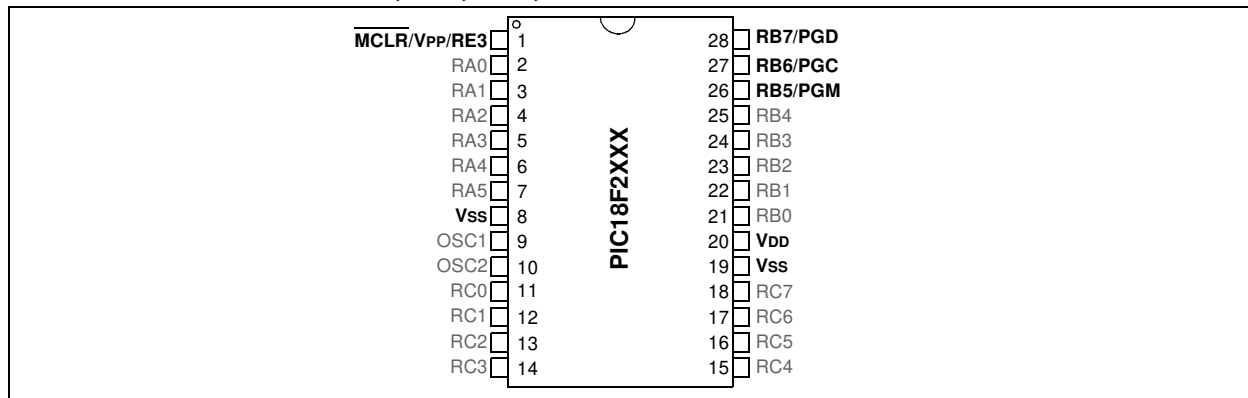
The following devices are included in 28-pin SPDIP, PDIP and SOIC parts:

- PIC18F2221
- PIC18F2321
- PIC18F2410
- PIC18F2420
- PIC18F2423
- PIC18F2450
- PIC18F2455
- PIC18F2458
- PIC18F2480
- PIC18F2510
- PIC18F2515
- PIC18F2520
- PIC18F2523
- PIC18F2525
- PIC18F2550
- PIC18F2553
- PIC18F2580
- PIC18F2585
- PIC18F2610
- PIC18F2620
- PIC18F2680
- PIC18F2682
- PIC18F2685

The following devices are included in 28-pin SSOP parts:

- PIC18F2221
- PIC18F2321

FIGURE 2-1: 28-Pin SPDIP, PDIP, SOIC,SSOP

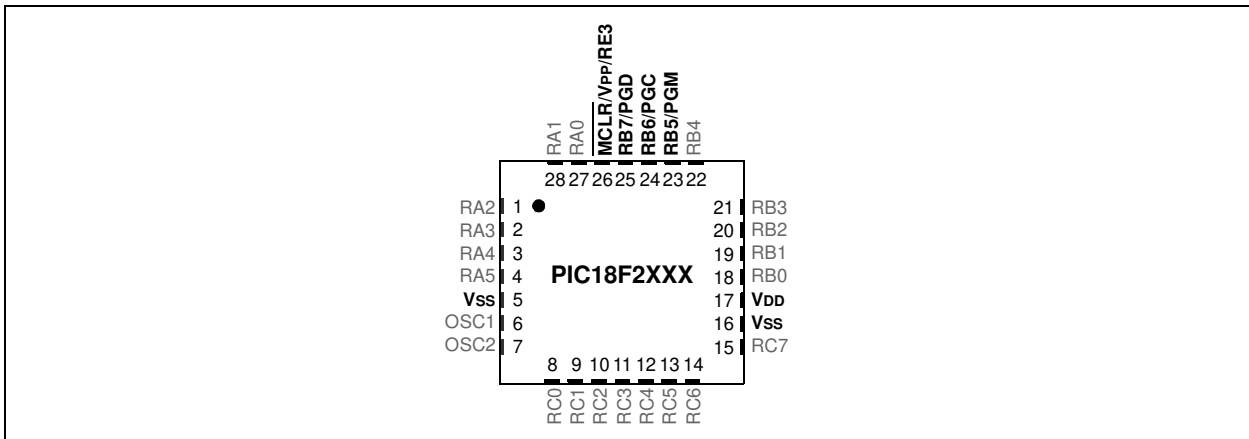


PIC18F2XXX/4XXX FAMILY

The following devices are included in 28-pin QFN parts:

- | | | | |
|--------------|--------------|--------------|--------------|
| • PIC18F2221 | • PIC18F2423 | • PIC18F2510 | • PIC18F2580 |
| • PIC18F2321 | • PIC18F2450 | • PIC18F2520 | • PIC18F2682 |
| • PIC18F2410 | • PIC18F2480 | • PIC18F2523 | • PIC18F2685 |
| • PIC18F2420 | • | • | • |

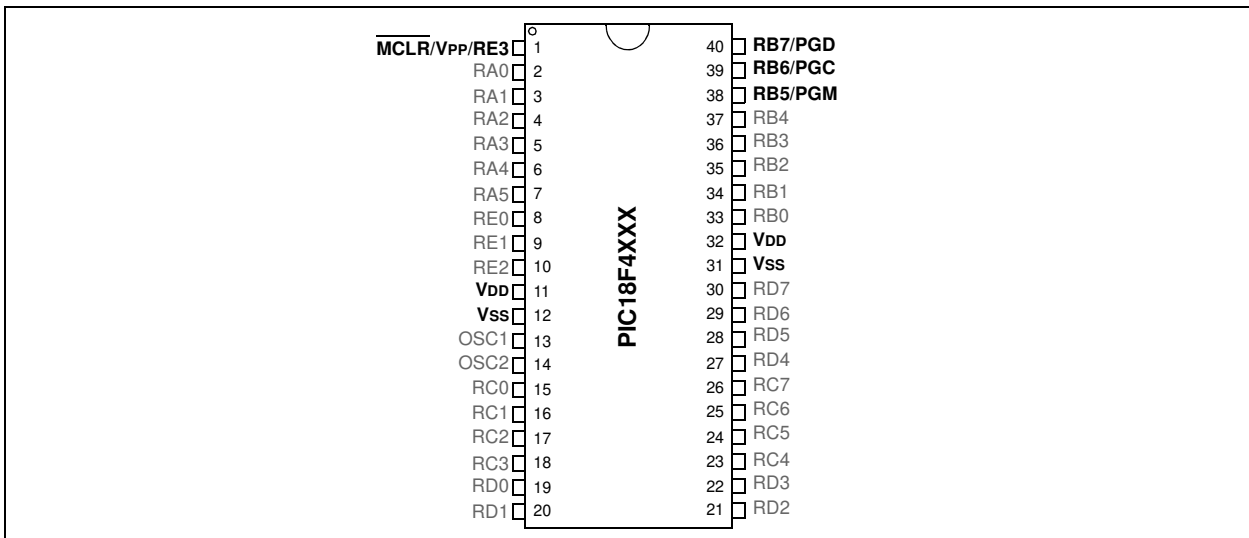
FIGURE 2-2: 28-Pin QFN



The following devices are included in 40-pin PDIP parts:

- | | | | |
|--------------|--------------|--------------|--------------|
| • PIC18F4221 | • PIC18F4455 | • PIC18F4523 | • PIC18F4610 |
| • PIC18F4321 | • PIC18F4458 | • PIC18F4525 | • PIC18F4620 |
| • PIC18F4410 | • PIC18F4480 | • PIC18F4550 | • PIC18F4680 |
| • PIC18F4420 | • PIC18F4510 | • PIC18F4553 | • PIC18F4682 |
| • PIC18F4423 | • PIC18F4515 | • PIC18F4580 | • PIC18F4685 |
| • PIC18F4450 | • PIC18F4520 | • PIC18F4585 | • |

FIGURE 2-3: 40-Pin PDIP

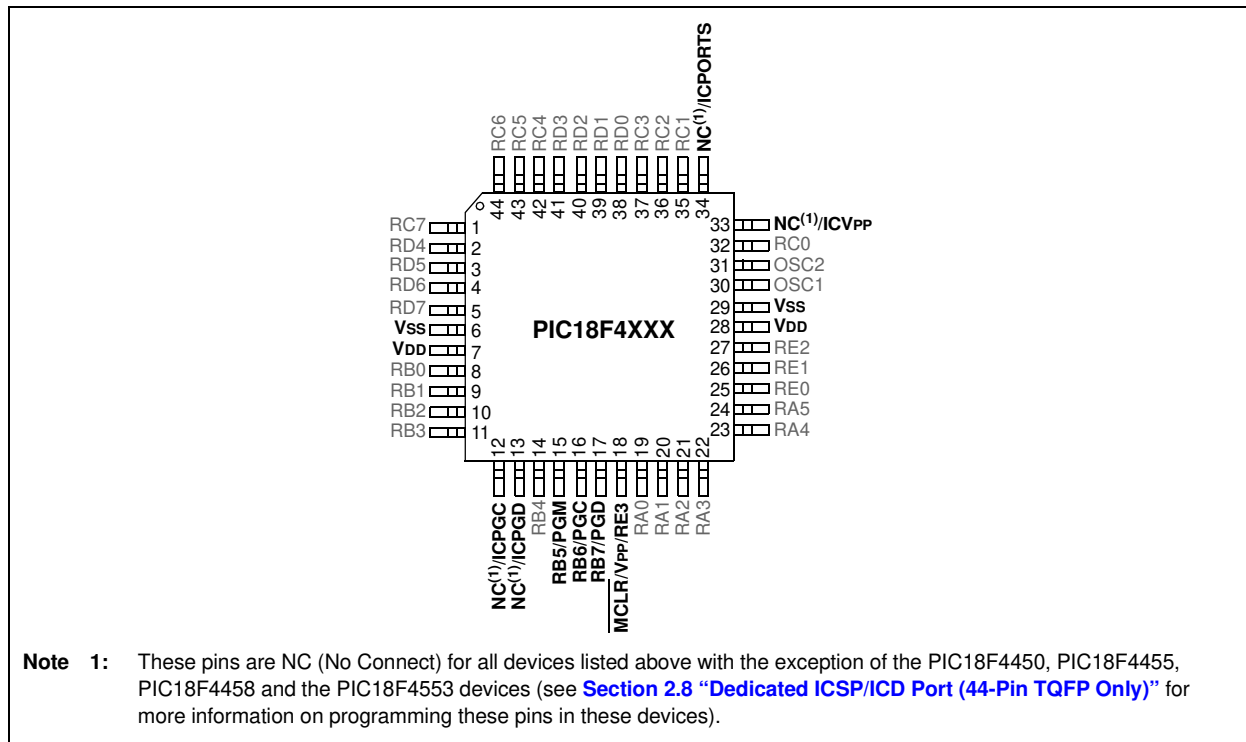


PIC18F2XXX/4XXX FAMILY

The following devices are included in 44-pin TQFP parts:

- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4520
- PIC18F4515
- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

FIGURE 2-4: 44-PIN TQFP

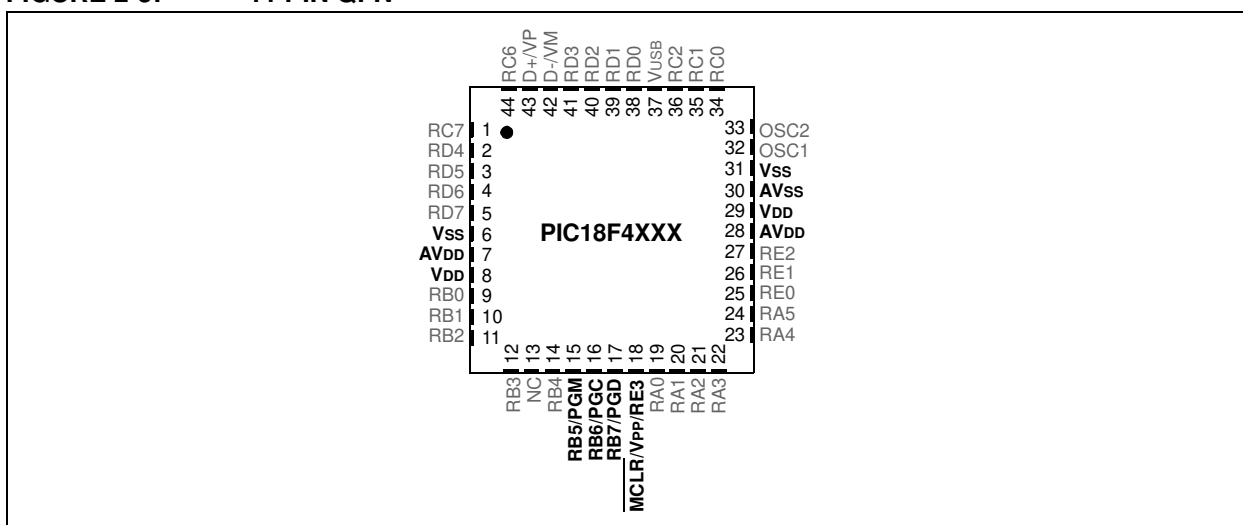


PIC18F2XXX/4XXX FAMILY

The following devices are included in 44-pin QFN parts:

- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4520
- PIC18F4515
- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

FIGURE 2-5: 44-PIN QFN



2.3 Memory Maps

For PIC18FX6X0 devices, the code memory space extends from 0000h to 0FFFFh (64 Kbytes) in four 16-Kbyte blocks. For PIC18FX5X5 devices, the code memory space extends from 0000h to 0BFFFFh (48 Kbytes) in three 16-Kbyte blocks. Addresses, 0000h through 07FFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

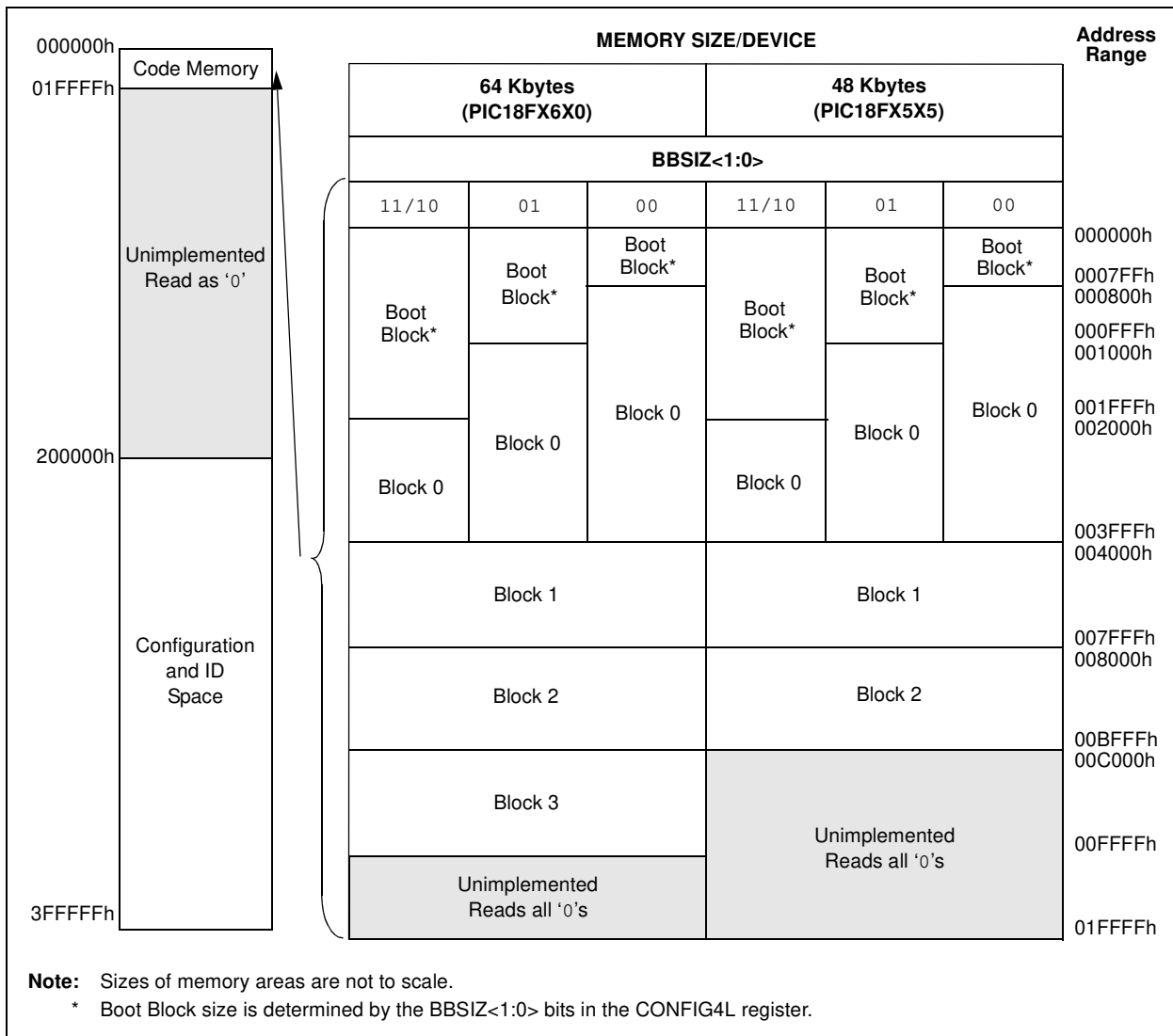
The size of the Boot Block in PIC18F2585/2680/4585/4680 devices can be configured as 1, 2 or 4K words (see [Figure 2-6](#)). This is done through the BBSIZ<1:0> bits in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

PIC18F2XXX/4XXX FAMILY

TABLE 2-2: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2515	000000h-00BFFFh (48K)
PIC18F2525	
PIC18F2585	
PIC18F4515	
PIC18F4525	
PIC18F4585	
PIC18F2610	000000h-00FFFFh (64K)
PIC18F2620	
PIC18F2680	
PIC18F4610	
PIC18F4620	
PIC18F4680	

FIGURE 2-6: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX5X5/X6X0 DEVICES



PIC18F2XXX/4XXX FAMILY

For PIC18F2685/4685 devices, the code memory space extends from 0000h to 017FFFh (96 Kbytes) in five 16-Kbyte blocks. For PIC18F2682/4682 devices, the code memory space extends from 0000h to 0013FFFh (80 Kbytes) in four 16-Kbyte blocks. Addresses, 0000h through 0FFFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

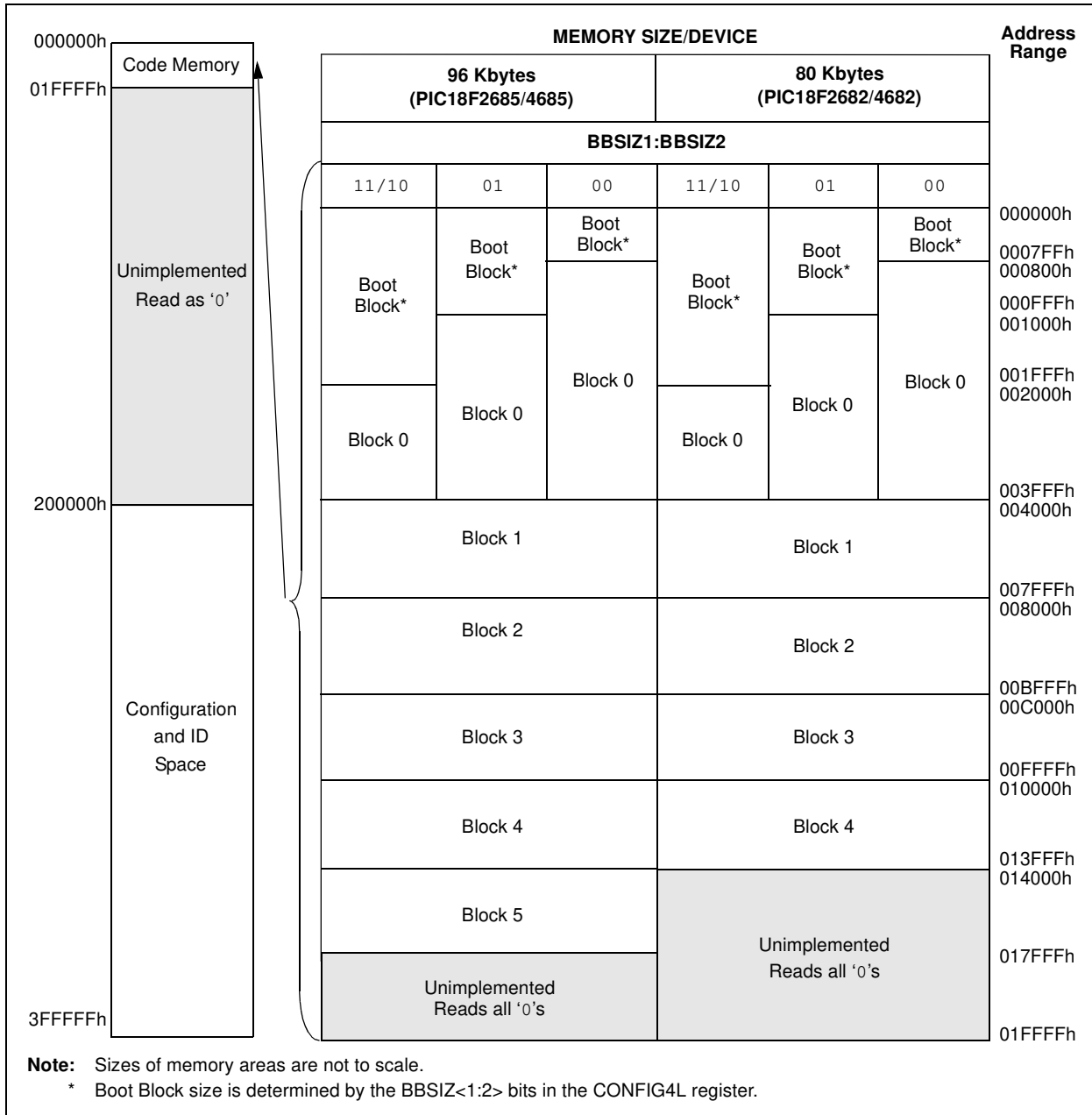
The size of the Boot Block in PIC18F2685/4685 and PIC18F2682/4682 devices can be configured as 1, 2 or 4K words (see [Figure 2-7](#)). This is done through the BBSIZ<2:1> bits in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

TABLE 2-3: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2682	000000h-013FFFh (80K)
PIC18F4682	
PIC18F2685	000000h-017FFFh (96K)
PIC18F4685	

PIC18F2XXX/4XXX FAMILY

FIGURE 2-7: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18F2685/4685 AND PIC18F2682/4682 DEVICES



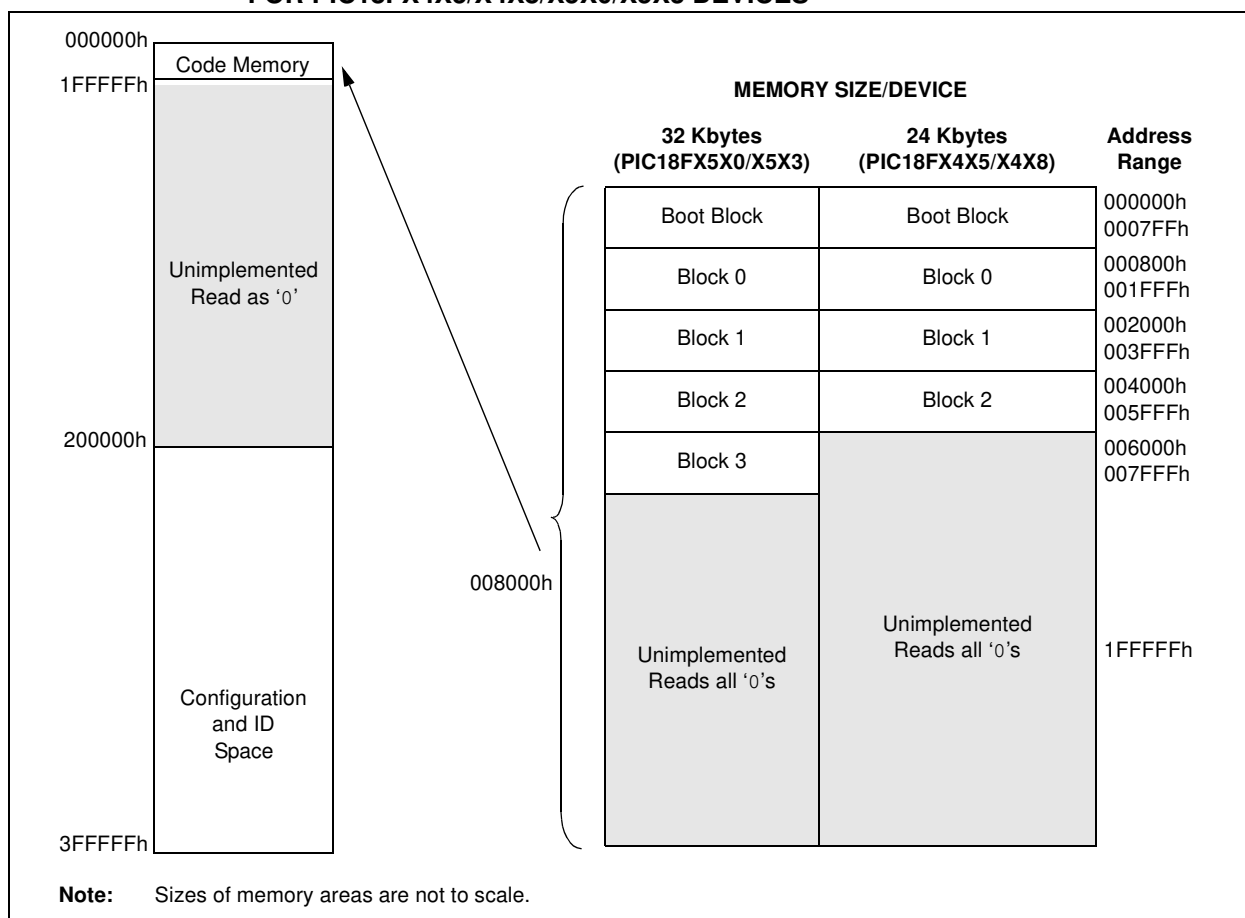
For PIC18FX5X0/X5X3 devices, the code memory space extends from 000000h to 007FFFh (32 Kbytes) in four 8-Kbyte blocks. For PIC18FX4X5/X4X8 devices, the code memory space extends from 000000h to 005FFFh (24 Kbytes) in three 8-Kbyte blocks. Addresses, 000000h through 0007FFFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

PIC18F2XXX/4XXX FAMILY

TABLE 2-4: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2455	000000h-005FFFh (24K)
PIC18F2458	
PIC18F4455	
PIC18F4458	
PIC18F2510	000000h-007FFFh (32K)
PIC18F2520	
PIC18F2523	
PIC18F2550	
PIC18F2553	
PIC18F4510	
PIC18F4520	
PIC18F4523	
PIC18F4550	
PIC18F4553	

FIGURE 2-8: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX4X5/X4X8/X5X0/X5X3 DEVICES



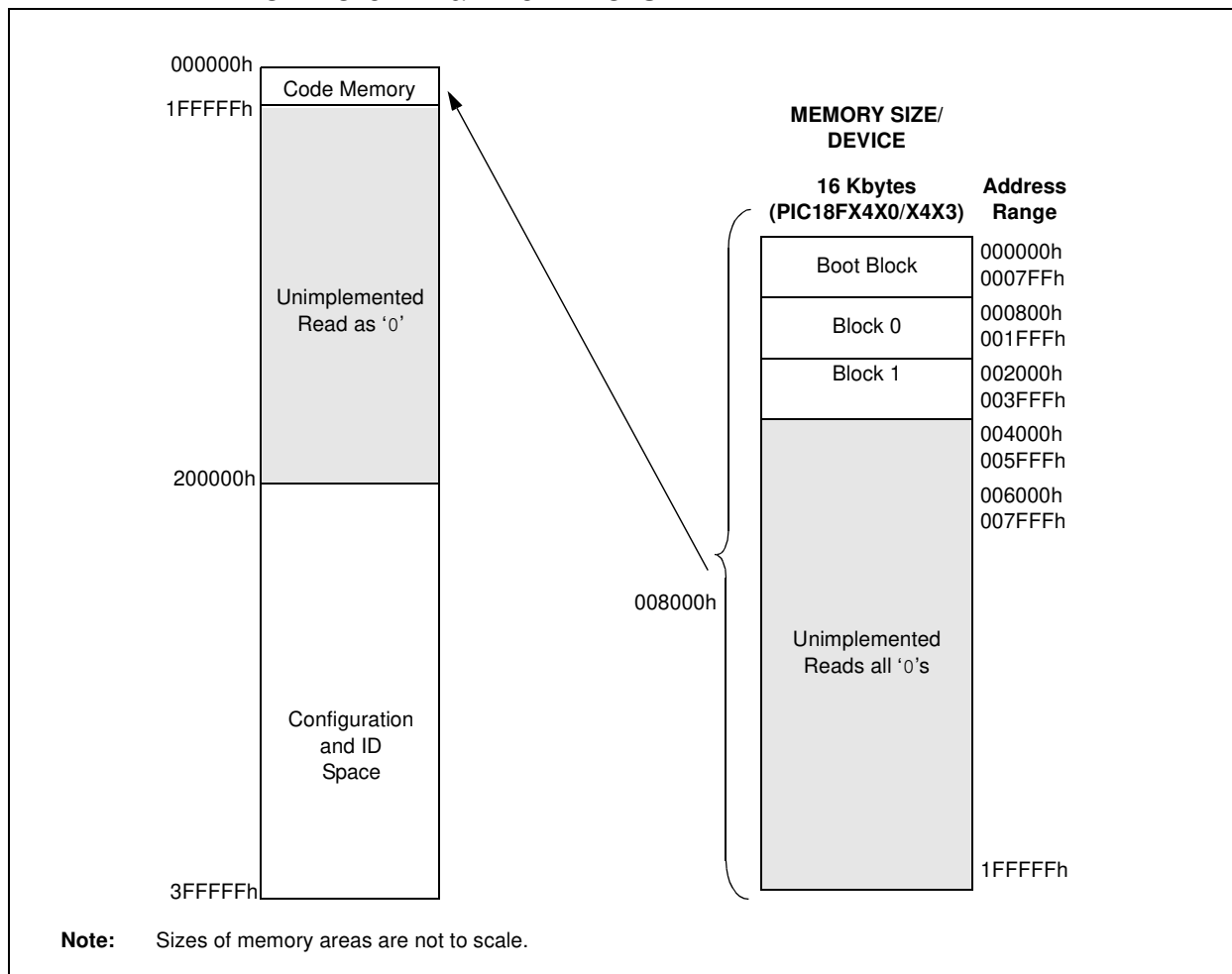
For PIC18FX4X0/X4X3 devices, the code memory space extends from 000000h to 003FFFh (16 Kbytes) in two 8-Kbyte blocks. Addresses, 000000h through 0003FFFh, however, define a "Boot Block" region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

PIC18F2XXX/4XXX FAMILY

TABLE 2-5: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2410	000000h-003FFFh (16K)
PIC18F2420	
PIC18F2423	
PIC18F2450	
PIC18F4410	
PIC18F4420	
PIC18F4450	

FIGURE 2-9: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX4X0/X4X3 DEVICES



For PIC18F2480/4480 devices, the code memory space extends from 0000h to 03FFFh (16 Kbytes) in one 16-Kbyte block. For PIC18F2580/4580 devices, the code memory space extends from 0000h to 07FFFh (32 Kbytes) in two 16-Kbyte blocks. Addresses, 0000h through 07FFFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

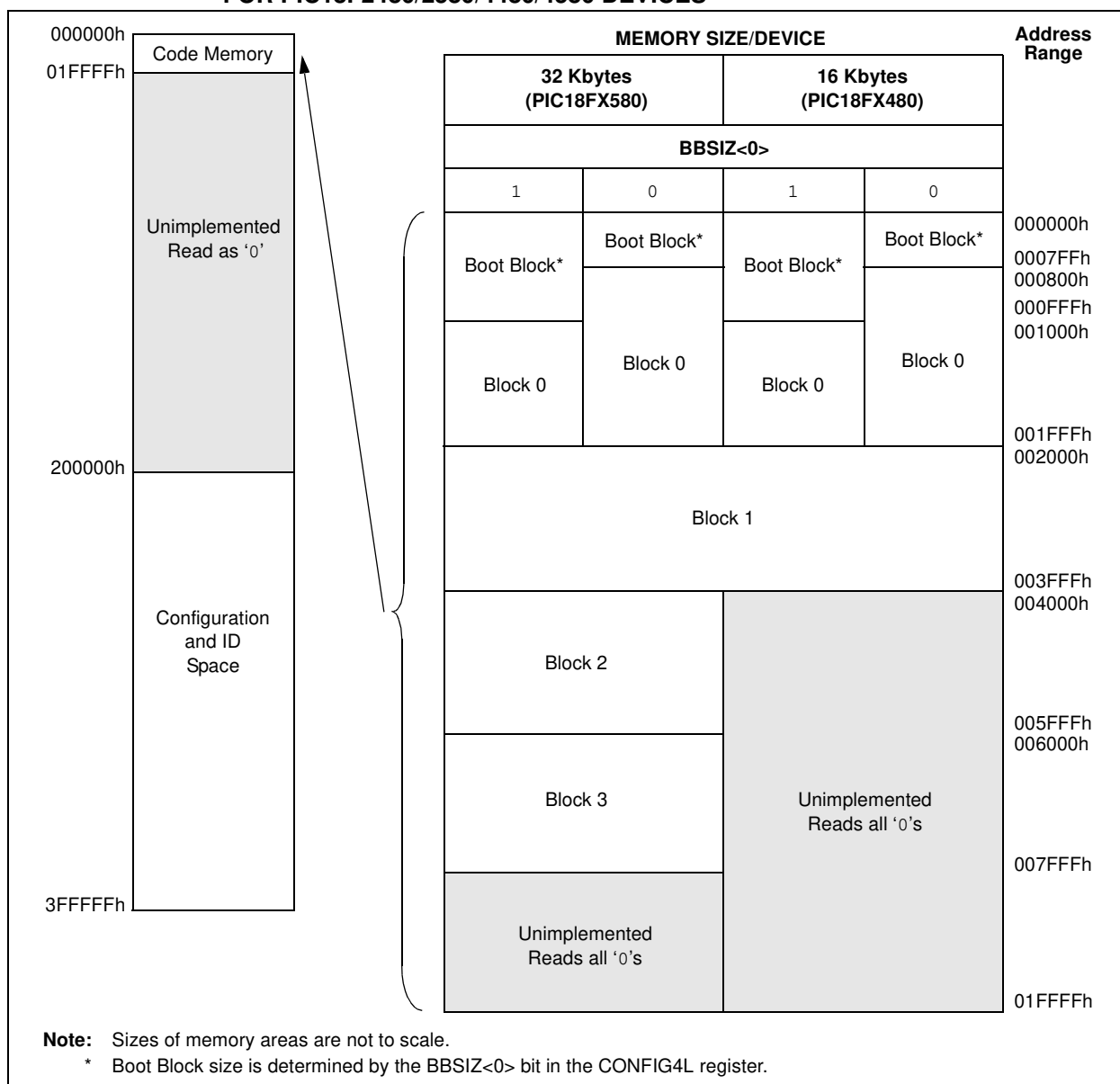
The size of the Boot Block in PIC18F2480/2580/4480/4580 devices can be configured as 1 or 2K words (see [Figure 2-10](#)). This is done through the BBSIZ<0> bit in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

PIC18F2XXX/4XXX FAMILY

TABLE 2-6: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2480	000000h-003FFFh (16K)
PIC18F4480	
PIC18F2580	000000h-007FFFh (32K)
PIC18F4580	

FIGURE 2-10: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18F2480/2580/4480/4580 DEVICES



For PIC18F2221/4221 devices, the code memory space extends from 0000h to 00FFFh (4 Kbytes) in one 4-Kbyte block. For PIC18F2321/4321 devices, the code memory space extends from 0000h to 01FFFh (8 Kbytes) in two 4-Kbyte blocks. Addresses, 0000h through 07FFFh, however, define a variable “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

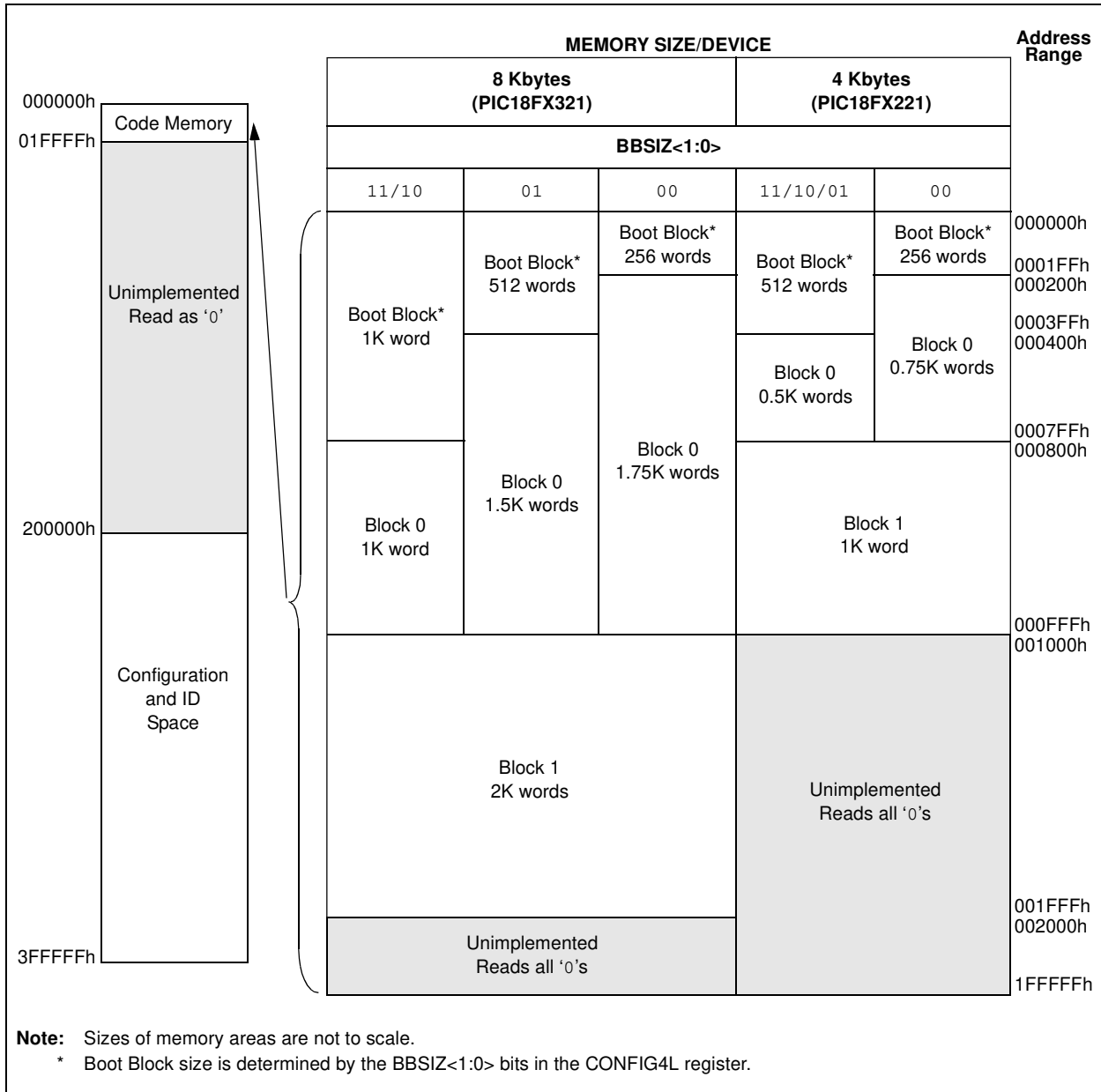
PIC18F2XXX/4XXX FAMILY

The size of the Boot Block in PIC18F2221/2321/4221/4321 devices can be configured as 256, 512 or 1024 words (see Figure 2-11). This is done through the BBSIZ<1:0> bits in the Configuration register, CONFIG4L (see Figure 2-11). It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

TABLE 2-7: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2221	000000h-000FFFh (4K)
PIC18F4221	
PIC18F2321	000000h-001FFFh (8K)
PIC18F4321	

FIGURE 2-11: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18F2221/2321/4221/4321 DEVICES



PIC18F2XXX/4XXX FAMILY

In addition to the code memory space, there are three blocks that are accessible to the user through Table Reads and Table Writes. Their locations in the memory map are shown in [Figure 2-12](#).

Users may store identification information (ID) in eight ID registers. These ID registers are mapped in addresses, 200000h through 200007h. The ID locations read out normally, even after code protection is applied.

Locations, 300000h through 30000Dh, are reserved for the Configuration bits. These bits select various device options and are described in [Section 5.0 “Configuration Word”](#). These Configuration bits read out normally, even after code protection.

Locations, 3FFFEh and 3FFFFh, are reserved for the Device ID bits. These bits may be used by the programmer to identify what device type is being programmed and are described in [Section 5.0 “Configuration Word”](#). These Device ID bits read out normally, even after code protection.

2.3.1 MEMORY ADDRESS POINTER

Memory in the address space, 000000h to 3FFFFFFh, is addressed via the Table Pointer register, which is comprised of three pointer registers:

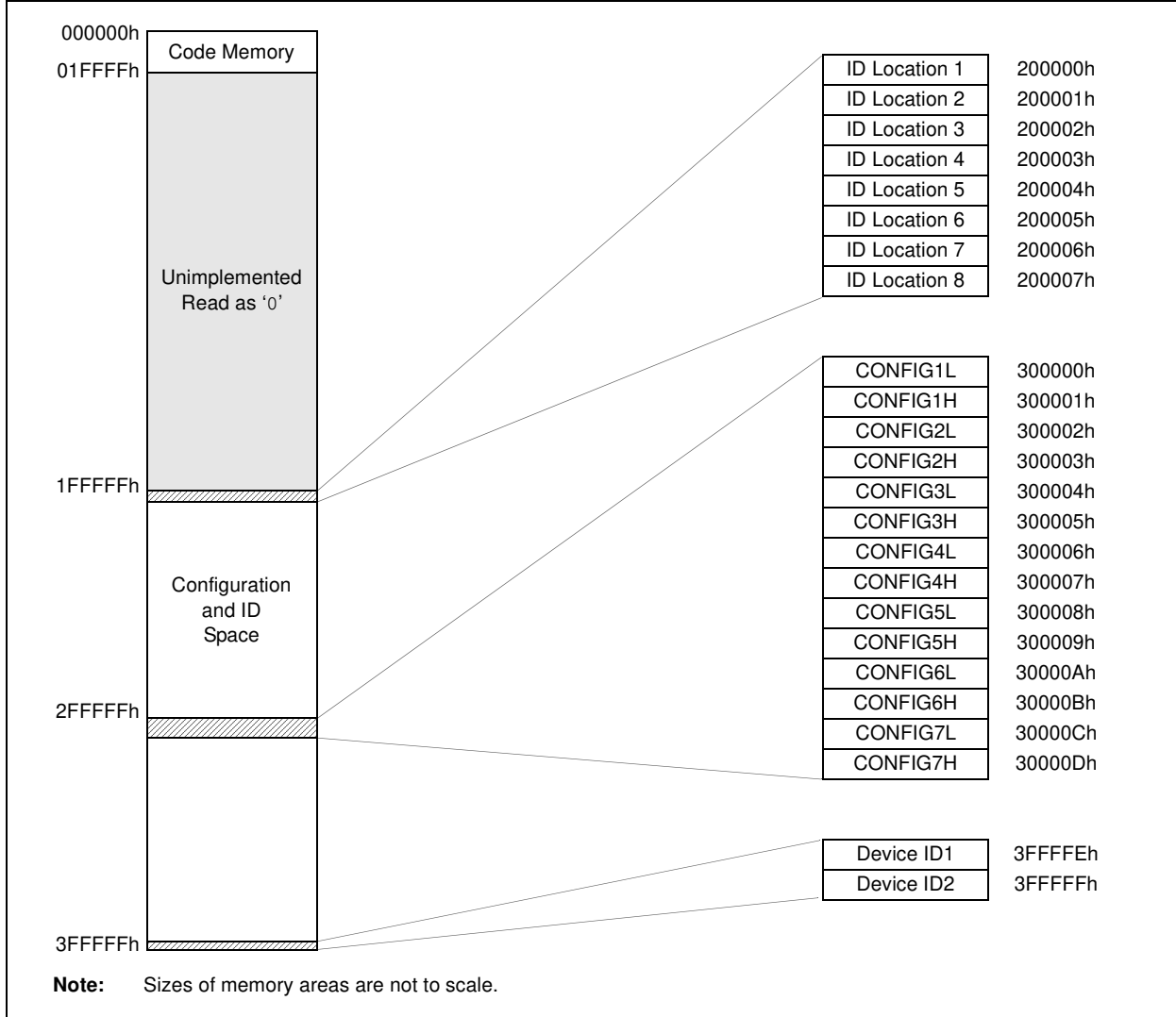
- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

PIC18F2XXX/4XXX FAMILY

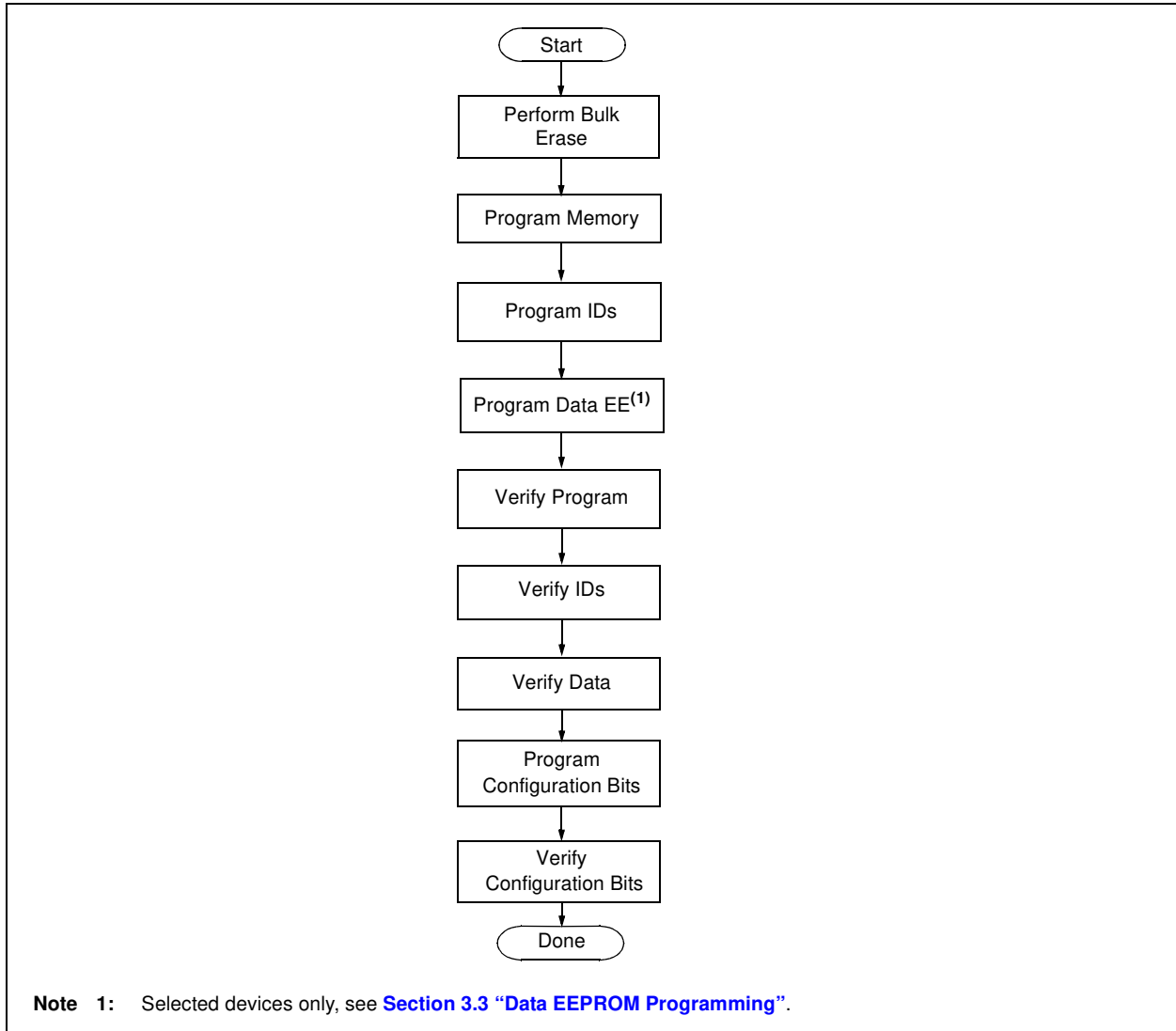
FIGURE 2-12: CONFIGURATION AND ID LOCATIONS FOR PIC18F2XXX/4XXX FAMILY DEVICES



2.4 High-Level Overview of the Programming Process

Figure 2-13 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory, ID locations and data EEPROM are programmed (selected devices only, see [Section 3.3 “Data EEPROM Programming”](#)). These memories are then verified to ensure that programming was successful. If no errors are detected, the Configuration bits are then programmed and verified.

FIGURE 2-13: HIGH-LEVEL PROGRAMMING FLOW



PIC18F2XXX/4XXX FAMILY

2.5 Entering and Exiting High-Voltage ICSP Program/Verify Mode

As shown in [Figure 2-14](#), the High-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low and then raising $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$ to V_{IH} (high voltage). Once in this mode, the code memory, data EEPROM (selected devices only, see [Section 3.3 “Data EEPROM Programming”](#)), ID locations and Configuration bits can be accessed and programmed in serial fashion. [Figure 2-15](#) shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 2-14: ENTERING HIGH-VOLTAGE PROGRAM/VERIFY MODE

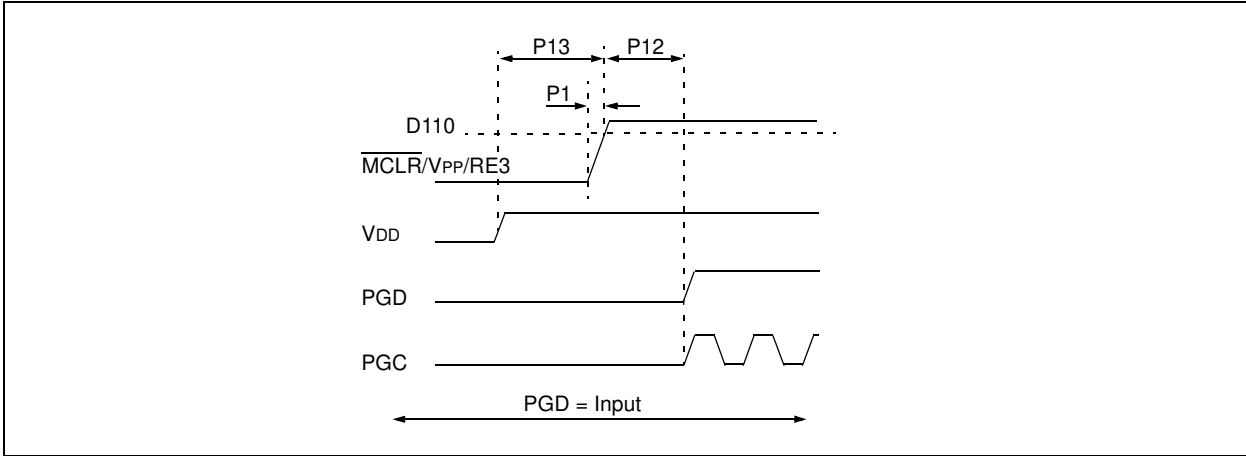
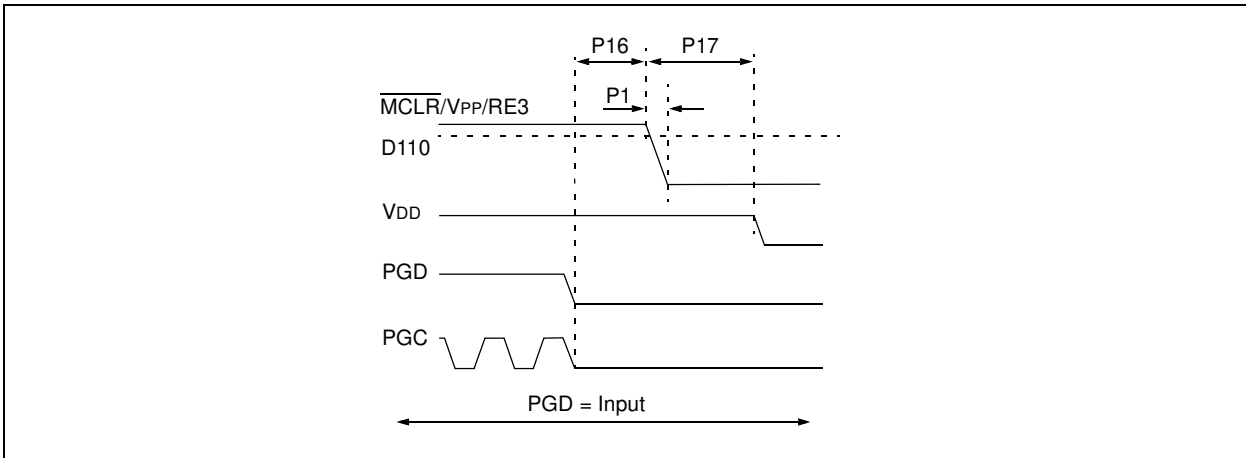


FIGURE 2-15: EXITING HIGH-VOLTAGE PROGRAM/VERIFY MODE



PIC18F2XXX/4XXX FAMILY

2.6 Entering and Exiting Low-Voltage ICSP Program/Verify Mode

When the LVP Configuration bit is '1' (see [Section 5.3 "Single-Supply ICSP Programming"](#)), the Low-Voltage ICSP mode is enabled. As shown in [Figure 2-16](#), Low-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low, placing a logic high on PGM and then raising $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$ to V_{IH} . In this mode, the RB5/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin. [Figure 2-17](#) shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 2-16: ENTERING LOW-VOLTAGE PROGRAM/VERIFY MODE

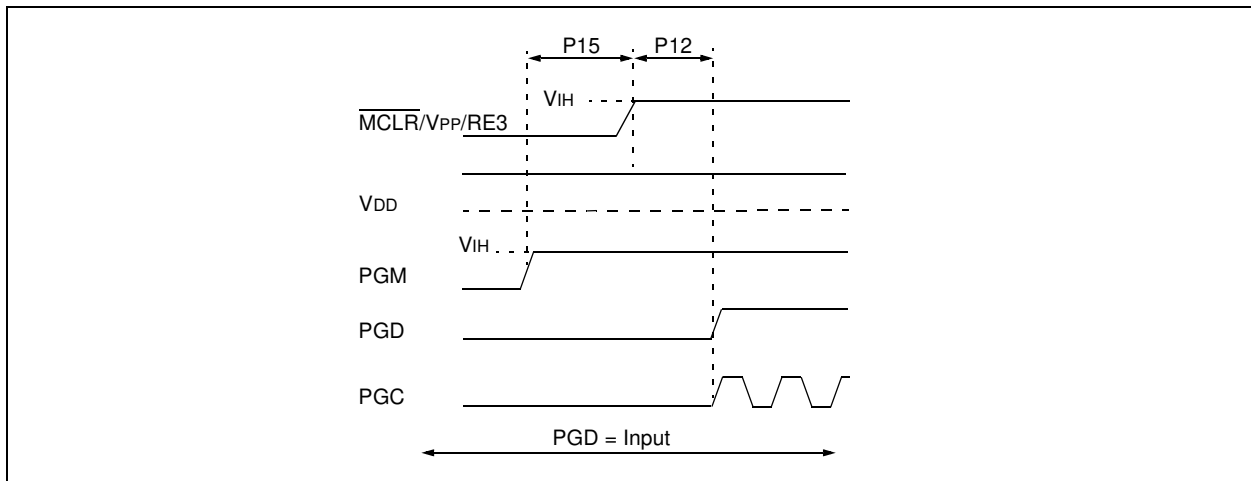
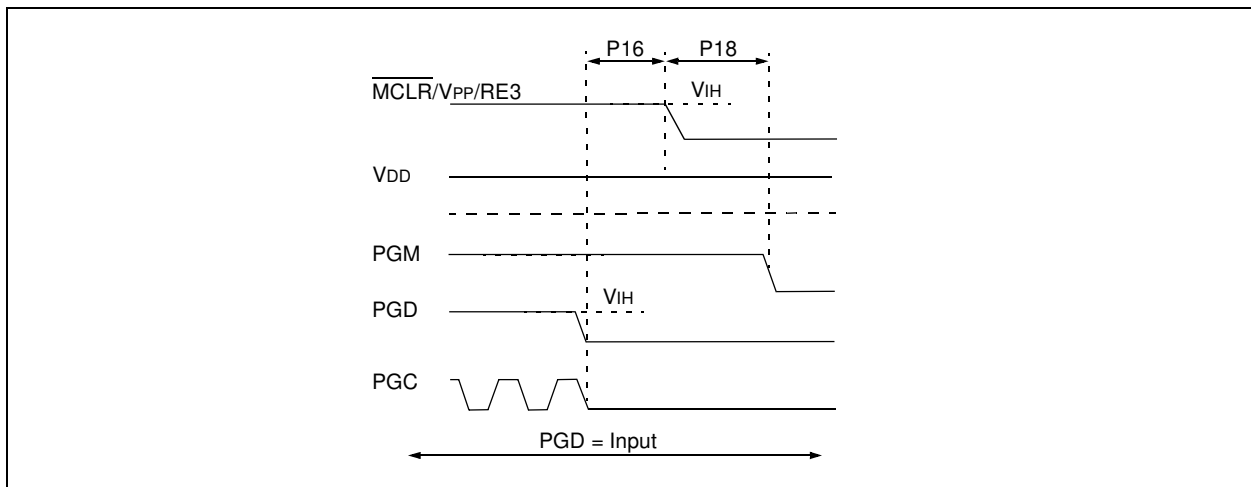


FIGURE 2-17: EXITING LOW-VOLTAGE PROGRAM/VERIFY MODE



PIC18F2XXX/4XXX FAMILY

2.7 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC and are Least Significant bit (LSb) first.

2.7.1 4-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in [Table 2-8](#).

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or 8 bits of input data and 8 bits of output data.

Throughout this specification, commands and data are presented as illustrated in [Table 2-9](#). The 4-bit command is shown Most Significant bit (MSb) first. The command operand, or “Data Payload”, is shown as <MSB><LSB>. [Figure 2-18](#) demonstrates how to serially present a 20-bit command/operand to the device.

2.7.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

TABLE 2-8: COMMANDS FOR PROGRAMMING

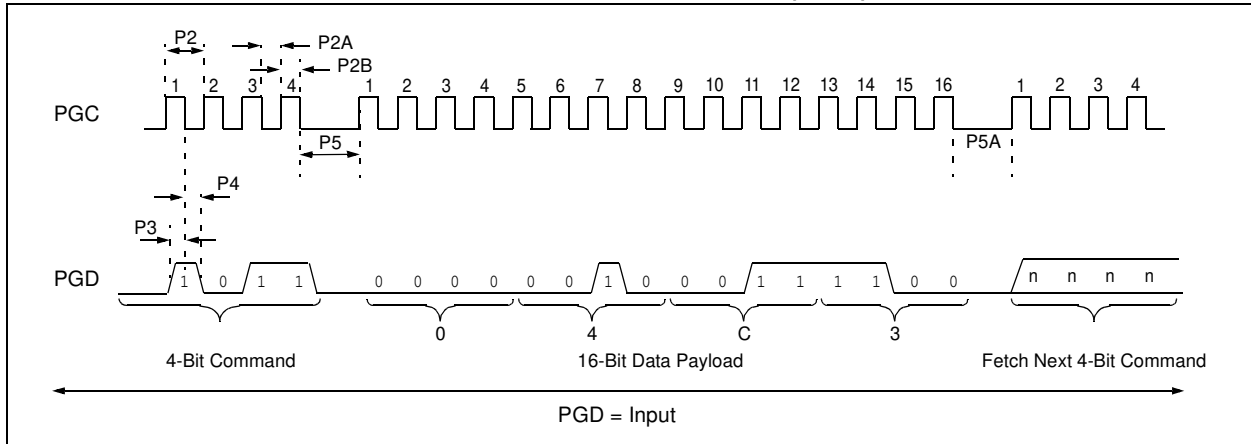
Description	4-Bit Command
Core Instruction (Shift in 16-bit instruction)	0000
Shift Out TABLAT Register	0010
Table Read	1000
Table Read, Post-Increment	1001
Table Read, Post-Decrement	1010
Table Read, Pre-Increment	1011
Table Write	1100
Table Write, Post-Increment by 2	1101
Table Write, Start Programming, Post-Increment by 2	1110
Table Write, Start Programming	1111

TABLE 2-9: SAMPLE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
1101	3C 40	Table Write, post-increment by 2

PIC18F2XXX/4XXX FAMILY

FIGURE 2-18: TABLE WRITE, POST-INCREMENT TIMING (1101)



2.8 Dedicated ICSP/ICD Port (44-Pin TQFP Only)

The PIC18F4455/4458/4550/4553 44-pin TQFP devices are designed to support an alternate programming input: the dedicated ICSP/ICD port. The primary purpose of this port is to provide an alternate In-Circuit Debugging (ICD) option and free the pins (RB6, RB7 and MCLR) that would normally be used for debugging the application. In conjunction with ICD capability, however, the dedicated ICSP/ICD port also provides an alternate port for ICSP.

Setting the ICPRT Configuration bit enables the dedicated ICSP/ICD port. The dedicated ICSP/ICD port functions the same as the default ICSP/ICD port; however, alternate pins are used instead of the default pins. Table 2-10 identifies the functionally equivalent pins for ICSP purposes:

The dedicated ICSP/ICD port is an alternate port. Thus, ICSP is still available through the default port even though the ICPRT Configuration bit is set. When the V_{IH} is seen on the MCLR/VPP/RE3 pin prior to applying V_{IH} to the ICRST/ICVPP pin, then the state of the ICRST/ICVPP pin is ignored. Likewise, when the V_{IH} is seen on ICRST/ICVPP prior to applying V_{IH} to MCLR/VPP/RE3, then the state of the MCLR/VPP/RE3 pin is ignored.

Note: The ICPRT Configuration bit can only be programmed through the default ICSP port. Chip Erase functions through the dedicated ICSP/ICD port do not affect this bit.

When the ICPRT Configuration bit is set (dedicated ICSP/ICD port enabled), the NC/ICPORTS pin must be tied to either VDD or VSS.

The ICPRT Configuration bit must be maintained clear for all 28-pin and 40-pin devices; otherwise, unexpected operation may occur.

TABLE 2-10: ICSP™ EQUIVALENT PINS

Pin Name	During Programming			
	Pin Name	Pin Type	Dedicated Pins	Pin Description
MCLR/VPP/RE3	VPP	P	NC/ICRST/ICVPP	Programming Enable
RB6	PGC	I	NC/ICCK/ICPGC	Serial Clock
RB7	PGD	I/O	NC/ICDT/ICPGD	Serial Data

Legend: I = Input, O = Output, P = Power

PIC18F2XXX/4XXX FAMILY

3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the various memory regions within the device.

In all cases, except high-voltage ICSP Bulk Erase, the EECON1 register must be configured in order to operate on a particular memory region.

When using the EECON1 register to act on code memory, the EEPGD bit must be set (EECON1<7> = 1) and the CFGS bit must be cleared (EECON1<6> = 0). The WREN bit must be set (EECON1<2> = 1) to enable writes of any sort (e.g., erases) and this must be done prior to initiating a write sequence. The FREE bit must be set (EECON1<4> = 1) in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit (EECON1<1> = 1). It is strongly recommended that the WREN bit only be set immediately prior to a program erase.

3.1 ICSP Erase

3.1.1 HIGH-VOLTAGE ICSP BULK ERASE

Erasing code or data EEPROM is accomplished by configuring two Bulk Erase Control registers located at 3C0004h and 3C0005h. Code memory may be erased, portions at a time, or the user may erase the entire device in one action. Bulk Erase operations will also clear any code-protect settings associated with the memory block being erased. Erase options are detailed in [Table 3-1](#). If data EEPROM is code-protected (CPD = 0), the user must request an erase of data EEPROM (e.g., 0084h as shown in [Table 3-1](#)).

TABLE 3-1: BULK ERASE OPTIONS

Description	Data (3C0005h:3C0004h)
Chip Erase	3F8Fh
Erase Data EEPROM ⁽¹⁾	0084h
Erase Boot Block	0081h
Erase Configuration Bits	0082h
Erase Code EEPROM Block 0	0180h
Erase Code EEPROM Block 1	0280h
Erase Code EEPROM Block 2	0480h
Erase Code EEPROM Block 3	0880h
Erase Code EEPROM Block 4	1080h
Erase Code EEPROM Block 5	2080h

Note 1: Selected devices only, see [Section 3.3 “Data EEPROM Programming”](#).

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the NOP command), serial execution will cease until the erase completes (Parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

The code sequence to erase the entire device is shown in [Table](#) and the flowchart is shown in [Figure 3-1](#).

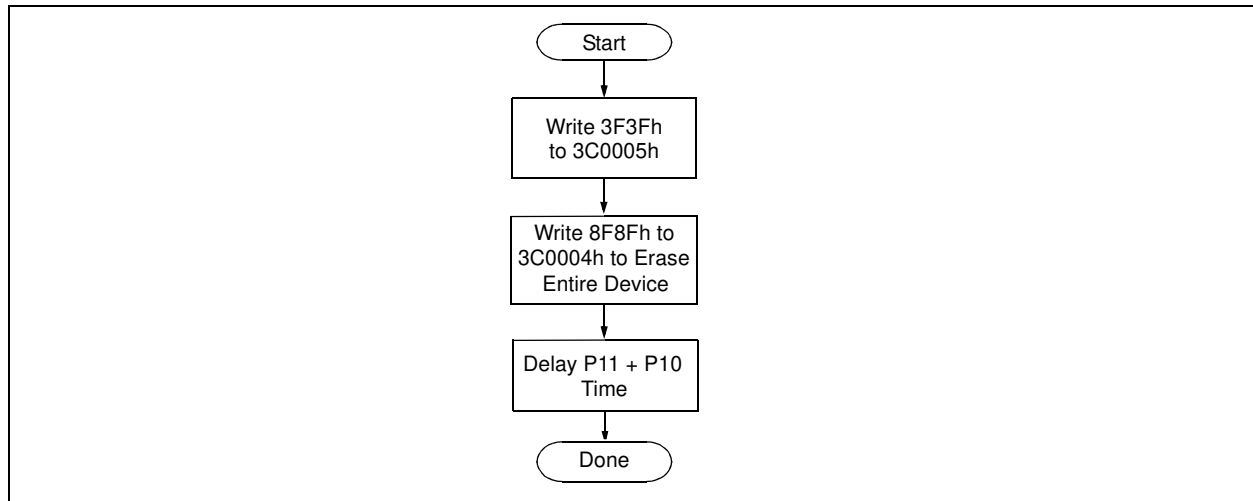
Note: A Bulk Erase is the only way to reprogram code-protect bits from an ON state to an OFF state.

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TABLE 3-2: BULK ERASE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 05	MOVLW 05h
0000	6E F6	MOVWF TBLPTRL
1100	3F 3F	Write 3F3Fh to 3C0005h
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 04	MOVLW 04h
0000	6E F6	MOVWF TBLPTRL
1100	8F 8F	Write 8F8Fh TO 3C0004h to erase entire device. NOP Hold PGD low until erase completes.
0000	00 00	
0000	00 00	

FIGURE 3-1: BULK ERASE FLOW



PIC18F2XXX/4XXX FAMILY

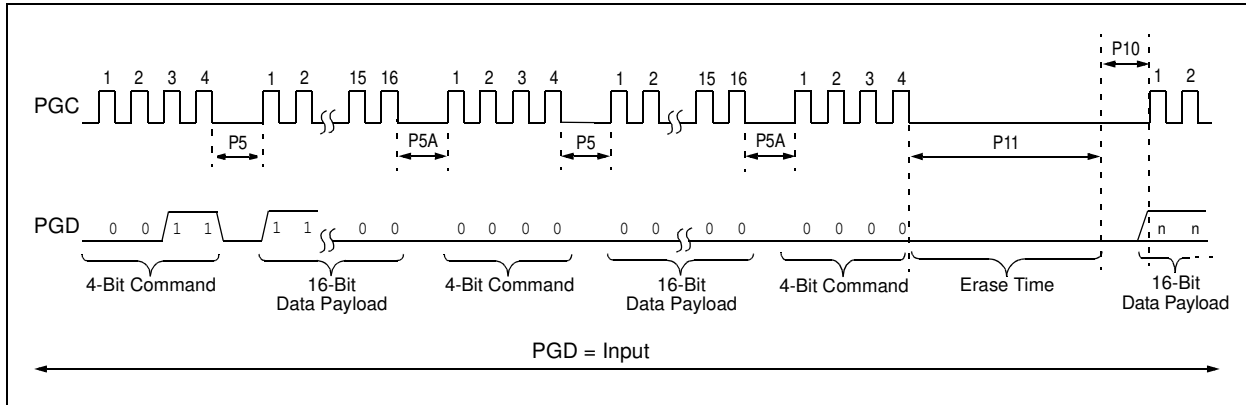
3.1.2 LOW-VOLTAGE ICSP BULK ERASE

When using low-voltage ICSP, the part must be supplied by the voltage specified in Parameter D111 if a Bulk Erase is to be executed. All other Bulk Erase details, as described above, apply.

If it is determined that a program memory erase must be performed at a supply voltage below the Bulk Erase limit, refer to the erase methodology described in [Section 3.1.3 “ICSP Row Erase”](#) and [Section 3.2.1 “Modifying Code Memory”](#).

If it is determined that a data EEPROM erase (selected devices only, see [Section 3.3 “Data EEPROM Programming”](#)) must be performed at a supply voltage below the Bulk Erase limit, follow the methodology described in [Section 3.3 “Data EEPROM Programming”](#) and write ‘1’s to the array.

FIGURE 3-2: BULK ERASE TIMING



3.1.3 ICSP ROW ERASE

Regardless of whether high or low-voltage ICSP is used, it is possible to erase one row (64 bytes of data), provided the block is not code or write-protected. Rows are located at static boundaries, beginning at program memory address, 000000h, extending to the internal program memory limit (see [Section 2.3 “Memory Maps”](#)).

The Row Erase duration is externally timed and is controlled by PGC. After the WR bit in EECON1 is set, a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by Parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to Row Erase a PIC18F2XXX/4XXX Family device is shown in [Table 3-3](#). The flowchart, shown in [Figure 3-3](#), depicts the logic necessary to completely erase a PIC18F2XXX/4XXX Family device. The timing diagram that details the Start Programming command and Parameters P9 and P10 is shown in [Figure 3-5](#).

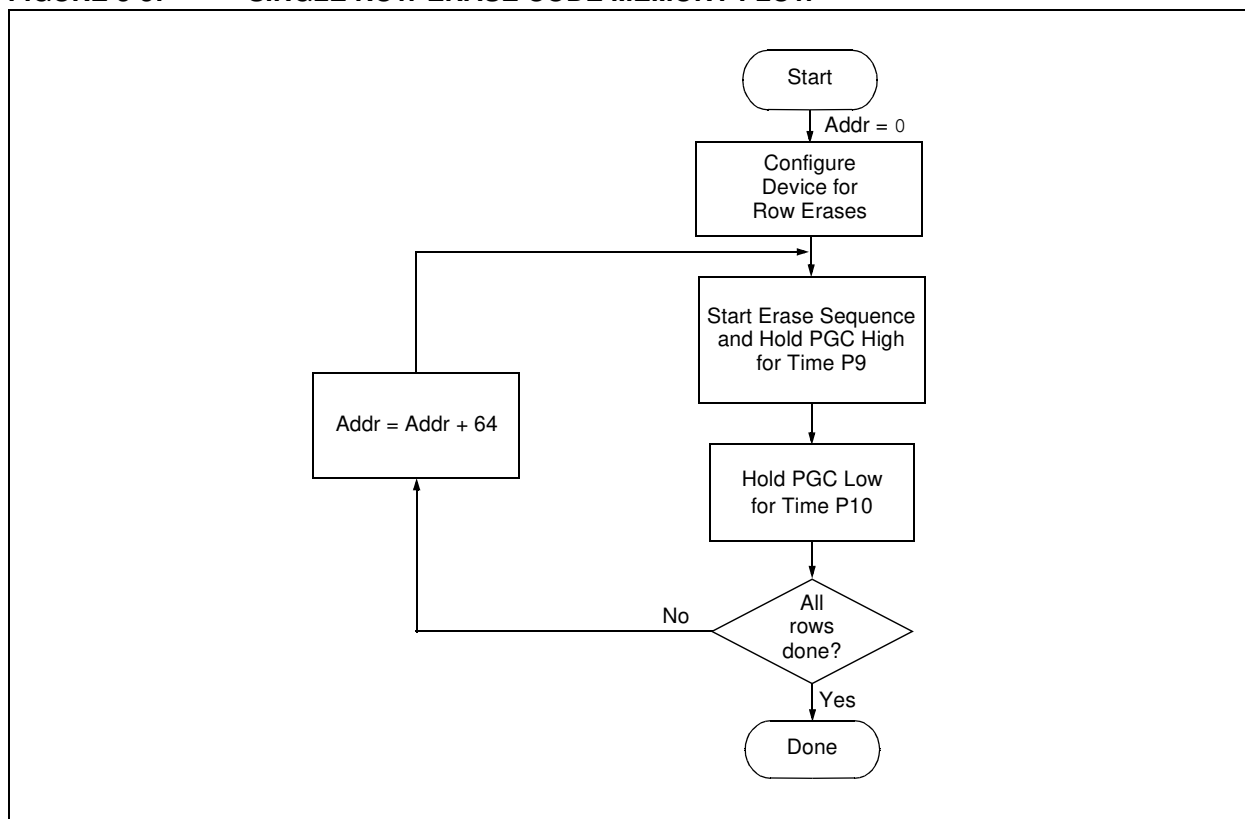
Note: The TBLPTR register can point to any byte within the row intended for erase.

PIC18F2XXX/4XXX FAMILY

TABLE 3-3: ERASE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory and enable writes.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
0000	84 A6	BSF EECON1, WREN
Step 2: Point to first row in code memory.		
0000	6A F8	CLRF TBLPTRU
0000	6A F7	CLRF TBLPTRH
0000	6A F6	CLRF TBLPTRL
Step 3: Enable erase and erase single row.		
0000	88 A6	BSF EECON1, FREE
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
Step 4: Repeat Step 3, with the Address Pointer incremented by 64 until all rows are erased.		

FIGURE 3-3: SINGLE ROW ERASE CODE MEMORY FLOW



PIC18F2XXX/4XXX FAMILY

3.2 Code Memory Programming

Programming code memory is accomplished by first loading data into the write buffer and then initiating a programming sequence. The write and erase buffer sizes, shown in [Table 3-4](#), can be mapped to any location of the same size, beginning at 000000h. The actual memory write sequence takes the contents of this buffer and programs the proper amount of code memory that contains the Table Pointer.

The programming duration is externally timed and is controlled by PGC. After a Start Programming command is issued (4-bit command, '1111'), a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by Parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to program a PIC18F2XXX/4XXX Family device is shown in [Table 3-5](#). The flowchart, shown in [Figure 3-4](#), depicts the logic necessary to completely write a PIC18F2XXX/4XXX Family device. The timing diagram that details the Start Programming command and Parameters P9 and P10 is shown in [Figure 3-5](#).

Note: The TBLPTR register must point to the same region when initiating the programming sequence as it did when the write buffers were loaded.

TABLE 3-4: WRITE AND ERASE BUFFER SIZES

Devices (Arranged by Family)	Write Buffer Size (Bytes)	Erase Buffer Size (Bytes)
PIC18F2221, PIC18F2321, PIC18F4221, PIC18F4321	8	64
PIC18F2450, PIC18F4450	16	64
PIC18F2410, PIC18F2510, PIC18F4410, PIC18F4510	32	64
PIC18F2420, PIC18F2520, PIC18F4420, PIC18F4520		
PIC18F2423, PIC18F2523, PIC18F4423, PIC18F4523		
PIC18F2480, PIC18F2580, PIC18F4480, PIC18F4580		
PIC18F2455, PIC18F2550, PIC18F4455, PIC18F4550		
PIC18F2458, PIC18F2553, PIC18F4458, PIC18F4553		
PIC18F2515, PIC18F2610, PIC18F4515, PIC18F4610	64	64
PIC18F2525, PIC18F2620, PIC18F4525, PIC18F4620		
PIC18F2585, PIC18F2680, PIC18F4585, PIC18F4680		
PIC18F2682, PIC18F2685, PIC18F4682, PIC18F4685		

PIC18F2XXX/4XXX FAMILY

TABLE 3-5: WRITE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory and enable writes.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Load write buffer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 3: Repeat for all but the last two bytes.		
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
Step 4: Load write buffer for last two bytes.		
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
To continue writing data, repeat Steps 2 through 4, where the Address Pointer is incremented by 2 at each iteration of the loop.		