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16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, Op Amps and Advanced Analog

Operating Conditions

- 3.0V to 3.6V, -40°C to +85°C, DC to 70 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 60 MIPS

Core: 16-Bit dsPIC33E/PIC24E CPU

- Code Efficient (C and Assembly) Architecture
- Two 40-Bit-Wide Accumulators
- Single Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support

Clock Management

- 1.0% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 0.6 mA/MHz Dynamic Current (typical)
- 30 μ A IPD Current (typical)

High-Speed PWM

- Up to Three PWM Pairs with Independent Timing
- Dead Time for Rising and Falling Edges
- 7.14 ns PWM Resolution
- PWM Support for:
 - DC/DC, AC/DC, Inverters, PFC, Lighting
 - BLDC, PMSM, ACIM, SRM
- Programmable Fault Inputs
- Flexible Trigger Configurations for ADC Conversions

Advanced Analog Features

- ADC module:
 - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
 - Six analog inputs on 28-pin devices and up to 16 analog inputs on 64-pin devices
- Flexible and Independent ADC Trigger Sources
- Up to Three Op Amp/Comparators with Direct Connection to the ADC module:
 - Additional dedicated comparator
 - Programmable references with 32 voltage points
- Charge Time Measurement Unit (CTMU):
 - Supports mTouch™ capacitive touch sensing
 - Provides high-resolution time measurement (1 ns)
 - On-chip temperature measurement

Timers/Output Compare/Input Capture

- 12 General Purpose Timers:
 - Five 16-bit and up to two 32-bit timers/counters
 - Four Output Compare (OC) modules, configurable as timers/counters
 - PTG module with two configurable timers/counters
 - 32-bit Quadrature Encoder Interface (QEI) module, configurable as a timer/counter
- Four Input Capture (IC) modules
- Peripheral Pin Select (PPS) to allow Function Remap
- Peripheral Trigger Generator (PTG) for Scheduling Complex Sequences

Communication Interfaces

- Two UART modules (17.5 Mbps):
 - With support for LIN/J2602 protocols and IrDA®
- Two 4-Wire SPI modules (15 Mbps)
- ECAN™ module (1 Mbaud) CAN 2.0B Support
- Two I²C™ modules (up to 1 Mbaud) with SMBus Support
- PPS to allow Function Remap
- Programmable Cyclic Redundancy Check (CRC)

Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- UART, SPI, ADC, ECAN, IC, OC and Timers

Input/Output

- Sink/Source 12 mA or 6 mA, Pin-Specific for Standard V_{OH}/V_{OL}, up to 22 or 14 mA, respectively for Non-Standard V_{OH1}
- 5V Tolerant Pins
- Peripheral Pin Select (PPS) to allow Digital Function Remapping
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Up to 5 mA Overvoltage Clamp Current
- Change Notification Interrupts on All I/O Pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C) Planned
- AEC-Q100 REVG (Grade 0, -40°C to +150°C) Planned
- Class B Safety Library, IEC 60730

Debugger Development Support

- In-Circuit and In-Application Programming
- Two Program and Two Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

**dsPIC33EPXXXGP50X,
dsPIC33EPXXXMC20X/50X AND
PIC24EPXXXGP/MC20X PRODUCT
FAMILIES**

The device names, pin counts, memory sizes and peripheral availability of each device are listed in [Table 1](#) (General Purpose Families) and [Table 2](#) (Motor Control Families). Their pinout diagrams appear on the following pages.

TABLE 1: dsPIC33EPXXXGP50X and PIC24EPXXXGP20X GENERAL PURPOSE FAMILIES

Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbyte)	Remappable Peripherals						I ² C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages	
				16-Bit/32-Bit Timers	Input Capture	Output Compare	UART	SPI ⁽²⁾	ECAN™ Technology										External Interrupts ⁽³⁾
PIC24EP32GP202	512	32	4	5	4	4	2	2	—	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁴⁾ , QFN-S
PIC24EP64GP202	1024	64	8																
PIC24EP128GP202	1024	128	16																
PIC24EP256GP202	1024	256	32																
PIC24EP512GP202	1024	512	48	5	4	4	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
PIC24EP32GP203	512	32	4																
PIC24EP64GP203	1024	64	8																
PIC24EP32GP204	512	32	4																
PIC24EP64GP204	1024	64	8	5	4	4	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA ⁽⁴⁾ , TQFP, QFN, UQFN
PIC24EP128GP204	1024	128	16																
PIC24EP256GP204	1024	256	32																
PIC24EP512GP204	1024	512	48																
PIC24EP64GP206	1024	64	8	5	4	4	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
PIC24EP128GP206	1024	128	16																
PIC24EP256GP206	1024	256	32																
PIC24EP512GP206	1024	512	48																
dsPIC33EP32GP502	512	32	4	5	4	4	2	2	1	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁴⁾ , QFN-S
dsPIC33EP64GP502	1024	64	8																
dsPIC33EP128GP502	1024	128	16																
dsPIC33EP256GP502	1024	256	32																
dsPIC33EP512GP502	1024	512	48	5	4	4	2	2	1	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32GP503	512	32	4																
dsPIC33EP64GP503	1024	64	8																
dsPIC33EP32GP504	512	32	4																
dsPIC33EP64GP504	1024	64	8	5	4	4	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA ⁽⁴⁾ , TQFP, QFN, UQFN
dsPIC33EP128GP504	1024	128	16																
dsPIC33EP256GP504	1024	256	32																
dsPIC33EP512GP504	1024	512	48																
dsPIC33EP64GP506	1024	64	8	5	4	4	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP128GP506	1024	128	16																
dsPIC33EP256GP506	1024	256	32																
dsPIC33EP512GP506	1024	512	48																

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to [Section 25.0 "Op Amp/Comparator Module"](#) for details.

2: Only SPI2 is remappable.

3: INT0 is not remappable.

4: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES

Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals								i ² C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages	
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology										External Interrupts ⁽³⁾
PIC24EP32MC202	512	32	4																		
PIC24EP64MC202	1024	64	8																		
PIC24EP128MC202	1024	128	16	5	4	4	6	1	2	2	—	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
PIC24EP256MC202	1024	256	32																		
PIC24EP512MC202	1024	512	48																		
PIC24EP32MC203	512	32	4	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
PIC24EP64MC203	1024	64	8																		
PIC24EP32MC204	512	32	4																		
PIC24EP64MC204	1024	64	8																		
PIC24EP128MC204	1024	128	16	5	4	4	6	1	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
PIC24EP256MC204	1024	256	32																		
PIC24EP512MC204	1024	512	48																		
PIC24EP64MC206	1024	64	8																		
PIC24EP128MC206	1024	128	16	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
PIC24EP256MC206	1024	256	32																		
PIC24EP512MC206	1024	512	48																		
dsPIC33EP32MC202	512	32	4																		
dsPIC33EP64MC202	1024	64	8																		
dsPIC33EP128MC202	1024	128	16	5	4	4	6	1	2	2	—	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
dsPIC33EP256MC202	1024	256	32																		
dsPIC33EP512MC202	1024	512	48																		
dsPIC33EP32MC203	512	32	4	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP64MC203	1024	64	8																		
dsPIC33EP32MC204	512	32	4																		
dsPIC33EP64MC204	1024	64	8																		
dsPIC33EP128MC204	1024	128	16	5	4	4	6	1	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
dsPIC33EP256MC204	1024	256	32																		
dsPIC33EP512MC204	1024	512	48																		
dsPIC33EP64MC206	1024	64	8																		
dsPIC33EP128MC206	1024	128	16	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP256MC206	1024	256	32																		
dsPIC33EP512MC206	1024	512	48																		
dsPIC33EP32MC502	512	32	4																		
dsPIC33EP64MC502	1024	64	8																		
dsPIC33EP128MC502	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
dsPIC33EP256MC502	1024	256	32																		
dsPIC33EP512MC502	1024	512	48																		
dsPIC33EP32MC503	512	32	4	5	4	4	6	1	2	2	1	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP64MC503	1024	64	8																		

- Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to [Section 25.0 “Op Amp/Comparator Module”](#) for details.
2: Only SPI2 is remappable.
3: INTO is not remappable.
4: Only the PWM Faults are remappable.
5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)

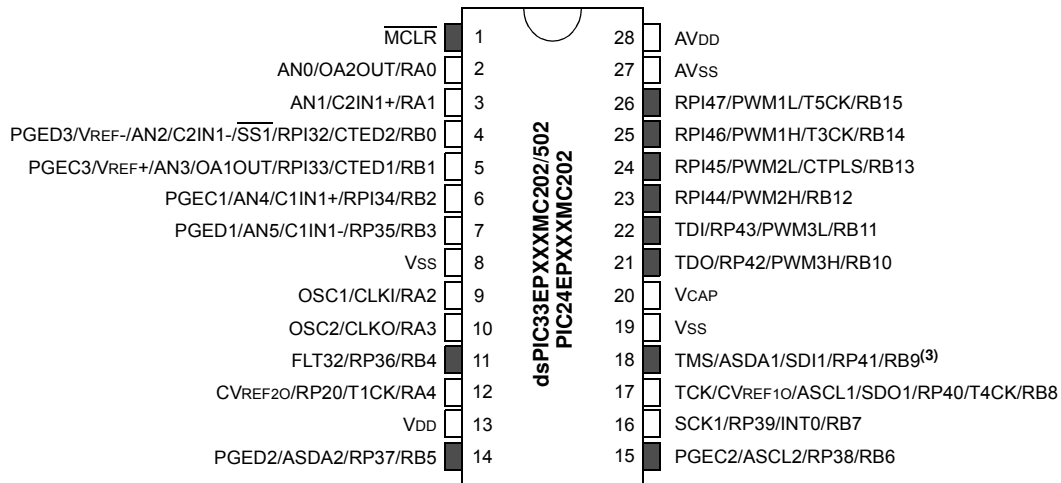
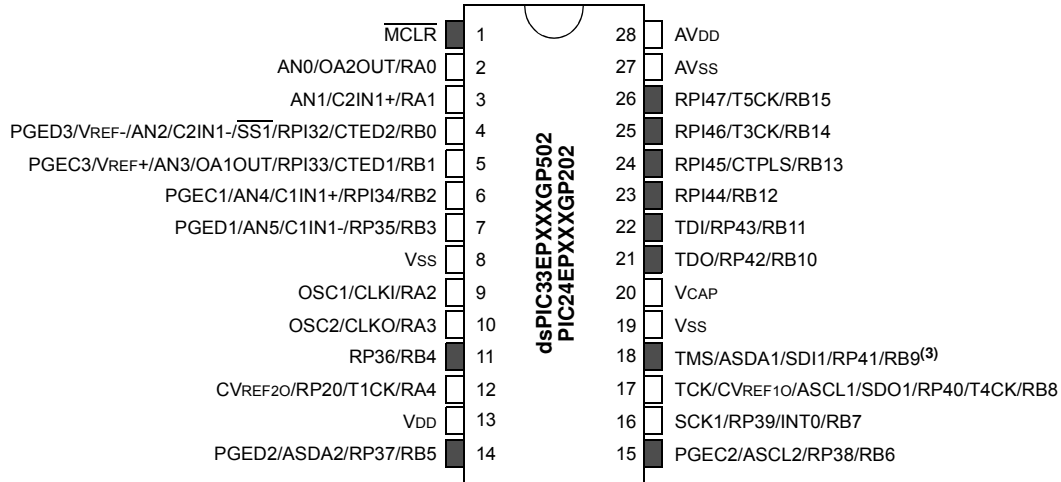
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals										CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages				
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	I ² C™												
dsPIC33EP32MC504	512	32	4																						
dsPIC33EP64MC504	1024	64	8																						
dsPIC33EP128MC504	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/48		VTLA ⁽⁵⁾ , TQFP, QFN, UQFN			
dsPIC33EP256MC504	1024	256	32																						
dsPIC33EP512MC504	1024	512	48																						
dsPIC33EP64MC506	1024	64	8																						
dsPIC33EP128MC506	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64		TQFP, QFN			
dsPIC33EP256MC506	1024	256	32																						
dsPIC33EP512MC506	1024	512	48																						

- Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to [Section 25.0 "Op Amp/Comparator Module"](#) for details.
2: Only SPI2 is remappable.
3: INTO is not remappable.
4: Only the PWM Faults are remappable.
5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP^(1,2)

■ = Pins are up to 5V tolerant

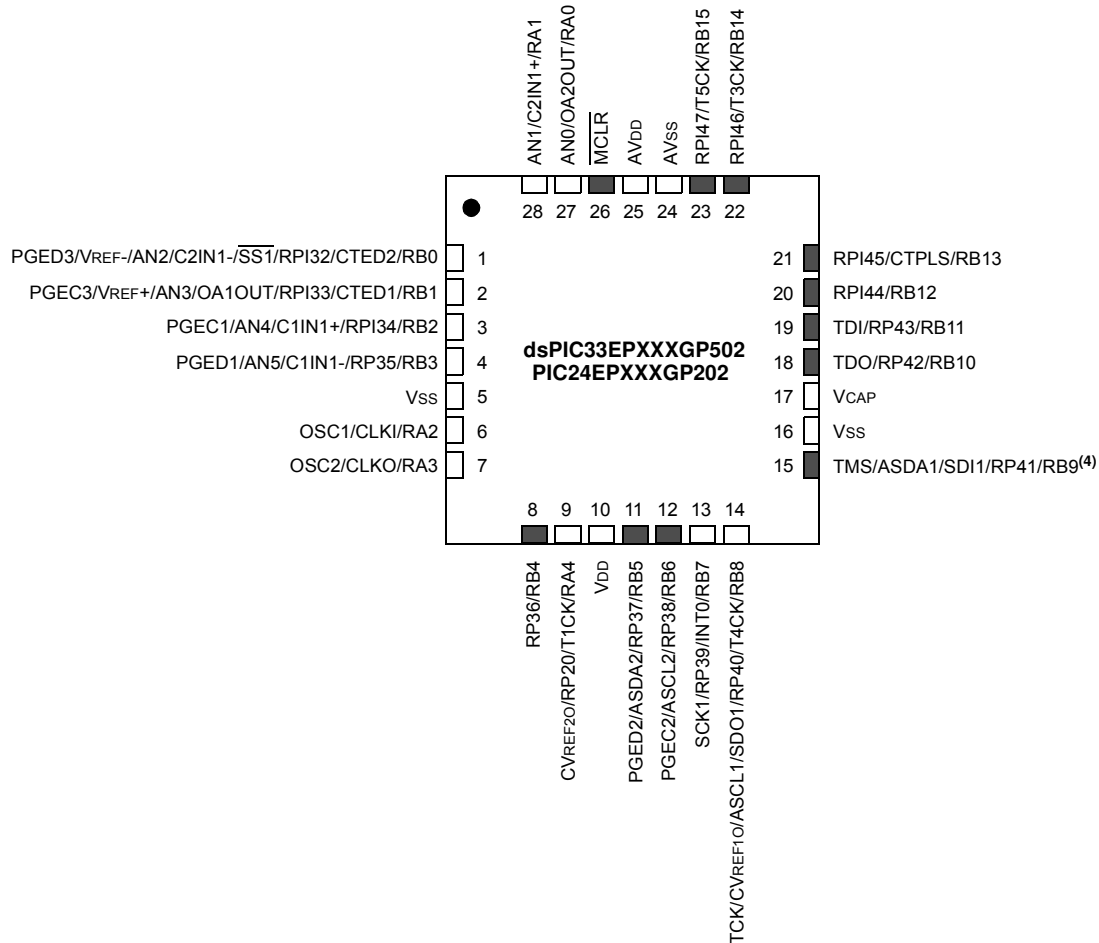


- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See [Section 11.0 “I/O Ports”](#) for more information.
- Note 3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

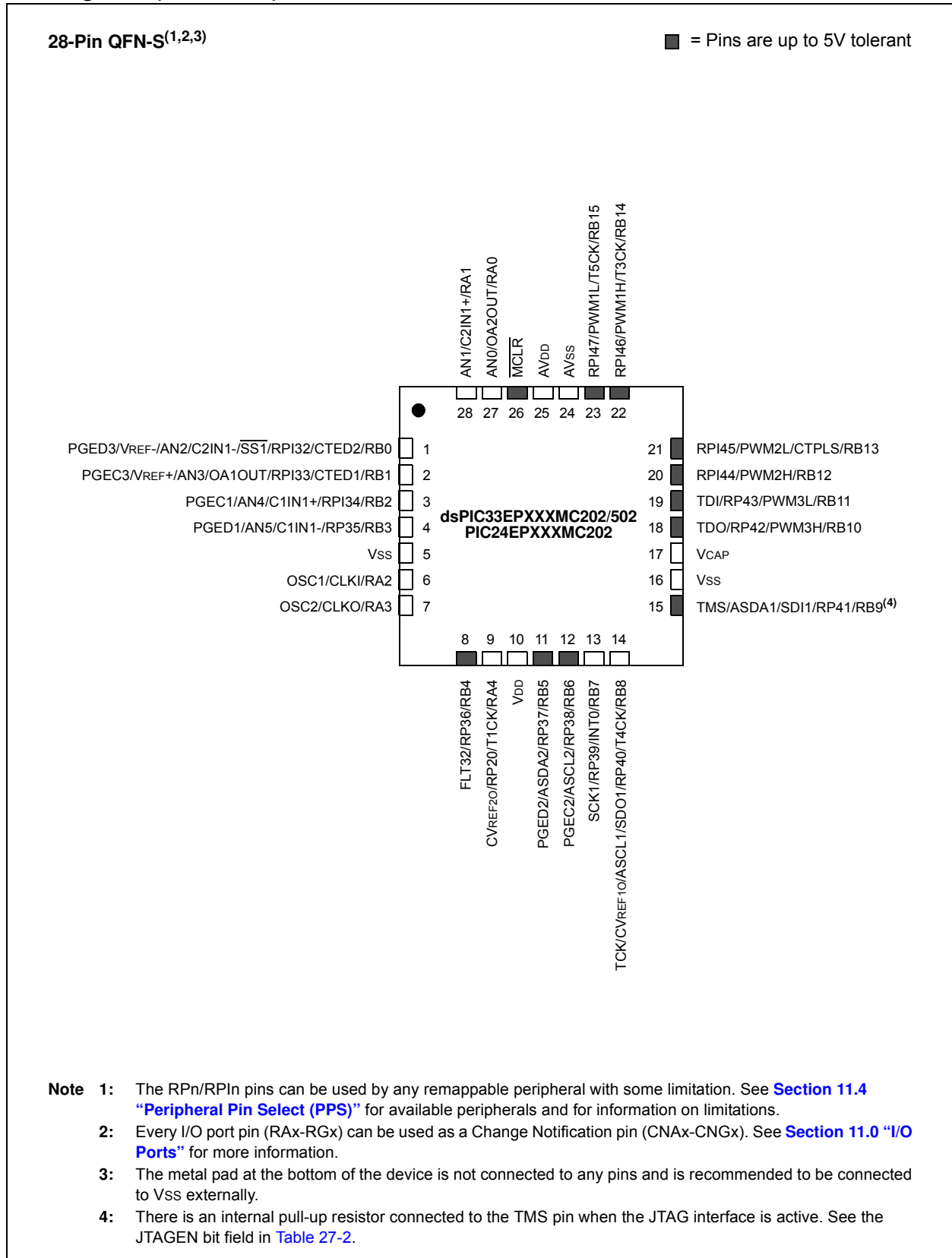
28-Pin QFN-S(1,2,3)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See [Section 11.4 "Peripheral Pin Select \(PPS\)"](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAx-CNGx). See [Section 11.0 "I/O Ports"](#) for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

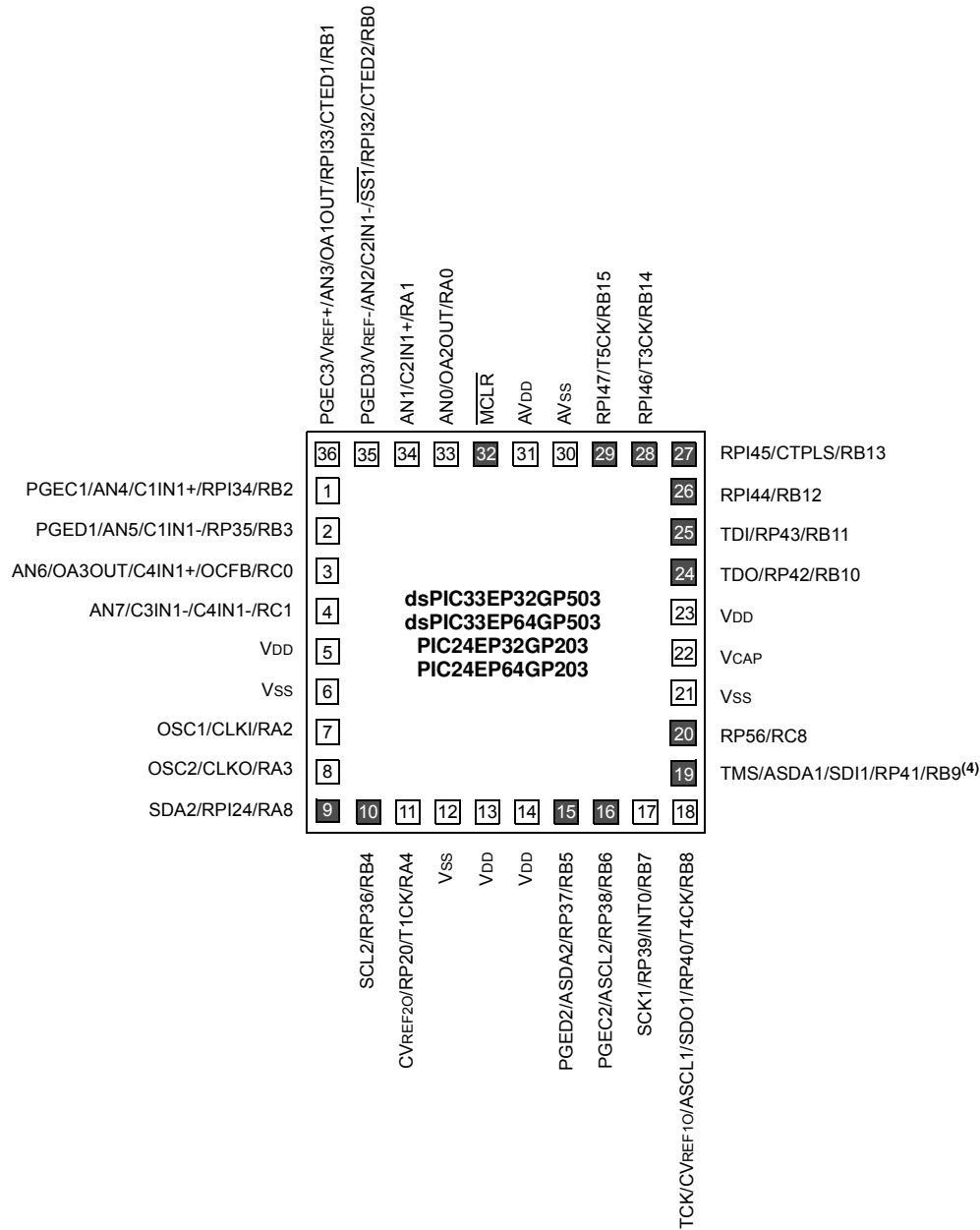


- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See [Section 11.0 “I/O Ports”](#) for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

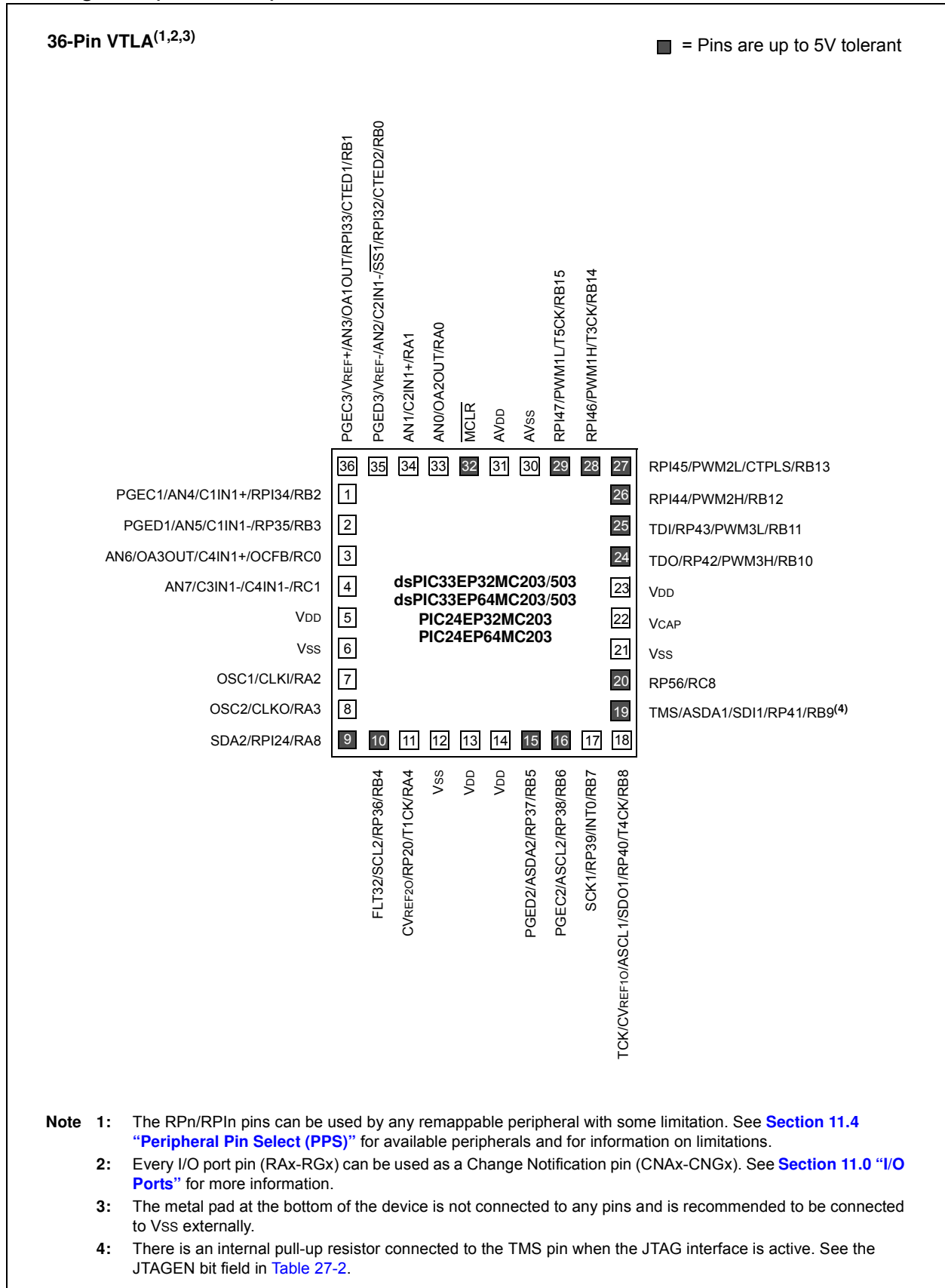
36-Pin VTLA^(1,2,3)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See [Section 11.0 “I/O Ports”](#) for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

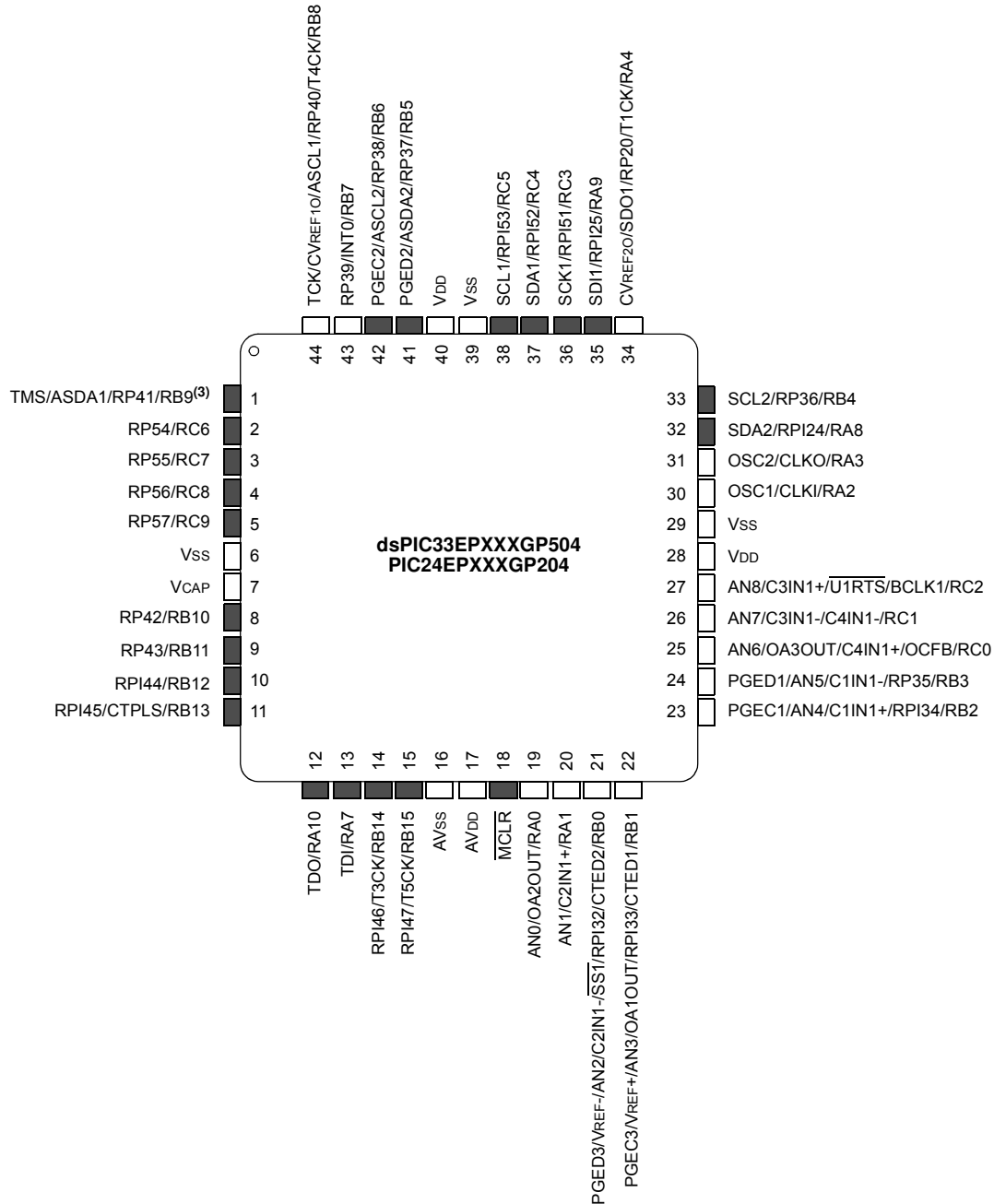
Pin Diagrams (Continued)



Pin Diagrams (Continued)

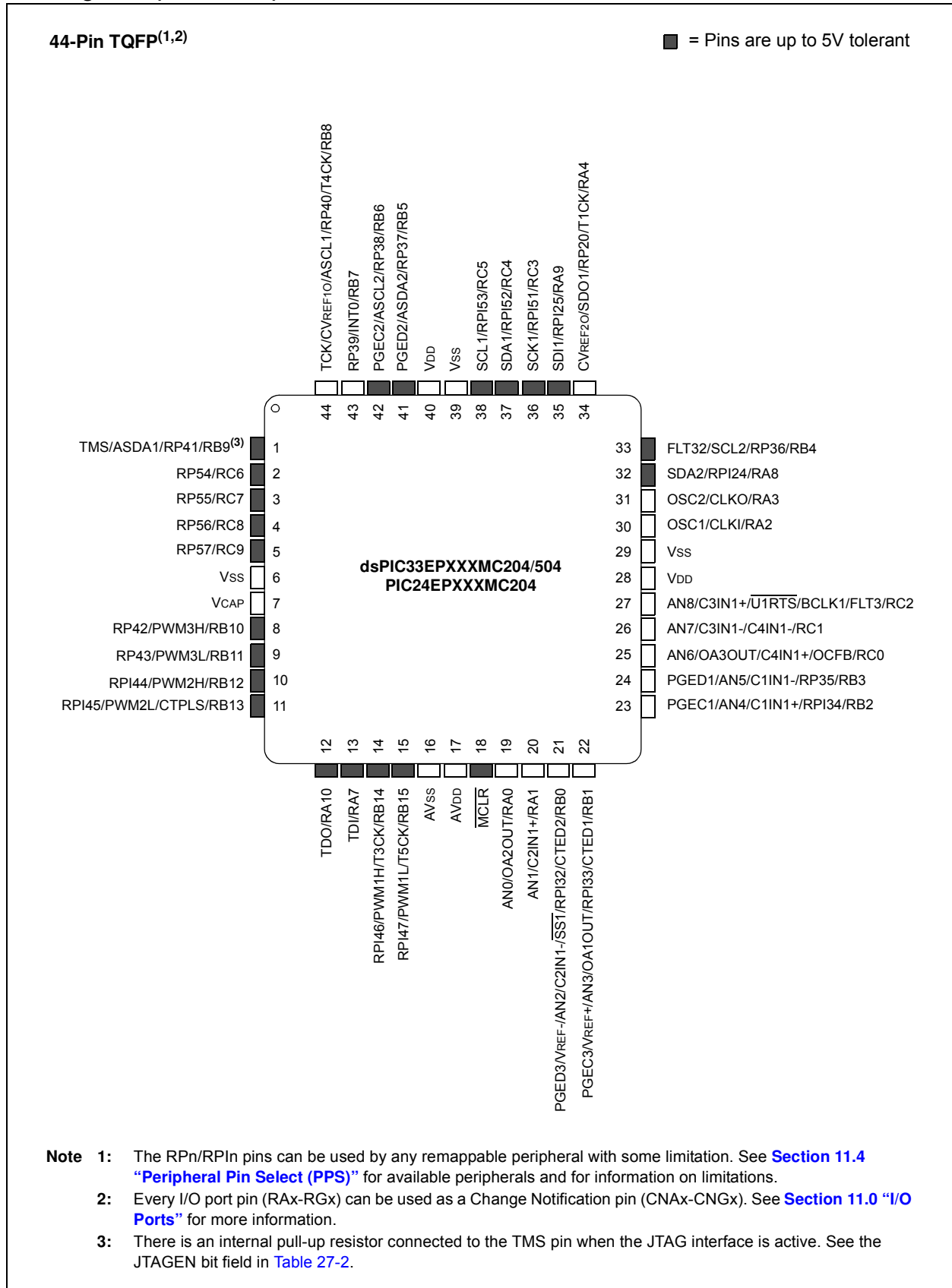
44-Pin TQFP^(1,2)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See [Section 11.0 “I/O Ports”](#) for more information.
- Note 3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

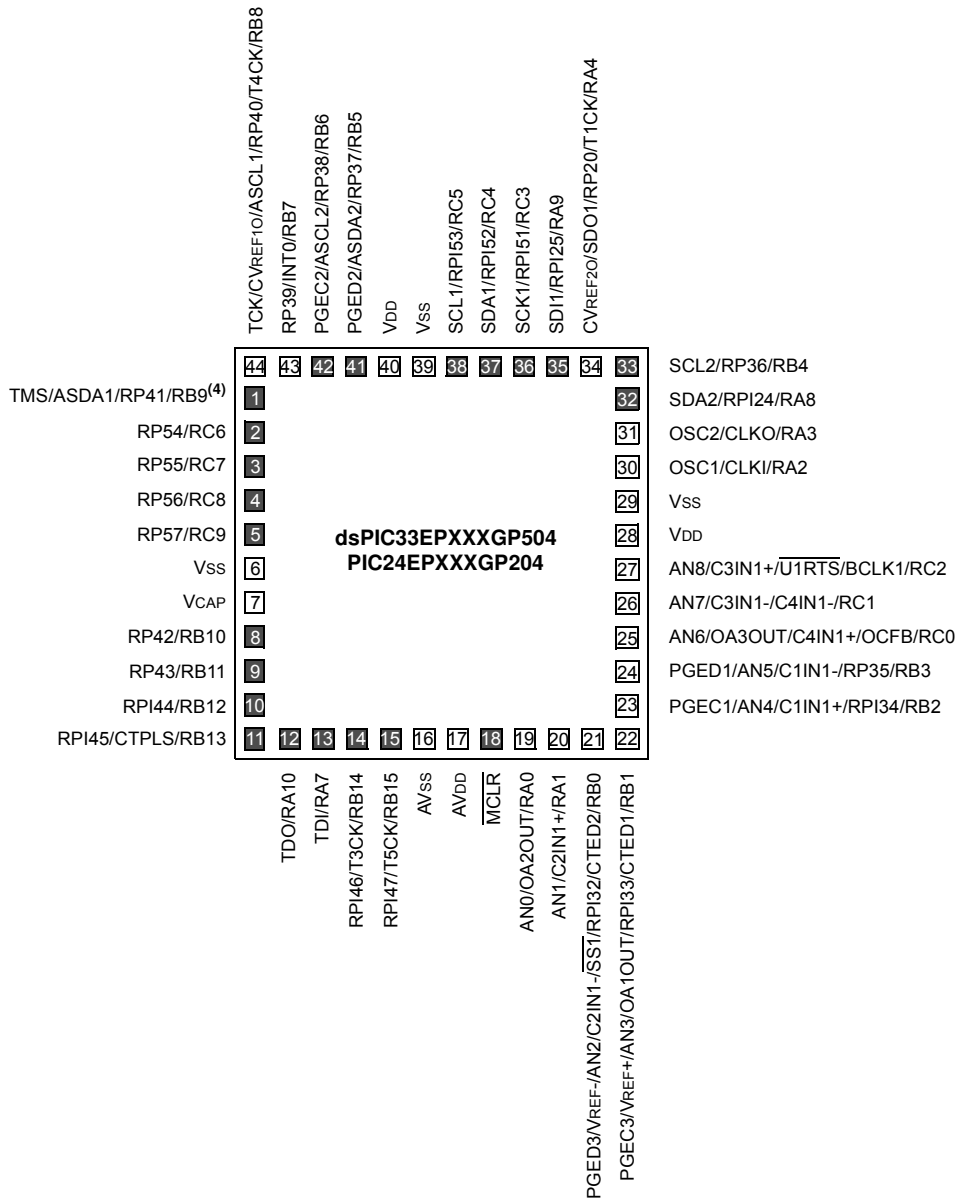
Pin Diagrams (Continued)



Pin Diagrams (Continued)

44-Pin VTLA^(1,2,3)

■ = Pins are up to 5V tolerant

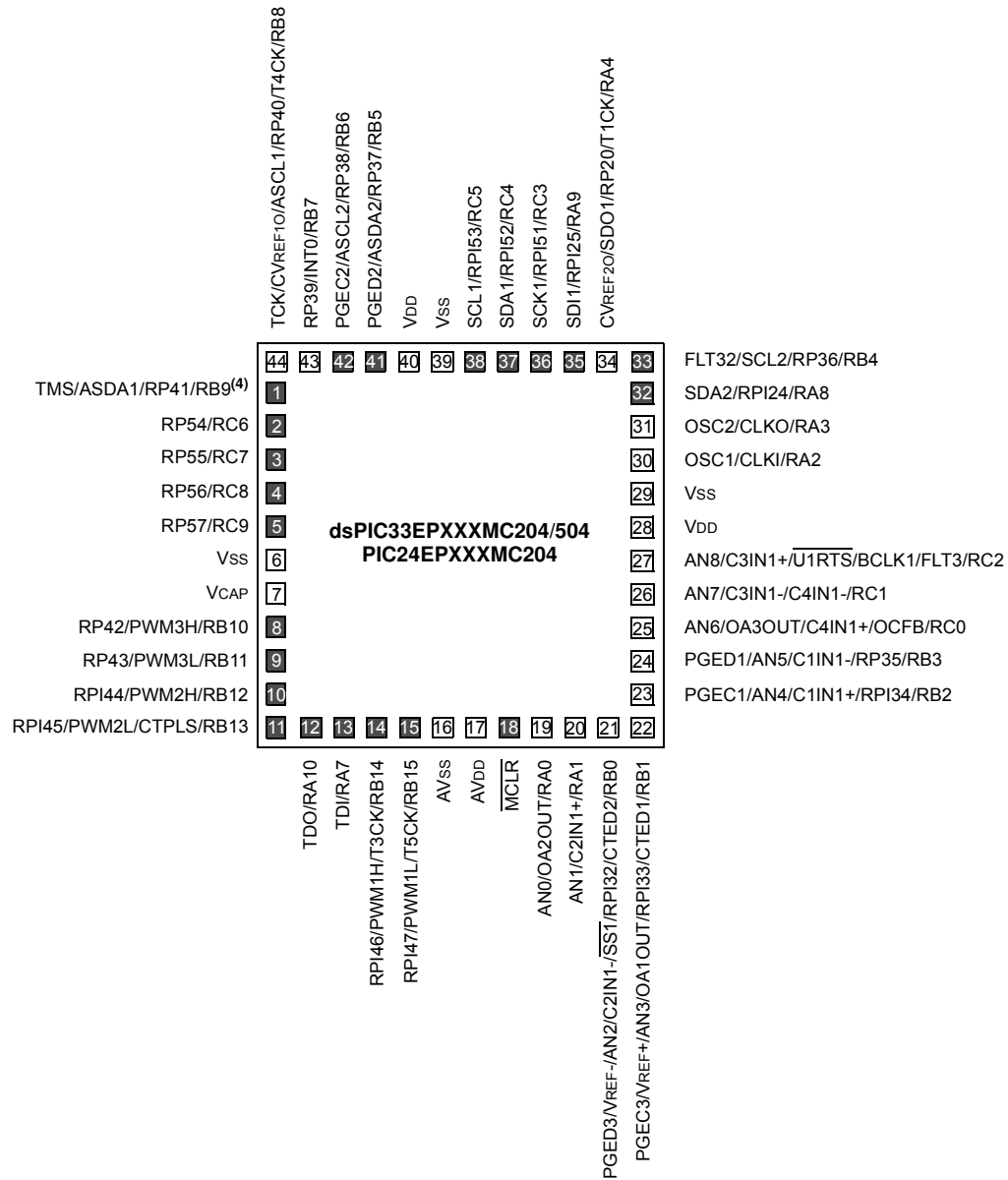


- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See [Section 11.0 “I/O Ports”](#) for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

44-Pin VTLA^(1,2,3)

■ = Pins are up to 5V tolerant

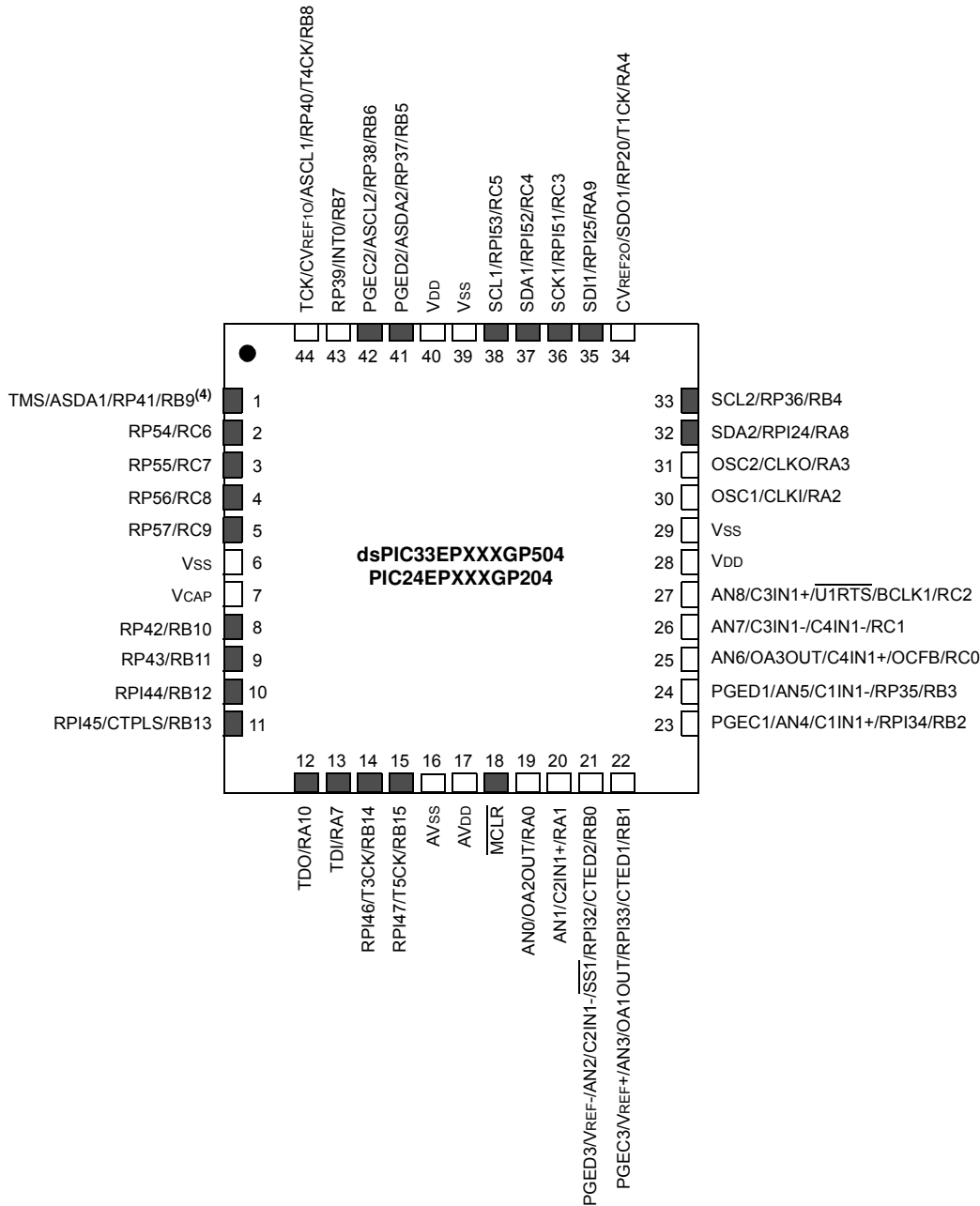


- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See [Section 11.0 “I/O Ports”](#) for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

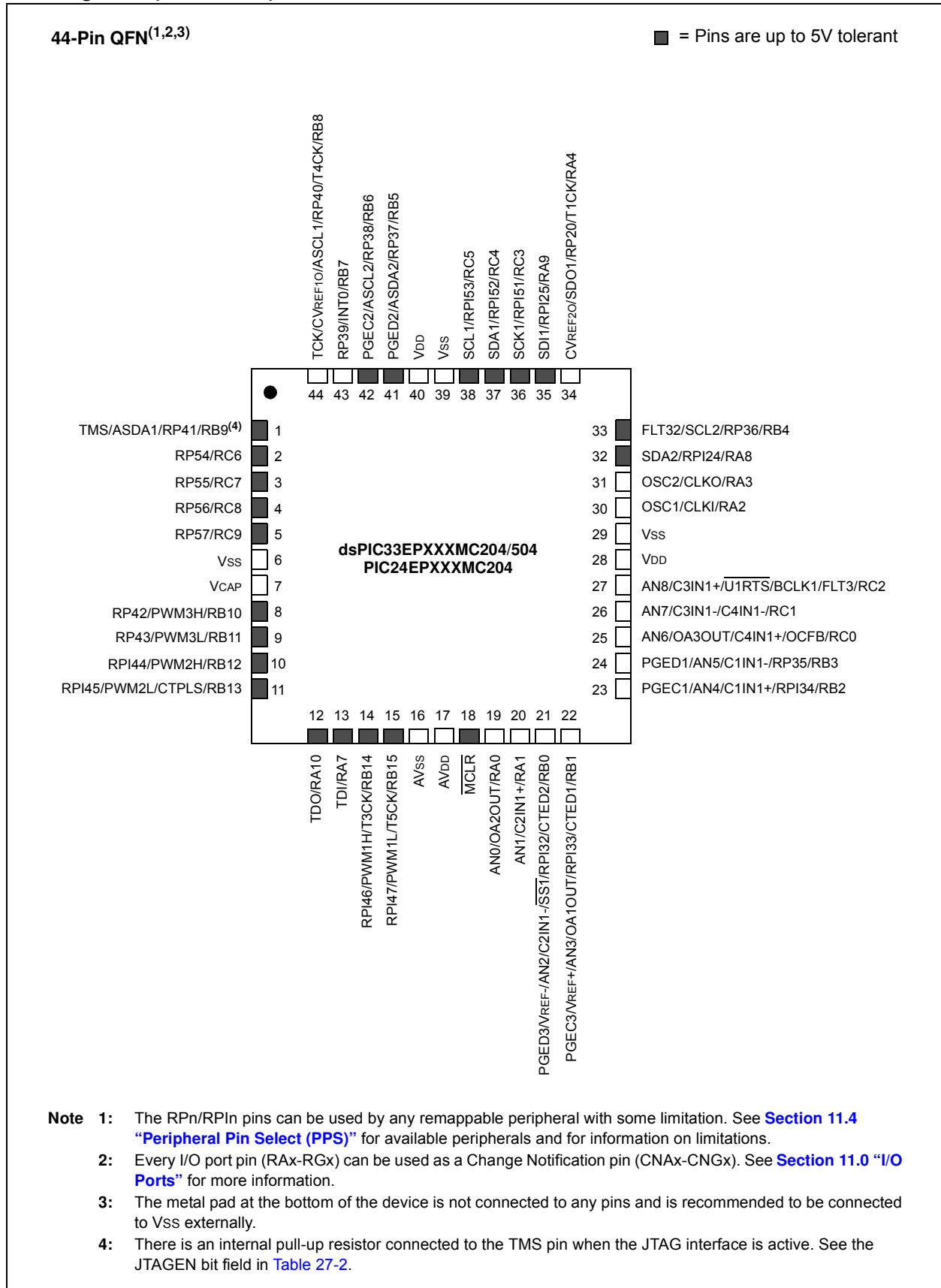
44-Pin QFN^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPI pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See [Section 11.0 “I/O Ports”](#) for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

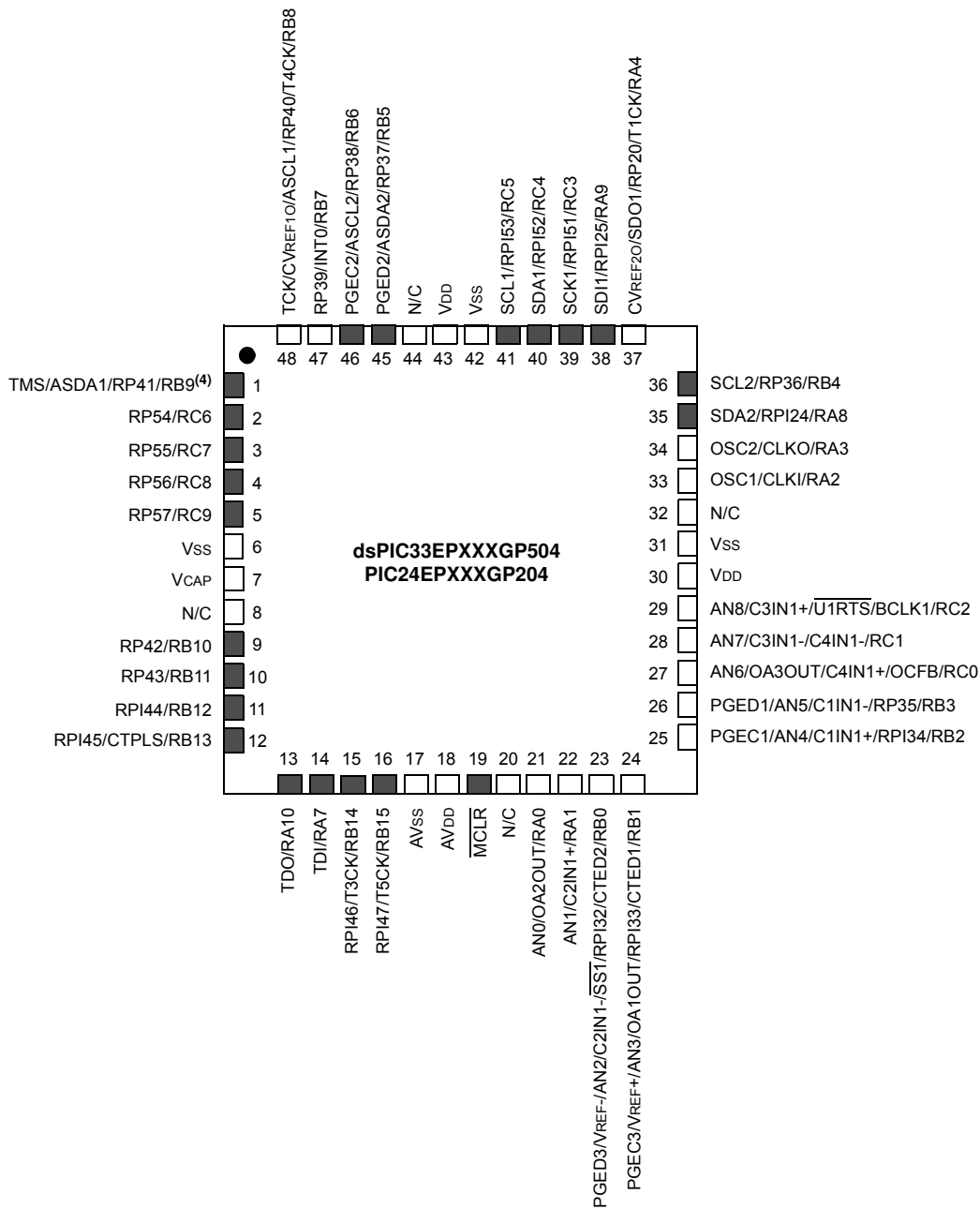


- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See [Section 11.0 “I/O Ports”](#) for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

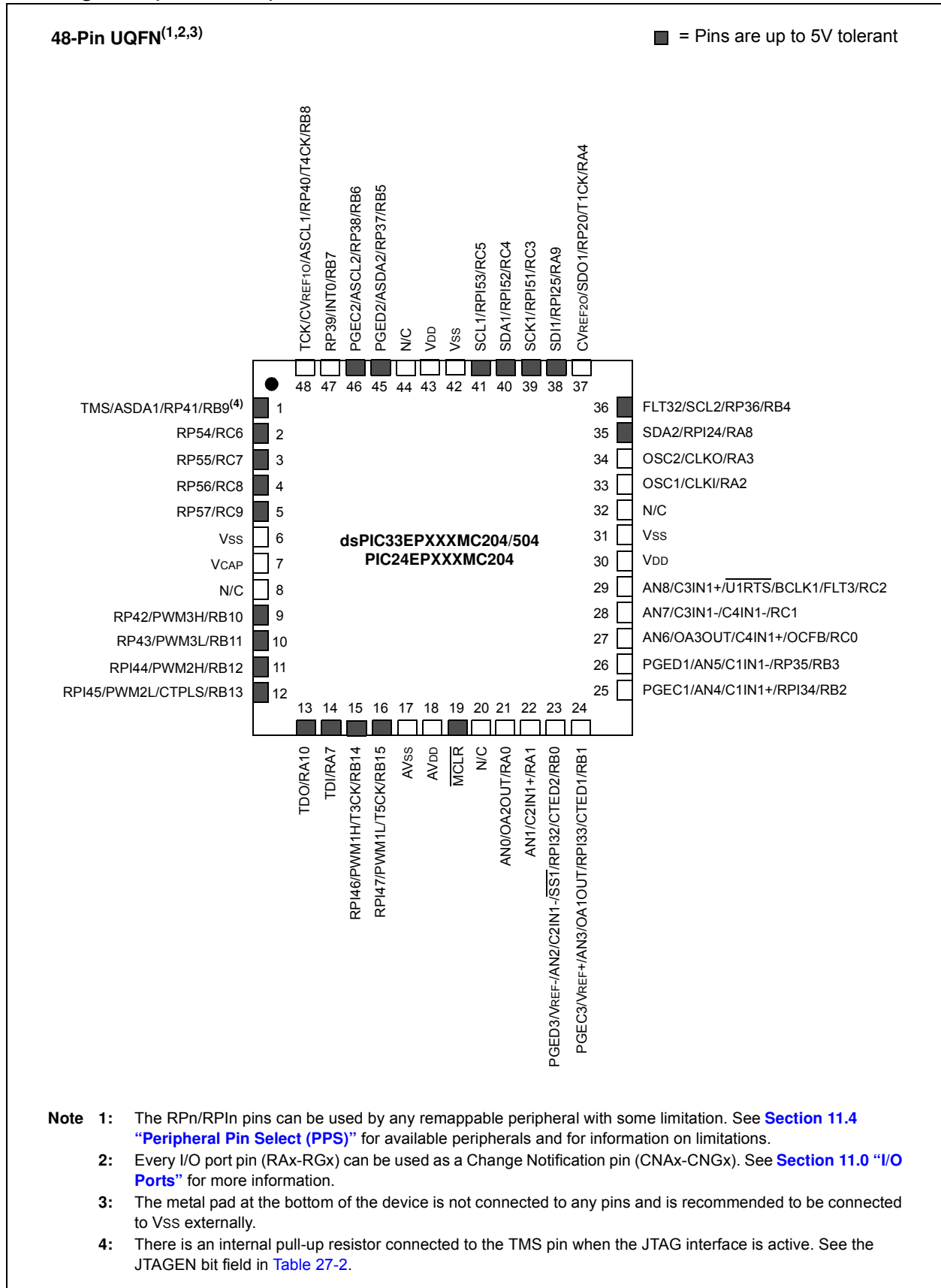
48-Pin UQFN^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPI pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See [Section 11.0 “I/O Ports”](#) for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

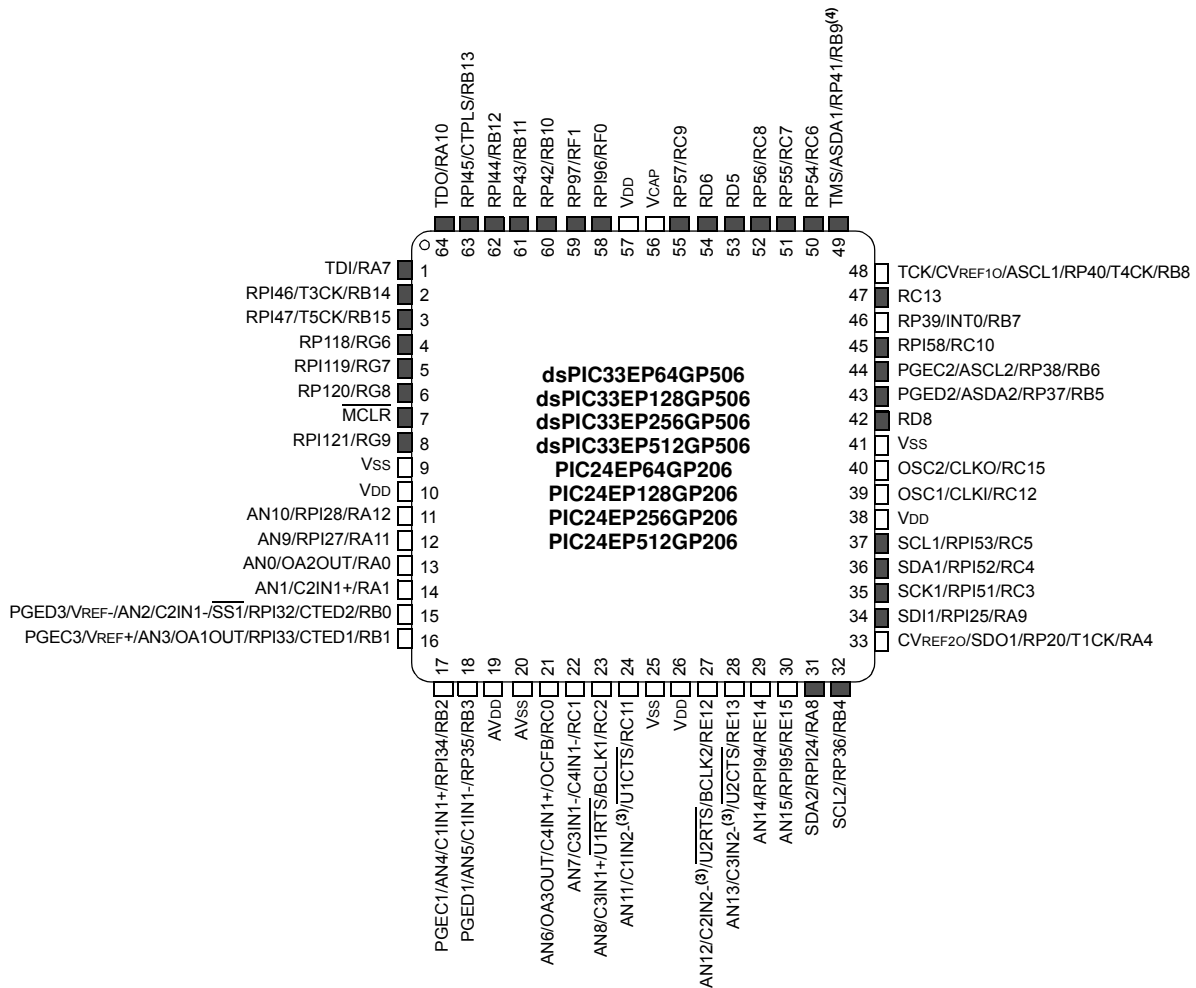


- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See [Section 11.0 “I/O Ports”](#) for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)

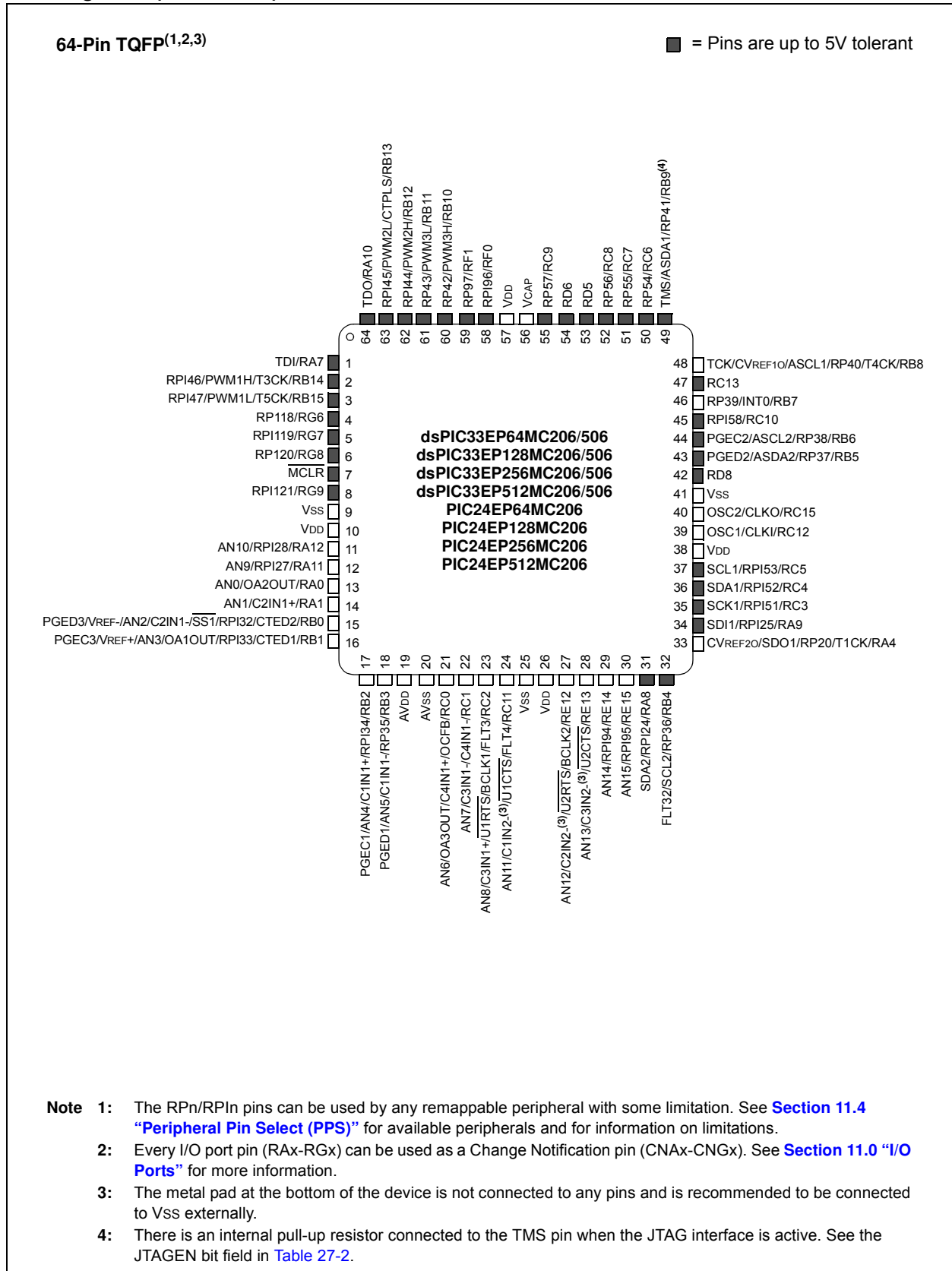
64-Pin TQFP^(1,2,3)

■ = Pins are up to 5V tolerant



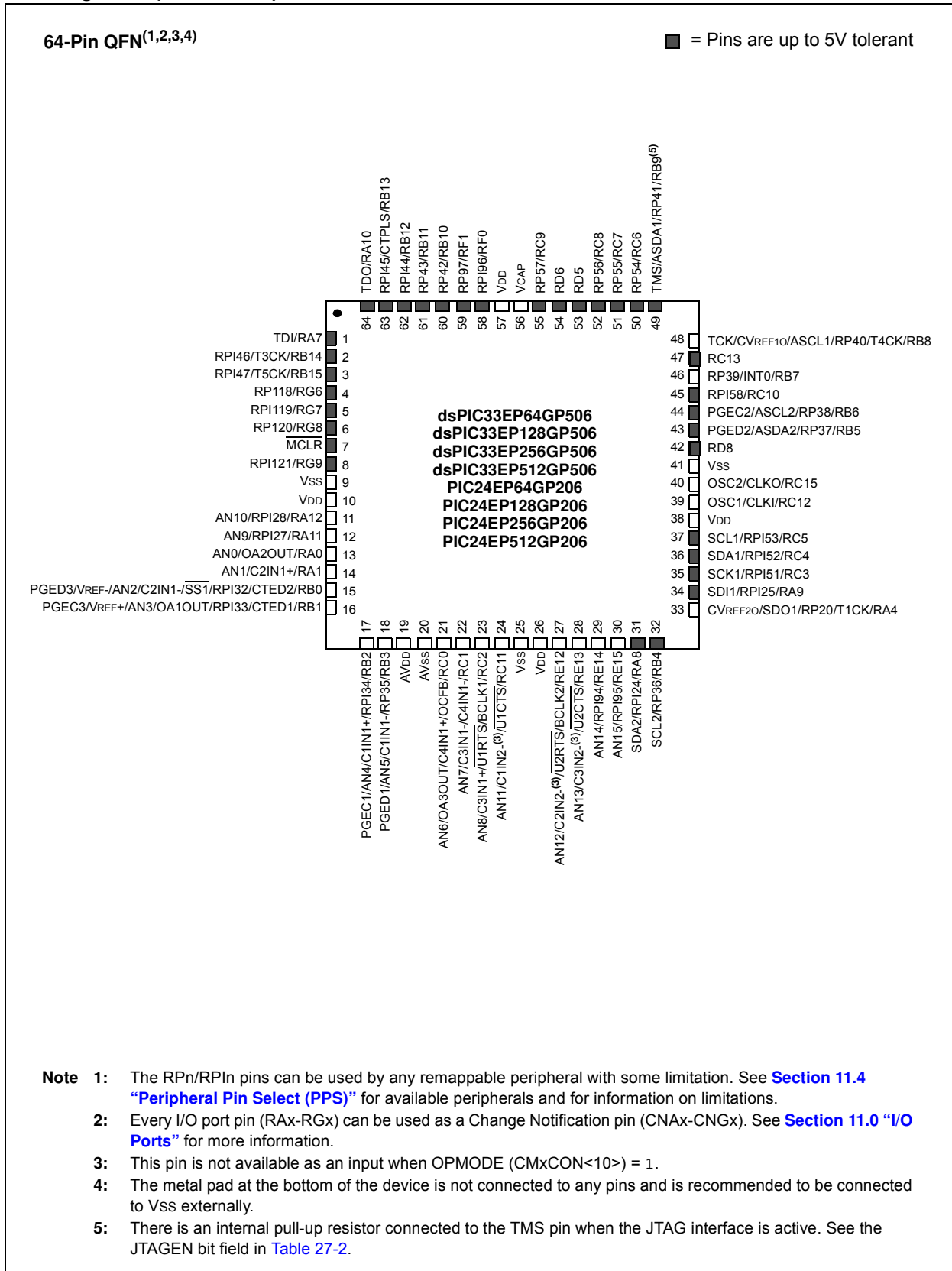
- Note**
- 1: The RPN/RPI pins can be used by any remappable peripheral with some limitation. See [Section 11.4 "Peripheral Pin Select \(PPS\)"](#) for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See [Section 11.0 "I/O Ports"](#) for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
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Pin Diagrams (Continued)



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See [Section 11.4 “Peripheral Pin Select \(PPS\)”](#) for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See [Section 11.0 “I/O Ports”](#) for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in [Table 27-2](#).

Pin Diagrams (Continued)



Pin Diagrams (Continued)

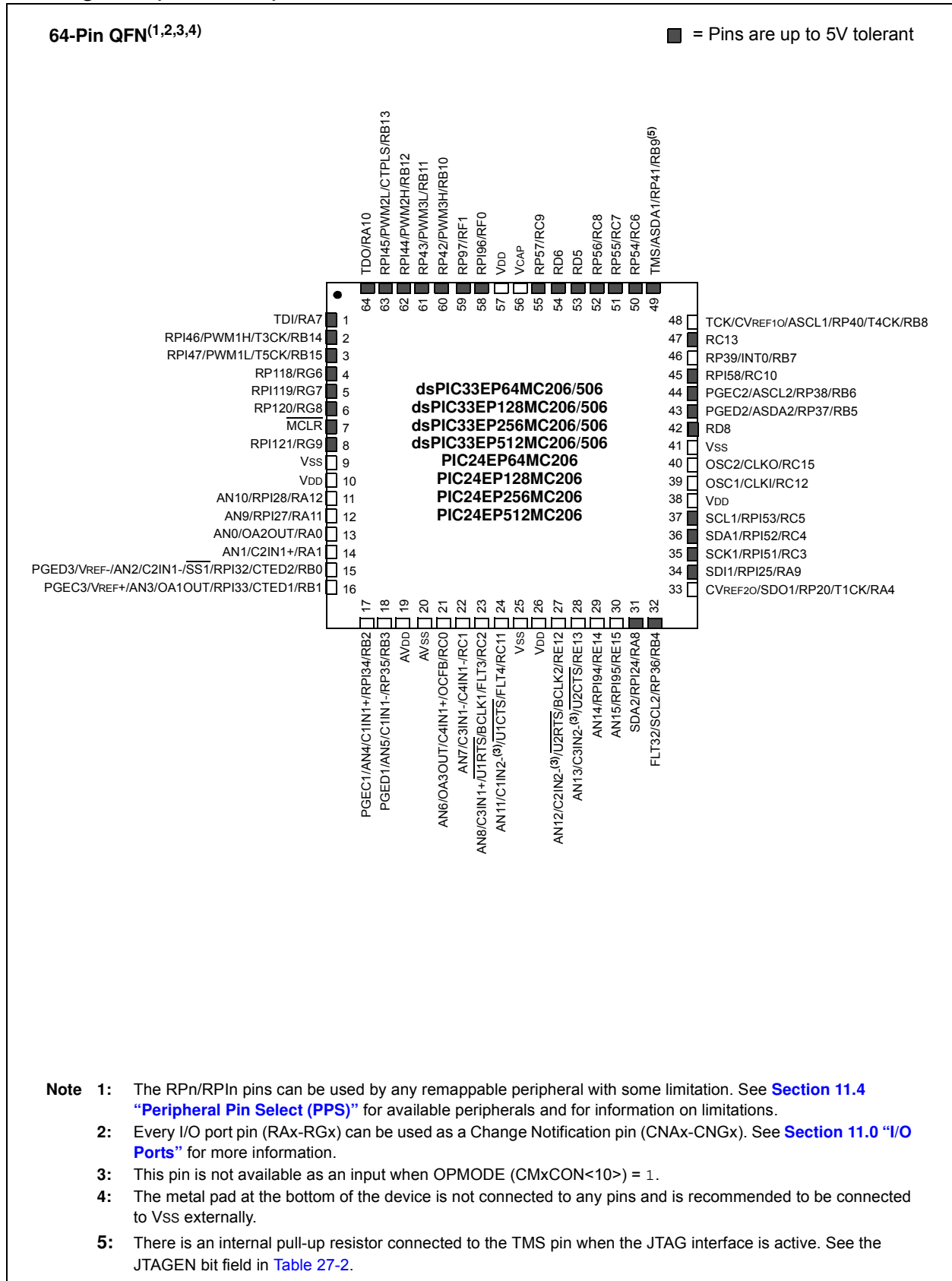


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Referenced Sources

This device data sheet is based on the following individual chapters of the “*dsPIC33/PIC24 Family Reference Manual*”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the [dsPIC33EP64MC506](#) product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- “**Introduction**” (DS70573)
- “**CPU**” (DS70359)
- “**Data Memory**” (DS70595)
- “**Program Memory**” (DS70613)
- “**Flash Programming**” (DS70609)
- “**Interrupts**” (DS70600)
- “**Oscillator**” (DS70580)
- “**Reset**” (DS70602)
- “**Watchdog Timer and Power-Saving Modes**” (DS70615)
- “**I/O Ports**” (DS70598)
- “**Timers**” (DS70362)
- “**Input Capture**” (DS70352)
- “**Output Compare**” (DS70358)
- “**High-Speed PWM**” (DS70645)
- “**Quadrature Encoder Interface (QEI)**” (DS70601)
- “**Analog-to-Digital Converter (ADC)**” (DS70621)
- “**UART**” (DS70582)
- “**Serial Peripheral Interface (SPI)**” (DS70569)
- “**Inter-Integrated Circuit (I²C™)**” (DS70330)
- “**Enhanced Controller Area Network (ECAN™)**” (DS70353)
- “**Direct Memory Access (DMA)**” (DS70348)
- “**CodeGuard™ Security**” (DS70634)
- “**Programming and Diagnostics**” (DS70608)
- “**Op Amp/Comparator**” (DS70357)
- “**Programmable Cyclic Redundancy Check (CRC)**” (DS70346)
- “**Device Configuration**” (DS70618)
- “**Peripheral Trigger Generator (PTG)**” (DS70669)
- “**Charge Time Measurement Unit (CTMU)**” (DS70661)

