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PIC24FJ128GA310 FAMILY

64/80/100-Pin, General Purpose, 16-Bit Flash Microcontrollers with LCD Controller and XLP Technology

Extreme Low-Power Features:

- Multiple Power Management Options for Extreme Power Reduction:
  - VBAT allows the device to transition to a backup battery for the lowest power consumption with RTCC
  - Deep Sleep allows near total power-down with the ability to wake-up on external triggers
  - Sleep and Idle modes selectively shut down peripherals and/or core for substantial power reduction and fast wake-up
  - Doze mode allows CPU to run at a lower clock speed than peripherals
- Alternate Clock modes Allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction
- Extreme Low-Power Current Consumption for Deep Sleep:
  - WDT: 270 nA @ 3.3V typical
  - RTCC: 400 nA @ 32 kHz, 3.3V typical
  - Deep Sleep current, 40 na, 3.3V typical

Peripheral Features:

- LCD Display Controller:
  - Up to 60 segments by 8 commons
  - Internal charge pump and low-power, internal resistor biasing
  - Operation in Sleep mode
- Up to Five External Interrupt Sources
- Peripheral Pin Select (PPS): Allows Independent I/O Mapping of Many Peripherals
- Five 16-Bit Timers/Counters with Prescaler:
  - Can be paired as 32-bit timers/counters
- Six-Channel DMA supports All Peripheral modules:
  - Minimizes CPU overhead and increases data throughput

Peripheral Features (Continued):

- Seven Input Capture modules, each with a Dedicated 16-Bit Timer
- Seven Output Compare/PWM modules, each with a Dedicated 16-Bit Timer
- Enhanced Parallel Master/Slave Port (EPMP/EPSP)
- Hardware Real-Time Clock/Calendar (RTCC):
  - Runs in Deep Sleep and VBAT modes
- Two 3-Wire/4-Wire SPI modules (support 4 Frame modes) with 8-Level FIFO Buffer
- Two I²C™ modules Support Multi-Master/Slave mode and 7-Bit/10-Bit Addressing
- Four UART modules:
  - Support RS-485, RS-232 and LIN/J2602
  - On-chip hardware encoder/decoder for IrDA®
  - Auto-wake-up on Auto-Baud Detect
  - 4-level deep FIFO buffer
- Programmable 32-Bit Cyclic Redundancy Check (CRC) Generator
- Digital Signal Modulator Provides On-Chip FSK and PSK Modulation for a Digital Signal Stream
- Configurable Open-Drain Outputs on Digital I/O Pins
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins

Analog Features:

- 10/12-Bit, 24-Channel Analog-to-Digital (A/D) Converter:
  - Conversion rate of 500 ksps (10-bit), 200 ksps (12-bit)
  - Conversion available during Sleep and Idle
- Three Rail-to-Rail Enhanced Analog Comparators with Programmable Input/Output Configuration
- On-Chip Programmable Voltage Reference
- Charge Time Measurement Unit (CTMU):
  - Used for capacitive touch sensing, up to 24 channels
  - Time measurement down to 1 ns resolution
  - CTMU temperature sensing

Device	Pins	Memory		Remappable Peripherals					I²C™	10/12-Bit ADC (ch)	Comparators	CTMU (ch)	EPMP/EPSP	LCD (pixels)	JTAG	Deep Sleep w/VBAT
		Flash Program (bytes)	Data SRAM (bytes)	16-Bit Timers	Capture Input	Compare/PWM Output	UART w/IrDA®	SPI								
PIC24FJ128GA310	100	128K	8K	5	7	7	4	2	2	24	3	24	Y	480	Y	Y
PIC24FJ128GA308	80	128K	8K	5	7	7	4	2	2	16	3	16	Y	368	Y	Y
PIC24FJ128GA306	64	128K	8K	5	7	7	4	2	2	16	3	16	Y	240	Y	Y
PIC24FJ64GA310	100	64K	8K	5	7	7	4	2	2	24	3	24	Y	480	Y	Y
PIC24FJ64GA308	80	64K	8K	5	7	7	4	2	2	16	3	16	Y	368	Y	Y
PIC24FJ64GA306	64	64K	8K	5	7	7	4	2	2	16	3	16	Y	240	Y	Y

High-Performance CPU:

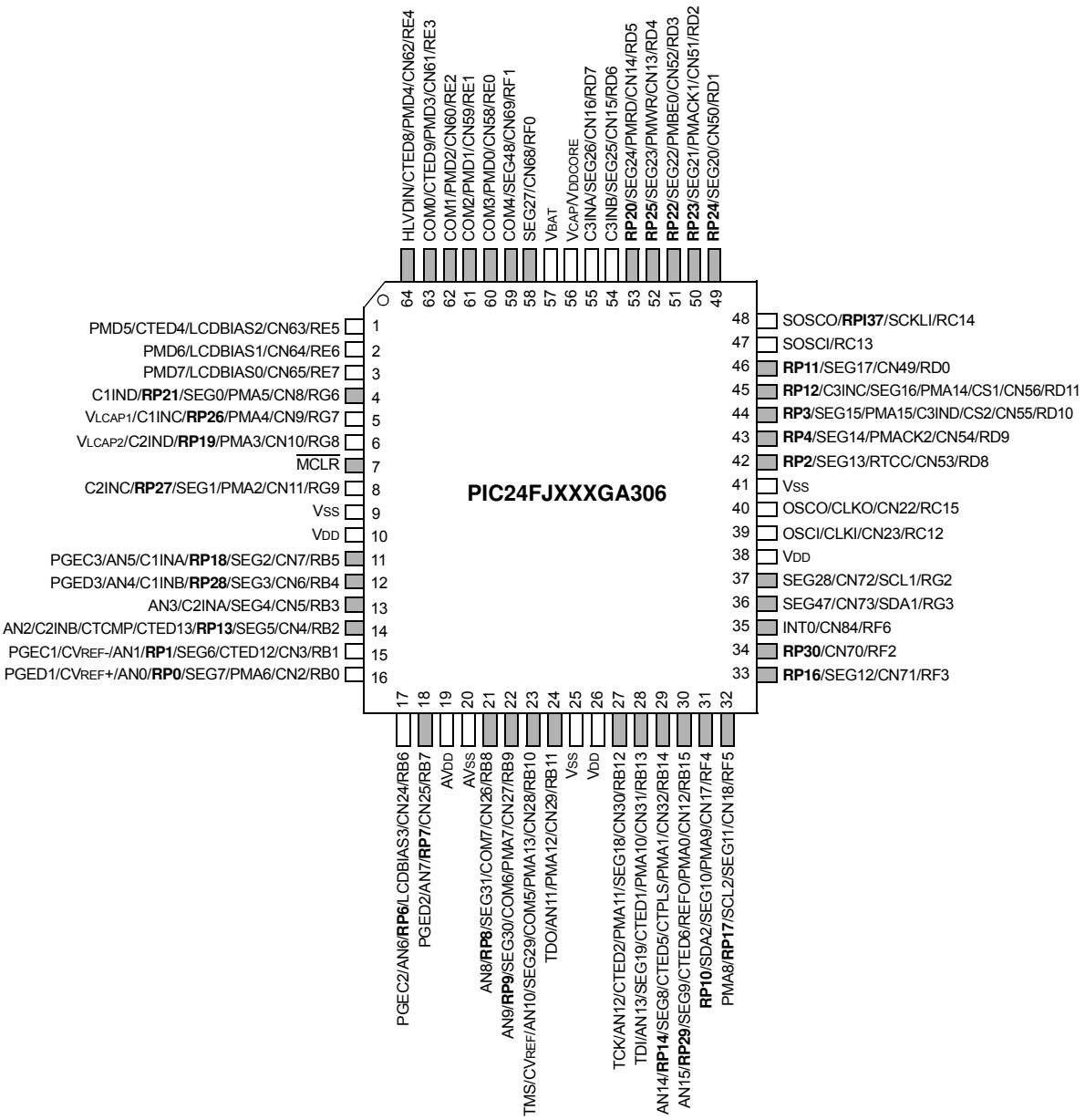
- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Internal Oscillator:
  - 4x PLL option
  - Multiple clock divide options
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory

Special Microcontroller Features:

- Operating Voltage Range of 2.0V to 3.6V
- Two On-Chip Voltage Regulators (1.8V and 1.2V) for Regular and Extreme Low-Power Operation
- 20,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- Flash Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Programmable Reference Clock Output
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via 2 Pins
- JTAG Boundary Scan Support
- Fail-Safe Clock Monitor Operation:
  - Detects clock failure and switches to on-chip, low-power RC oscillator
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Operation Below V_{BOR}
- High/Low-Voltage Detect (HLVD)
- Flexible Watchdog Timer (WDT) with its Own RC Oscillator for Reliable Operation
- Standard and Ultra Low-Power Watchdog Timers (ULPW) for Reliable Operation in Standard and Deep Sleep modes

Pin Diagrams

64-Pin TQFP, QFN(1)

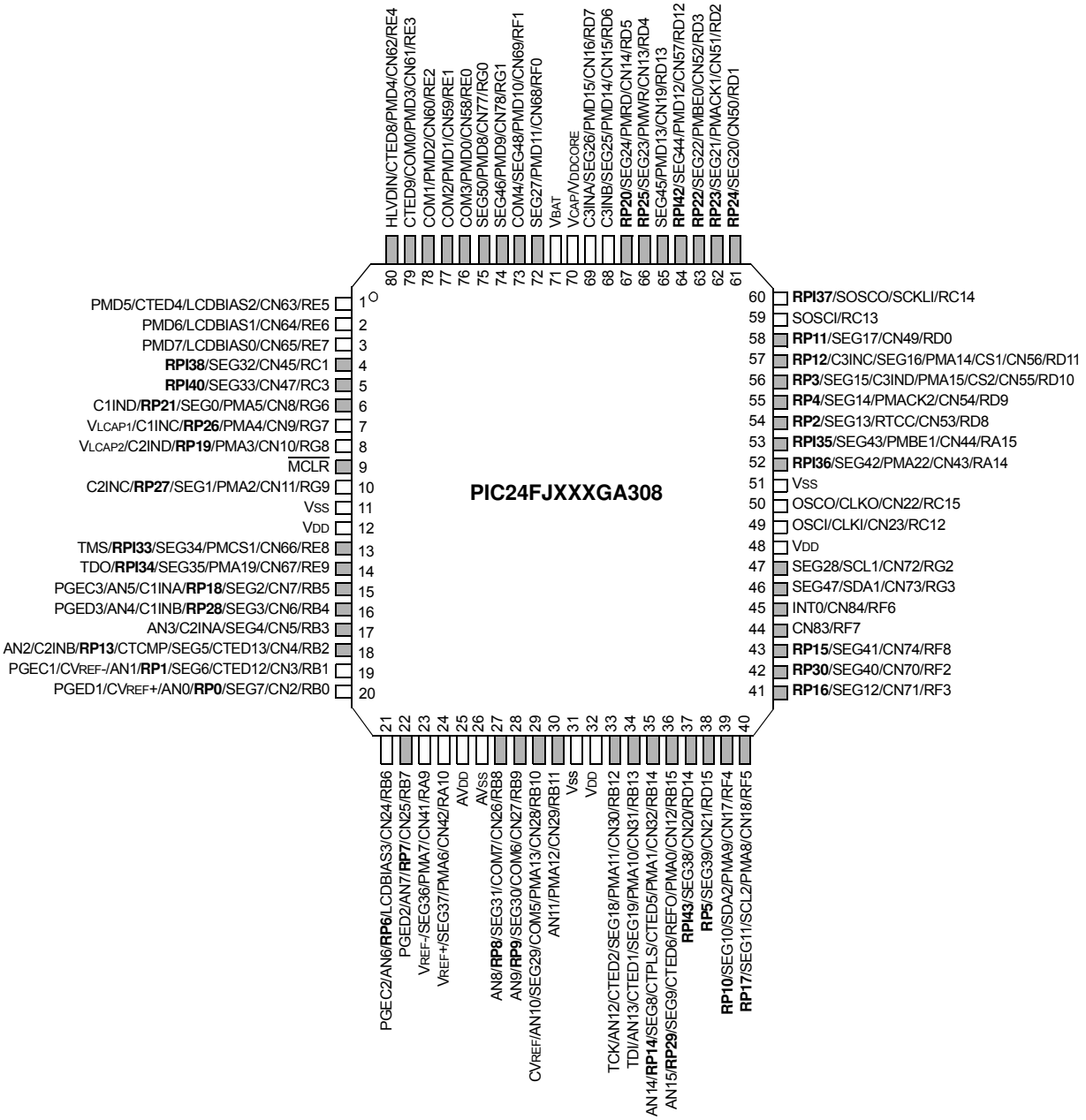


Legend: **RPn** and **RPIn** represent remappable pins for the Peripheral Pin Select feature. Shaded pins indicate pins that are tolerant up to +5.5V.

Note 1: Refer to Table 4-22 for the list of analog ports.

Pin Diagrams (Continued)

80-Pin TQFP(1)

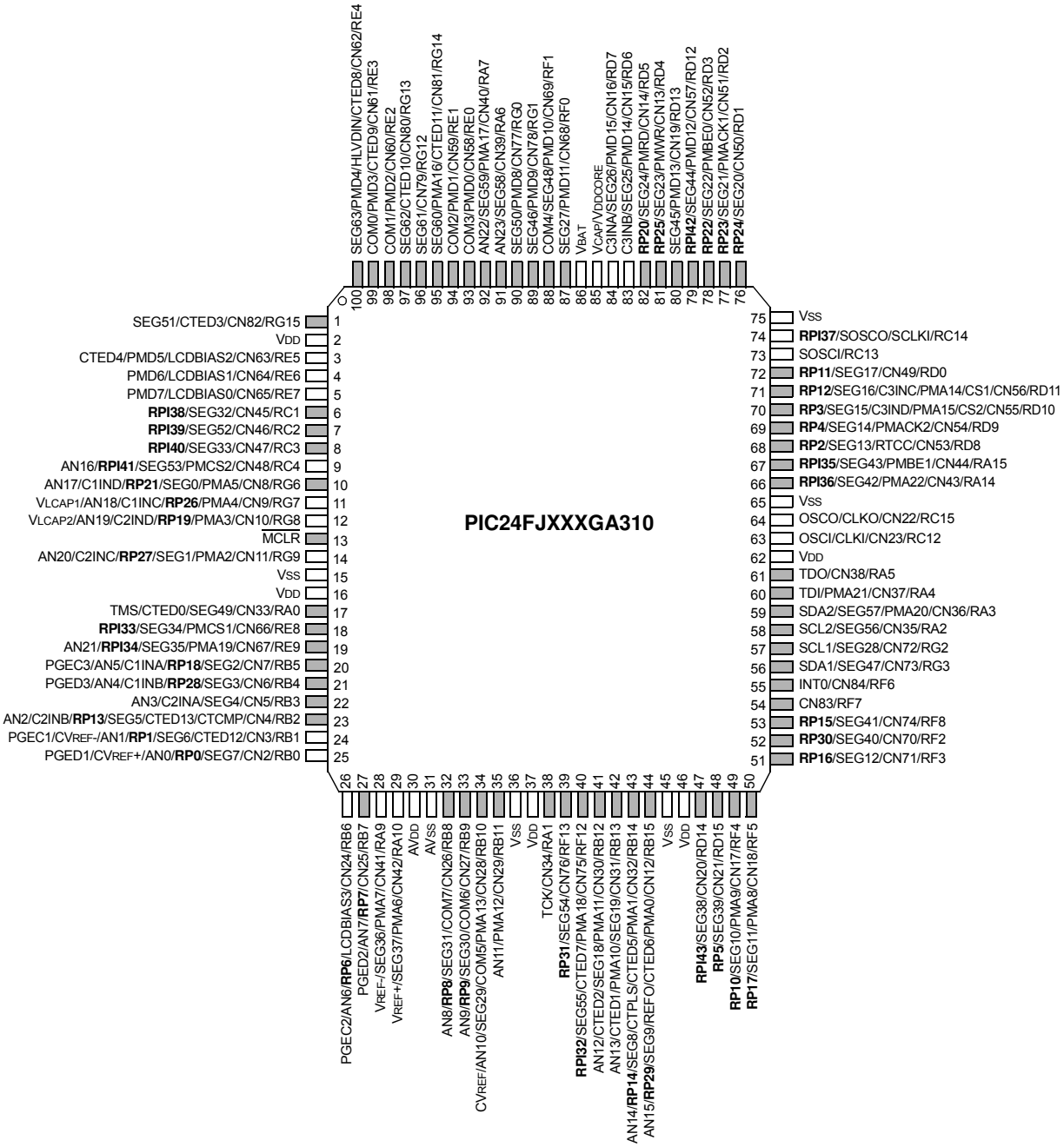


Legend: **RPn** and **RPIn** represent remappable pins for the Peripheral Pin Select feature. Shaded pins indicate pins that are tolerant up to +5.5V.

Note 1: Refer to Table 4-22 for the list of analog ports.

Pin Diagrams (Continued)

100-Pin TQFP(1)



Legend: **RPn** and **RPIn** represent remappable pins for the Peripheral Pin Select feature. Shaded pins indicate pins that are tolerant up to +5.5V.

Note 1: Refer to Table 4-22 for the list of analog ports.

Pin Diagrams (Continued)

121-Pin BGA (Top View)(1,2)

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VBAT	N/C	RD12	RD2	RD1
B	N/C	RG15	RE2	RE1	RA7	RF0	VCAP/ VDDCORE	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	N/C	RD7	RD4	N/C	RC13	RD11
D	RC1	RE7	RE5	N/C	N/C	N/C	RD6	RD13	RD0	N/C	RD10
E	RC4	RC3	RG6	RC2	N/C	RG1	N/C	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	N/C	N/C	VDD	OSCI/ RC12	VSS	OSCO/ RC15
G	RE8	RE9	RA0	N/C	VDD	VSS	VSS	N/C	RA5	RA3	RA4
H	RB5	RB4	N/C	N/C	N/C	VDD	N/C	RF7	RF6	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	N/C	N/C	RF8	RG3
K	RB1	RB0	RA10	RB8	N/C	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Legend: Shaded pins indicate pins that are tolerant up to +5.5V.

Note 1: See Table 1 for complete pinout descriptions.

2: Refer to Table 4-22 for the list of analog ports.

TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 121-PIN DEVICES

Pin	Function	Pin	Function
A1	SEG63/PMD4/HLVDIN/CTED8/CN62/RE4	E1	AN16/**RPI41**/SEG53/PMCS2/CN48/RC4
A2	COM0/PMD3/CTED9/CN61/RE3	E2	**RPI40**/SEG33/CN47/RC3
A3	SEG62/CTED10/CN80/RG13	E3	AN17/C1IND/**RP21**/SEG0/PMA5/CN8/RG6
A4	COM3/PMD0/CN58/RE0	E4	**RPI39**/SEG52/CN46/RC2
A5	SEG50/PMD8/CN77/RG0	E5	N/C
A6	SEG48/COM4/PMD10/CN69/RF1	E6	SEG46/PMD9/CN78/RG1
A7	VBAT	E7	N/C
A8	N/C	E8	**RPI35**/SEG43/PMBE1/CN44/RA15
A9	**RPI42**/SEG44/PMD12/CN57/RD12	E9	**RP2**/SEG13/RTCC/CN53/RD8
A10	**RP23**/SEG21/PMACK1/CN51/RD2	E10	**RP4**/SEG14/PMACK2/CN54/RD9
A11	**RP24**/SEG20/CN50/RD1	E11	**RPI36**/SEG42/PMA22/CN43/RA14
B1	N/C	F1	$\overline{\text{MCLR}}$
B2	SEG51/CTED3/CN82/RG15	F2	VLCAP2/AN19/C2IND/**RP19**/PMA3/CN10/RG8
B3	COM1/PMD2/CN60/RE2	F3	AN20/C2INC/**RP27**/SEG1/PMA2/CN11/RG9
B4	COM2/PMD1/CN59/RE1	F4	VLCAP1/AN18/C1INC/**RP26**/PMA4/CN9/RG7
B5	AN22/SEG59/PMA17/CN40/RA7	F5	VSS
B6	SEG27/PMD11/CN68/RF0	F6	N/C
B7	VCAP	F7	N/C
B8	**RP20**/SEG24/PMRD/CN14/RD5	F8	VDD
B9	**RP22**/SEG22/PMBE0/CN52/RD3	F9	OSCI/CLKI/CN23/RC12
B10	VSS	F10	VSS
B11	RPI37/SOSCO/SCLKI/RC14	F11	OSCO/CLKO/CN22/RC15
C1	PMD6/LCDBIAS1/CN64/RE6	G1	**RPI33**/SEG34/PMCS1/CN66/RE8
C2	VDD	G2	AN21/**RPI34**/SEG35/PMPA19/CN67/RE9
C3	SEG61/CN79/RG12	G3	TMS/SEG49/CTED0/CN33/RA0
C4	SEG60/PMA16/CTED11/CN81/RG14	G4	N/C
C5	AN23/SEG58/CN39/RA6	G5	VDD
C6	N/C	G6	VSS
C7	C3INA/SEG26/PMD15/CN16/RD7	G7	VSS
C8	**RP25**/SEG23/PMWR/CN13/RD4	G8	N/C
C9	N/C	G9	TDO/CN38/RA5
C10	SOSCI/RC13	G10	SDA2/SEG57/PMA20/CN36/RA3
C11	**RP12**/SEG16/C3INC/PMA14/CS1/CN56/RD11	G11	TDI/PMA21/CN37/RA4
D1	**RPI38**/SEG32/CN45/RC1	H1	PGEC3/AN5/C1INA/**RP18**/SEG2/CN7/RB5
D2	PMD7/LCDBIAS0/CN65/RE7	H2	PGED3/AN4/C1INB/**RP28**/SEG3/CN6/RB4
D3	PMD5/CTED4/LCDBIAS2/CN63/RE5	H3	N/C
D4	N/C	H4	N/C
D5	N/C	H5	N/C
D6	N/C	H6	VDD
D7	C3INB/SEG25/PMD14/CN15/RD6	H7	N/C
D8	SEG45/PMD13/CN19/RD13	H8	CN83/RF7
D9	**RP11**/SEG17/CN49/RD0	H9	INT0/CN84/RF6
D10	N/C	H10	SCL1/SEG28/CN72/RG2
D11	**RP3**/SEG15/C3IND/PMA15/CS2/CN55/RD10	H11	SCL2/SEG56/CN35/RA2

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 121-PIN DEVICES (CONTINUED)

Pin	Function	Pin	Function
J1	AN3/C2INA/SEG4/CN5/RB3	K7	AN14/**RP14**/SEG8/CTPLS/CTED5/PMA1/CN32/RB14
J2	AN2/C2INB/**RP13**/SEG5/CTCMP/CTED13/CN4/RB2	K8	VDD
J3	PGED2/AN7/**RP7**/CN25/RB7	K9	**RP5**/SEG39/CN21/RD15
J4	AVDD	K10	**RP16**/SEG12/CN71/RF3
J5	AN11/PMA12/CN29/RB11	K11	**RP30**/SEG40/CN70/RF2
J6	TCK/CN34/RA1	L1	PGEC2/AN6/**RP6**/LCDBIAS3/CN24/RB6
J7	AN12/SEG18/CTED2/PMA11/CN30/RB12	L2	VREF-/SEG36/PMA7/CN41/RA9
J8	N/C	L3	AVSS
J9	N/C	L4	AN9/**RP9**/COM6/SEG30/CN27/RB9
J10	**RP15**/SEG41/CN74/RF8	L5	CVREF/AN10/COM5/SEG29/PMA13/CN28/RB10
J11	SDA1/SEG47/CN73/RG3	L6	**RP31**/SEG54/CN76/RF13
K1	PGEC1/CVREF-/AN1/RP1/SEG6/CTED12/CN3/RB1	L7	AN13/SEG19/CTED1/PMA10/CN31/RB13
K2	PGD1/CVREF+/AN0/**RP0**/SEG7/CN2/RB0	L8	AN15/**RP29**/SEG9/CTED6/REFO/PMA0/CN12/RB15
K3	VREF+/SEG37/PMA6/CN42/RA10	L9	**RPI43**/SEG38/CN20/RD14
K4	AN8/**RP8**/COM7/SEG31/CN26/RB8	L10	**RP10**/SEG10/PMA9/CN17/RF4
K5	N/C	L11	**RP17**/SEG11/PMA8/CN18/RF5
K6	**RPI32**/SEG55/CTED7/PMA18/CN75/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GA306
- PIC24FJ64GA308
- PIC24FJ64GA310
- PIC24FJ128GA306
- PIC24FJ128GA308
- PIC24FJ128GA310

The PIC24FJ128GA310 family adds many new features to Microchip's 16-bit microcontrollers, including new ultra low-power features, Direct Memory Access (DMA) for peripherals, and a built-in LCD Controller and Driver. Together, these provide a wide range of powerful features in one economical and power-saving package.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 XLP POWER-SAVING TECHNOLOGY

The PIC24FJ128GA310 family of devices introduces a greatly expanded range of power-saving operating modes for the ultimate in power conservation. The new modes include:

- Retention Sleep with essential circuits being powered from a separate low-voltage regulator
- Deep Sleep without RTCC for the lowest possible power consumption under software control
- V_{BAT} mode (with or without RTCC) to continue limited operation from a backup battery when V_{DD} is removed

Many of these new low-power modes also support the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from these new features, PIC24FJ128GA310 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of Idle and the many Sleep modes.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ128GA310 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- Two External Clock modes
- A Phase Lock Loop (PLL) frequency multiplier, which allows clock speeds of up to 32 MHz
- A Fast Internal Oscillator (FRC) (nominal 8 MHz output) with multiple frequency divider options
- A separate Low-Power Internal RC Oscillator (LPRC) (31 kHz nominal) for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger, or even in jumping from 64-pin to 100-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

1.2 DMA Controller

PIC24FJ128GA310 family devices also introduce a new Direct Memory Access Controller (DMA) to the PIC24F architecture. This module acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Six independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.3 LCD Controller

With the PIC24FJ128GA310 family of devices, Microchip introduces its versatile Liquid Crystal Display (LCD) controller and driver to the PIC24F family. The on-chip LCD driver includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump, and an integrated internal resistor ladder that allows contrast control in software and display operation above device V_{DD}.

1.4 Other Special Features

- **Peripheral Pin Select:** The Peripheral Pin Select (PPS) feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ128GA310 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are two independent I^2C™ modules that support both Master and Slave modes of operation. Devices also have, through the PPS feature, four independent UARTs with built-in IrDA® encoders/decoders and two SPI modules.
- **Analog Features:** All members of the PIC24FJ128GA310 family include the new 12-bit A/D Converter (ADC) module and a triple comparator module. The ADC module incorporates a range of new features that allow the converter to assess and make decisions on incoming data, reducing CPU overhead for routine ADC conversions. The comparator module includes three analog comparators that are configurable for a wide range of operations.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ128GA310 family include the CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits, and address widths up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- **Data Signal Modulator (DSM):** The Data Signal Modulator (DSM) allows the user to mix a digital data stream (the “modulator signal”) with a carrier signal to produce a modulated output.

1.5 Details on Individual Family Members

Devices in the PIC24FJ128GA310 family are available in 64-pin, 80-pin and 100-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in six ways:

1. Flash program memory (64 Kbytes for PIC24FJ64GA3XX devices and 128 Kbytes for PIC24FJ128GA3XX devices).
2. Available I/O pins and ports (53 pins on 6 ports for 64-pin devices, 69 pins on 7 ports for 80-pin devices and 85 pins on 7 ports for 100-pin devices).
3. Available Interrupt-on-Change Notification (ICN) inputs (52 on 64-pin devices, 66 on 80-pin devices and 82 on 100-pin devices).
4. Available remappable pins (29 pins on 64-pin devices, 40 on 80-pin devices and 44 pins on 100-pin devices).
5. Maximum available drivable LCD pixels (272 on 64-pin devices, 368 on 80-pin devices and 480 on 100-pin devices).
6. Analog input channels (16 channels for 64-pin and 80-pin devices, and 24 channels for 100-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

A list of the pin features available on the PIC24FJ128GA310 family devices, sorted by function, is shown in Table 1-4. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GA310 FAMILY: 64-PIN

Features	PIC24FJ64GA306	PIC24FJ128GA306
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	65 (61/4)	
I/O Ports	Ports B, C, D, E, F, G	
Total I/O Pins	53	
Remappable Pins	30 (29 I/Os, 1 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture Channels	7(1)	
Output Compare/PWM Channels	7(1)	
Input Change Notification Interrupt	52	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C™	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12/10-Bit Analog-to-Digital Converter (ADC) Module (input channels)	16	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	240 (30 SEG x 8 COM)	
Resets (and Delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	64-Pin TQFP and QFN	

Note 1: Peripherals are accessible through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ128GA310 FAMILY: 80-PIN

Features	PIC24FJ64GA308	PIC24FJ128GA308
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	65 (61/4)	
I/O Ports	Ports A, B, C, D, E, F, G	
Total I/O Pins	69	
Remappable Pins	40 (31 I/Os, 9 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture Channels	7(1)	
Output Compare/PWM Channels	7(1)	
Input Change Notification Interrupt	66	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C™	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12/10-Bit Analog-to-Digital Converter (ADC) Module (input channels)	16	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	368 (46 SEG x 8 COM)	
Resets (and Delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	80-Pin TQFP and QFN	

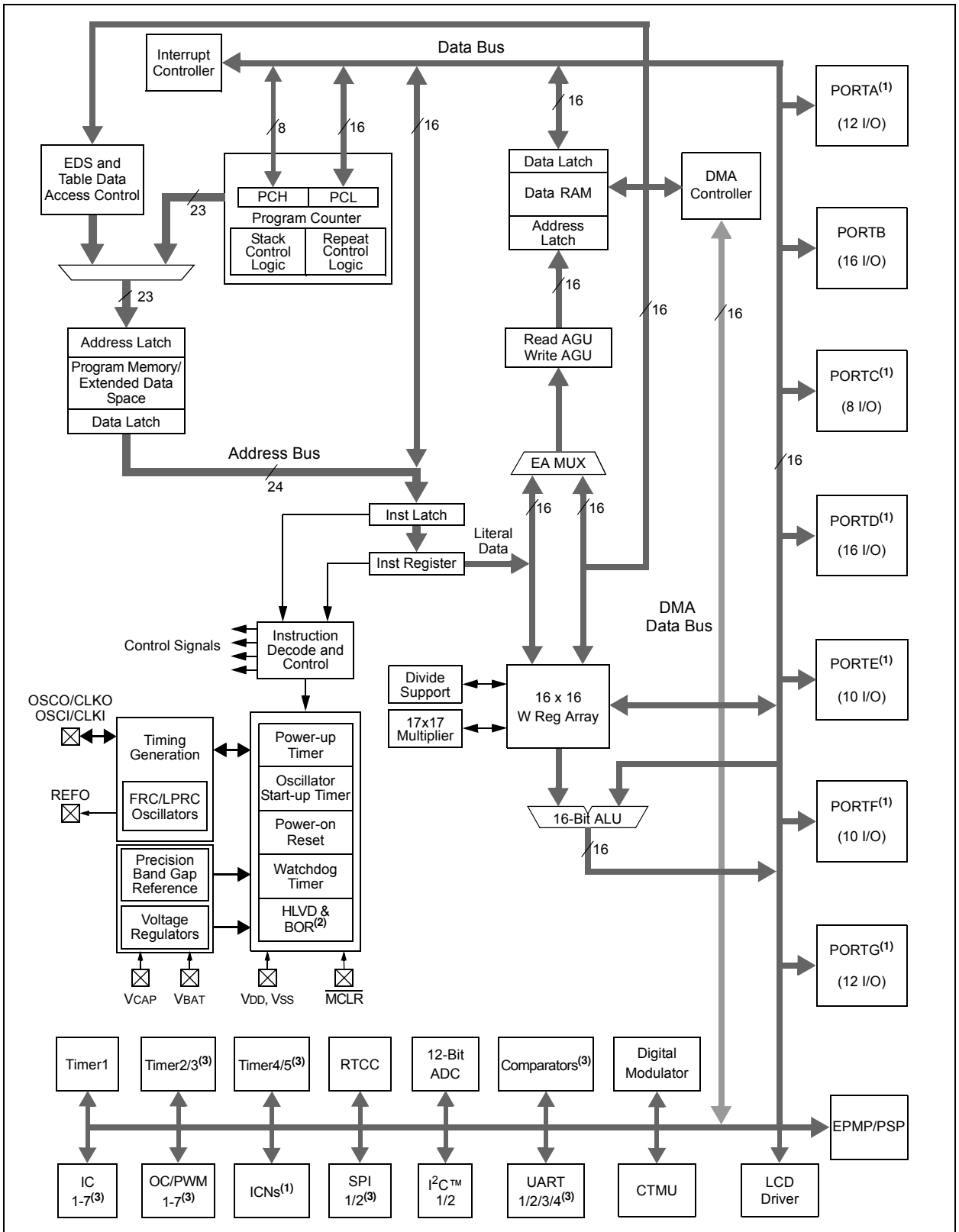
Note 1: Peripherals are accessible through remappable pins.

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ128GA310 FAMILY: 100-PIN DEVICES

Features	PIC24FJ64GA310	PIC24FJ128GA310
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/NMI traps)	66 (62/4)	
I/O Ports	Ports A, B, C, D, E, F, G	
Total I/O Pins	85	
Remappable Pins	44 (32 I/Os, 12 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture Channels	7(1)	
Output Compare/PWM Channels	7(1)	
Input Change Notification Interrupt	82	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C™	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12/10-Bit Analog-to-Digital Converter (ADC) Module (input channels)	24	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	480 (60 SEG x 8 COM)	
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	100-Pin TQFP and 121-Pin BGA	

Note 1: Peripherals are accessible through remappable pins.

FIGURE 1-1: PIC24FJ128GA310 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-4 for specific implementations by pin count.
2: BOR functionality is provided when the on-board voltage regulator is enabled.
3: These peripheral I/Os are only accessible through remappable pins.

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
AN0	16	20	25	K2	I	ANA	ADC Analog Inputs.
AN1	15	19	24	K1	I	ANA	
AN2	14	18	23	J2	I	ANA	
AN3	13	17	22	J1	I	ANA	
AN4	12	16	21	H2	I	ANA	
AN5	11	15	20	H1	I	ANA	
AN6	17	21	26	L1	I	ANA	
AN7	18	22	27	J3	I	ANA	
AN8	21	27	32	K4	I	ANA	
AN9	22	28	33	L4	I	ANA	
AN10	23	29	34	L5	I	ANA	
AN11	24	30	35	J5	I	ANA	
AN12	27	33	41	J7	I	ANA	
AN13	28	34	42	L7	I	ANA	
AN14	29	35	43	K7	I	ANA	
AN15	30	36	44	L8	I	ANA	
AN16	—	—	9	E1	I	ANA	
AN17	—	—	10	E3	I	ANA	
AN18	—	—	11	F4	I	ANA	
AN19	—	—	12	F2	I	ANA	
AN20	—	—	14	F3	I	ANA	
AN21	—	—	19	G2	I	ANA	
AN22	—	—	92	B5	I	ANA	
AN23	—	—	91	C5	I	ANA	
AVDD	19	25	30	J4	P	—	Positive Supply for Analog modules.
AVSS	20	26	31	L3	P	—	Ground Reference for Analog modules.
C1INA	11	15	20	H1	I	ANA	Comparator 1 Input A.
C1INB	12	16	21	H2	I	ANA	Comparator 1 Input B.
C1INC	5	7	11	F4	I	ANA	Comparator 1 Input C.
C1IND	4	6	10	E3	I	ANA	Comparator 1 Input D.
C2INA	13	17	22	J1	I	ANA	Comparator 2 Input A.
C2INB	14	18	23	J2	I	ANA	Comparator 2 Input B.
C2INC	8	10	14	F3	I	ANA	Comparator 2 Input C.
C2IND	6	8	12	F2	I	ANA	Comparator 2 Input D.
C3INA	55	69	84	C7	I	ANA	Comparator 3 Input A.
C3INB	54	68	83	D7	I	ANA	Comparator 3 Input B.
C3INC	45	57	71	C11	I	ANA	Comparator 3 Input C.
C3IND	44	56	70	D11	I	ANA	Comparator 3 Input D.
CLKI	39	49	63	F9	I	ANA	Main Clock Input Connection.
CLKO	40	50	64	F11	O	—	System Clock Output.

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
CN2	16	20	25	K2	I	ST	Interrupt-on-Change Inputs.
CN3	15	19	24	K1	I	ST	
CN4	14	18	23	J2	I	ST	
CN5	13	17	22	J1	I	ST	
CN6	12	16	21	H2	I	ST	
CN7	11	15	20	H1	I	ST	
CN8	4	6	10	E3	I	ST	
CN9	5	7	11	F4	I	ST	
CN10	6	8	12	F2	I	ST	
CN11	8	10	14	F3	I	ST	
CN12	30	36	44	L8	I	ST	
CN13	52	66	81	C8	I	ST	
CN14	53	67	82	B8	I	ST	
CN15	54	68	83	D7	I	ST	
CN16	55	69	84	C7	I	ST	
CN17	31	39	49	L10	I	ST	
CN18	32	40	50	L11	I	ST	
CN19	—	65	80	D8	I	ST	
CN20	—	37	47	L9	I	ST	
CN21	—	38	48	K9	I	ST	
CN22	40	50	64	F11	I	ST	
CN23	39	49	63	F9	I	ST	
CN24	17	21	26	L1	I	ST	
CN25	18	22	27	J3	I	ST	
CN26	21	27	32	K4	I	ST	
CN27	22	28	33	L4	I	ST	
CN28	23	29	34	L5	I	ST	
CN29	24	30	35	J5	I	ST	
CN30	27	33	41	J7	I	ST	
CN31	28	34	42	L7	I	ST	
CN32	29	35	43	K7	I	ST	
CN33	—	—	17	G3	I	ST	
CN34	—	—	38	J6	I	ST	
CN35	—	—	58	H11	I	ST	
CN36	—	—	59	G10	I	ST	
CN37	—	—	60	G11	I	ST	
CN38	—	—	61	G9	I	ST	
CN39	—	—	91	C5	I	ST	
CN40	—	—	92	B5	I	ST	
CN41	—	23	28	L2	I	ST	
CN42	—	24	29	K3	I	ST	
CN43	—	52	66	E11	I	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
CN44	—	53	67	E8	I	ST	Interrupt-on-Change Inputs.
CN45	—	4	6	D1	I	ST	
CN46	—	—	7	E4	I	ST	
CN47	—	5	8	E2	I	ST	
CN48	—	—	9	E1	I	ST	
CN49	46	58	72	D9	I	ST	
CN50	49	61	76	A11	I	ST	
CN51	50	62	77	A10	I	ST	
CN52	51	63	78	B9	I	ST	
CN53	42	54	68	E9	I	ST	
CN54	43	55	69	E10	I	ST	
CN55	44	56	70	D11	I	ST	
CN56	45	57	71	C11	I	ST	
CN57	—	64	79	A9	I	ST	
CN58	60	76	93	A4	I	ST	
CN59	61	77	94	B4	I	ST	
CN60	62	78	98	119	I	ST	
CN61	63	79	99	A2	I	ST	
CN62	64	80	100	A1	I	ST	
CN63	1	1	3	D3	I	ST	
CN64	2	2	4	C1	I	ST	
CN65	3	3	5	D2	I	ST	
CN66	—	13	18	G1	I	ST	
CN67	—	14	19	G2	I	ST	
CN68	58	72	87	B6	I	ST	
CN69	59	73	88	A6	I	ST	
CN70	34	42	52	K11	I	ST	
CN71	33	41	51	K10	I	ST	
CN72	37	47	57	H10	I	ST	
CN73	36	46	56	J11	I	ST	
CN74	—	43	53	J10	I	ST	
CN75	—	—	40	K6	I	ST	
CN76	—	—	39	L6	I	ST	
CN77	—	75	90	A5	I	ST	
CN78	—	74	89	E6	I	ST	
CN79	—	—	96	C3	I	ST	
CN80	—	—	97	A3	I	ST	
CN81	—	—	95	C4	I	ST	
CN82	—	—	1	B2	I	ST	
CN83	—	44	54	H8	I	ST	
CN84	35	45	55	H9	I	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
COM0	63	79	99	A2	O	—	LCD Driver Common Outputs.
COM1	62	78	98	B3	O	—	
COM2	61	77	94	B4	O	—	
COM3	60	76	93	A4	O	—	
COM4	59	73	88	A6	O	—	
COM5	23	29	34	L5	O	—	
COM6	22	28	33	L4	O	—	
COM7	21	27	32	K4	O	—	
CS1	45	57	71	C11	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe (shared with PMA14).
CS2	44	56	70	D11	O	—	Parallel Master Port Chip Select 2 Strobe (shared with PMA15).
CTCMP	14	18	23	J2	I	ANA	CTMU Comparator 2 Input (Pulse mode).
CTED0	—	—	17	G3	I	DIG	CTMU External Edge Inputs.
CTED1	28	34	42	L7	I	DIG	
CTED2	27	33	41	J7	I	DIG	
CTED3	—	—	1	B2	I	DIG	
CTED4	1	1	3	D3	I	DIG	
CTED5	29	35	43	K7	I	DIG	
CTED6	30	36	44	L8	I	DIG	
CTED7	—	—	40	47	I	DIG	
CTED8	64	80	100	A1	I	DIG	
CTED9	63	79	99	A2	I	DIG	
CTED10	—	—	97	A3	I	DIG	
CTED11	—	—	95	C4	I	DIG	
CTED12	15	19	24	K1	I	DIG	
CTED13	14	18	23	J2	I	DIG	
CTPLS	29	35	43	K7	O	—	CTMU Pulse Output.
CV_{REF}	23	29	34	L5	O	—	Comparator Voltage Reference Output.
CV_{REF+}	16	20	25	K2	I	ANA	Comparator/ADC Reference Voltage (high) Input.
CV_{REF-}	15	19	24	K1	I	ANA	Comparator/ADC Reference Voltage (low) Input.
INT0	35	45	55	H9	I	ST	External Interrupt Input 0.
LCDBIAS0	3	3	5	D2	I	ANA	Bias Inputs for LCD Driver Charge Pump.
LCDBIAS1	2	2	4	C1	I	ANA	
LCDBIAS2	1	1	3	D3	I	ANA	
LCDBIAS3	17	21	26	L1	I	ANA	
HLVDIN	64	80	100	A1	I	ANA	High/Low-Voltage Detect Input.
$\overline{MCLR}$	7	9	13	F1	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	39	49	63	F9	I	ANA	Main Oscillator Input Connection.
OSCO	40	50	64	F11	O	—	Main Oscillator Output Connection.

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
PGEC1	15	19	24	K1	I/O	ST	In-Circuit Debugger/Emulator/ICSP™ Programming Clock 1.
PGED1	16	20	25	K2	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 1.
PGEC2	17	21	26	L1	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock 2.
PGED2	18	22	27	J3	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 2.
PGEC3	11	15	20	H1	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock 3.
PGED3	12	16	21	H2	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 3.
PMA0	30	36	44	L8	I/O	ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	35	43	K7	I/O	ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	10	14	F3	O	—	Parallel Master Port Address (bits<22:2>).
PMA3	6	8	12	F2	O	—	
PMA4	5	7	11	F4	O	—	
PMA5	4	6	10	E3	O	—	
PMA6	16	24	29	K3	O	—	
PMA7	22	23	28	L2	O	—	
PMA8	32	40	50	L11	O	—	
PMA9	31	39	49	L10	O	—	
PMA10	28	34	42	L7	O	—	
PMA11	27	33	41	J7	O	—	
PMA12	24	30	35	J5	O	—	
PMA13	23	29	34	L5	O	—	
PMA14	45	57	71	C11	O	—	
PMA15	44	56	70	D11	O	—	
PMA16	—	—	95	C4	O	—	
PMA17	—	—	92	B5	O	—	
PMA18	—	—	40	K6	O	—	
PMA19	—	14	19	G2	O	—	
PMA20	—	—	59	G10	O	—	
PMA21	—	—	60	G11	O	—	
PMA22	—	52	66	E11	O	—	
PMACK1	50	62	77	A10	I	ST/TTL	Parallel Master Port Acknowledge Input 1.
PMACK2	43	55	69	E10	I	ST/TTL	Parallel Master Port Acknowledge Input 2.
PMBE0	51	63	78	B9	O	—	Parallel Master Port Byte Enable 0 Strobe.
PMBE1	—	53	67	E8	O	—	Parallel Master Port Byte Enable 1 Strobe.
PMCS1	—	13	18	G1	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe.
PMCS2	—	—	9	E1	O	—	Parallel Master Port Chip Select 2 Strobe.

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
PMD0	60	76	93	A4	I/O	ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	77	94	B4	I/O	ST/TTL	
PMD2	62	78	98	B3	I/O	ST/TTL	
PMD3	63	79	99	A2	I/O	ST/TTL	
PMD4	64	80	100	A1	I/O	ST/TTL	
PMD5	1	1	3	D3	I/O	ST/TTL	
PMD6	2	2	4	C1	I/O	ST/TTL	
PMD7	3	3	5	D2	I/O	ST/TTL	
PMD8	—	75	90	A5	I/O	ST/TTL	
PMD9	—	74	89	E6	I/O	ST/TTL	
PMD10	—	73	88	A6	I/O	ST/TTL	
PMD11	—	72	87	B6	I/O	ST/TTL	
PMD12	—	64	79	A9	I/O	ST/TTL	
PMD13	—	65	80	D8	I/O	ST/TTL	
PMD14	—	68	83	D7	I/O	ST/TTL	
PMD15	—	69	84	C7	I/O	ST/TTL	
PMRD	53	67	82	B8	O	—	Parallel Master Port Read Strobe.
PMWR	52	66	81	C8	O	—	Parallel Master Port Write Strobe.
RA0	—	—	17	G3	I/O	ST	PORTA Digital I/O.
RA1	—	—	38	J6	I/O	ST	
RA2	—	—	58	H11	I/O	ST	
RA3	—	—	59	G10	I/O	ST	
RA4	—	—	60	G11	I/O	ST	
RA5	—	—	61	G9	I/O	ST	
RA6	—	—	91	C5	I/O	ST	
RA7	—	—	92	B5	I/O	ST	
RA9	—	23	28	L2	I/O	ST	
RA10	—	24	29	K3	I/O	ST	
RA14	—	52	66	E11	I/O	ST	
RA15	—	53	67	E8	I/O	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
RB0	16	20	25	K2	I/O	ST	PORTB Digital I/O.
RB1	15	19	24	K1	I/O	ST	
RB2	14	18	23	J2	I/O	ST	
RB3	13	17	22	J1	I/O	ST	
RB4	12	16	21	H2	I/O	ST	
RB5	11	15	20	H1	I/O	ST	
RB6	17	21	26	L1	I/O	ST	
RB7	18	22	27	J3	I/O	ST	
RB8	21	27	32	K4	I/O	ST	
RB9	22	28	33	L4	I/O	ST	
RB10	23	29	34	L5	I/O	ST	
RB11	24	30	35	J5	I/O	ST	
RB12	27	33	41	J7	I/O	ST	
RB13	28	34	42	L7	I/O	ST	
RB14	29	35	43	K7	I/O	ST	
RB15	30	36	44	L8	I/O	ST	
RC1	—	4	6	D1	I/O	ST	PORTC Digital I/O.
RC2	—	—	7	E4	I/O	ST	
RC3	—	5	8	E2	I/O	ST	
RC4	—	—	9	E1	I/O	ST	
RC12	39	49	63	F9	I/O	ST	
RC13	47	59	73	C10	I	ST	
RC14	48	60	74	B11	I	ST	
RC15	40	50	64	F11	I/O	ST	
RD0	46	58	72	D9	I/O	ST	PORTD Digital I/O.
RD1	49	61	76	A11	I/O	ST	
RD2	50	62	77	A10	I/O	ST	
RD3	51	63	78	B9	I/O	ST	
RD4	52	66	81	C8	I/O	ST	
RD5	53	67	82	B8	I/O	ST	
RD6	54	68	83	D7	I/O	ST	
RD7	55	69	84	C7	I/O	ST	
RD8	42	54	68	E9	I/O	ST	
RD9	43	55	69	E10	I/O	ST	
RD10	44	56	70	D11	I/O	ST	
RD11	45	57	71	C11	I/O	ST	
RD12	—	64	79	A9	I/O	ST	
RD13	—	65	80	D8	I/O	ST	
RD14	—	37	47	L9	I/O	ST	
RD15	—	38	48	K9	I/O	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
RE0	60	76	93	A4	I/O	ST	PORTE Digital I/O.
RE1	61	77	94	B4	I/O	ST	
RE2	62	78	98	B3	I/O	ST	
RE3	63	79	99	A2	I/O	ST	
RE4	64	80	100	A1	I/O	ST	
RE5	1	1	3	D3	I/O	ST	
RE6	2	2	4	C1	I/O	ST	
RE7	3	3	5	D2	I/O	ST	
RE8	—	13	18	G1	I/O	ST	
RE9	—	14	19	G2	I/O	ST	
REFO	30	36	44	L8	O	—	Reference Clock Output.
RF0	58	72	87	B6	I/O	ST	PORTF Digital I/O.
RF1	59	73	88	A6	I/O	ST	
RF2	34	42	52	K11	I/O	ST	
RF3	33	41	51	K10	I/O	ST	
RF4	31	39	49	L10	I/O	ST	
RF5	32	40	50	L11	I/O	ST	
RF6	35	45	55	H9	I/O	ST	
RF7	—	44	54	H8	I/O	ST	
RF8	—	43	53	J10	I/O	ST	
RF12	—	—	40	K6	I/O	ST	
RF13	—	—	39	L6	I/O	ST	
RG0	—	75	90	A5	I/O	ST	PORTG Digital I/O.
RG1	—	74	89	E6	I/O	ST	
RG2	37	47	57	H10	I/O	ST	
RG3	36	46	56	J11	I/O	ST	
RG6	4	6	10	E3	I/O	ST	
RG7	5	7	11	F4	I/O	ST	
RG8	6	8	12	F2	I/O	ST	
RG9	8	10	14	F3	I/O	ST	
RG12	—	—	96	C3	I/O	ST	
RG13	—	—	97	A3	I/O	ST	
RG14	—	—	95	C4	I/O	ST	
RG15	—	—	1	B2	I/O	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
RP0	16	20	25	K2	I/O	ST	Remappable Peripheral (input or output).
RP1	15	19	24	K1	I/O	ST	
RP2	42	54	68	E9	I/O	ST	
RP3	44	56	70	D11	I/O	ST	
RP4	43	55	69	E10	I/O	ST	
RP5	—	38	48	K9	I/O	ST	
RP6	17	21	26	L1	I/O	ST	
RP7	18	22	27	J3	I/O	ST	
RP8	21	27	32	K4	I/O	ST	
RP9	22	28	33	L4	I/O	ST	
RP10	31	39	49	L10	I/O	ST	
RP11	46	58	72	D9	I/O	ST	
RP12	45	57	71	C11	I/O	ST	
RP13	14	18	23	J2	I/O	ST	
RP14	29	35	43	K7	I/O	ST	
RP15	—	43	53	J10	I/O	ST	
RP16	33	41	51	K10	I/O	ST	
RP17	32	40	50	L11	I/O	ST	
RP18	11	15	20	H1	I/O	ST	
RP19	6	8	12	F2	I/O	ST	
RP20	53	67	82	B8	I/O	ST	
RP21	4	6	10	E3	I/O	ST	
RP22	51	63	78	B9	I/O	ST	
RP23	50	62	77	A10	I/O	ST	
RP24	49	61	76	A11	I/O	ST	
RP25	52	66	81	C8	I/O	ST	
RP26	5	7	11	F4	I/O	ST	
RP27	8	10	14	F3	I/O	ST	
RP28	12	16	21	H2	I/O	ST	
RP29	30	36	44	L8	I/O	ST	
RP30	34	42	52	K11	I/O	ST	
RP31	—	—	39	L6	I/O	ST	
RPI32	—	—	40	K6	I	ST	Remappable Peripheral (input only).
RPI33	—	13	18	G1	I	ST	
RPI34	—	14	19	G2	I	ST	
RPI35	—	53	67	E8	I	ST	
RPI36	—	52	66	E11	I	ST	
RPI37	48	60	74	B11	I	ST	
RPI38	—	4	6	D1	I	ST	
RPI39	—	—	7	E4	I	ST	
RPI40	—	5	8	E2	I	ST	
RPI41	—	—	9	E1	I	ST	
RPI42	—	64	79	A9	I	ST	
RPI43	—	37	47	L9	I	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer