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PIC24FJ256GB110 Family Data Sheet

64/80/100-Pin, 16-Bit Flash Microcontrollers with USB On-The-Go (OTG)

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PIC24FJ256GB110 FAMILY

64/80/100-Pin, 16-Bit Flash Microcontrollers with USB On-The-Go (OTG)

Power Management:

- On-Chip 2.5V Voltage Regulator
- Switch between Clock Sources in Real Time
- Idle, Sleep and Doze modes with Fast Wake-up and Two-Speed Start-up
- Run mode: 1 mA/MIPS, 2.0V Typical
- Sleep mode Current Down to 100 nA Typical
- Standby Current with 32 kHz Oscillator: 2.5 μA, 2.0V typical

Universal Serial Bus Features:

- USB v2.0 On-The-Go (OTG) Compliant
- Dual Role Capable – can act as either Host or Peripheral
- Low-Speed (1.5 Mb/s) and Full-Speed (12 Mb/s) USB Operation in Host mode
- Full-Speed USB Operation in Device mode
- High-Precision PLL for USB
- Internal Voltage Boost Assist for USB Bus Voltage Generation
- Interface for Off-Chip Charge Pump for USB Bus Voltage Generation
- Supports up to 32 Endpoints (16 bidirectional):
  - USB Module can use any RAM location on the device as USB endpoint buffers
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- On-Chip Pull-up and Pull-Down Resistors

High-Performance CPU:

- Modified Harvard Architecture
- Up to 16 MIPS Operation at 32 MHz
- 8 MHz Internal Oscillator
- 17-Bit x 17-Bit Single-Cycle Hardware Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture with Flexible Addressing modes
- Linear Program Memory Addressing, Up to 12 Mbytes
- Linear Data Memory Addressing, Up to 64 Kbytes
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory

Analog Features:

- 10-Bit, Up to 16-Channel Analog-to-Digital (A/D) Converter at 500 ksps:
  - Conversions available in Sleep mode
- Three Analog Comparators with Programmable Input/ Output Configuration
- Charge Time Measurement Unit (CTMU)

Device	Pins	Program Memory (Bytes)	SRAM (Bytes)	Remappable Peripherals						I²C™	10-Bit A/D (ch)	Comparators	PMP/PSP	JTAG	CTMU	USBOTG
				Remappable Pins	Timers 16-Bit	Capture Input	Compare/ PWM Output	UART w/IrDA®	SPI							
PIC24FJ64GB106	64	64K	16K	29	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ128GB106	64	128K	16K	29	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ192GB106	64	192K	16K	29	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ256GB106	64	256K	16K	29	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ64GB108	80	64K	16K	40	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ128GB108	80	128K	16K	40	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ192GB108	80	192K	16K	40	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ256GB108	80	256K	16K	40	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ64GB110	100	64K	16K	44	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ128GB110	100	128K	16K	44	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ192GB110	100	192K	16K	44	5	9	9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ256GB110	100	256K	16K	44	5	9	9	4	3	3	16	3	Y	Y	Y	Y

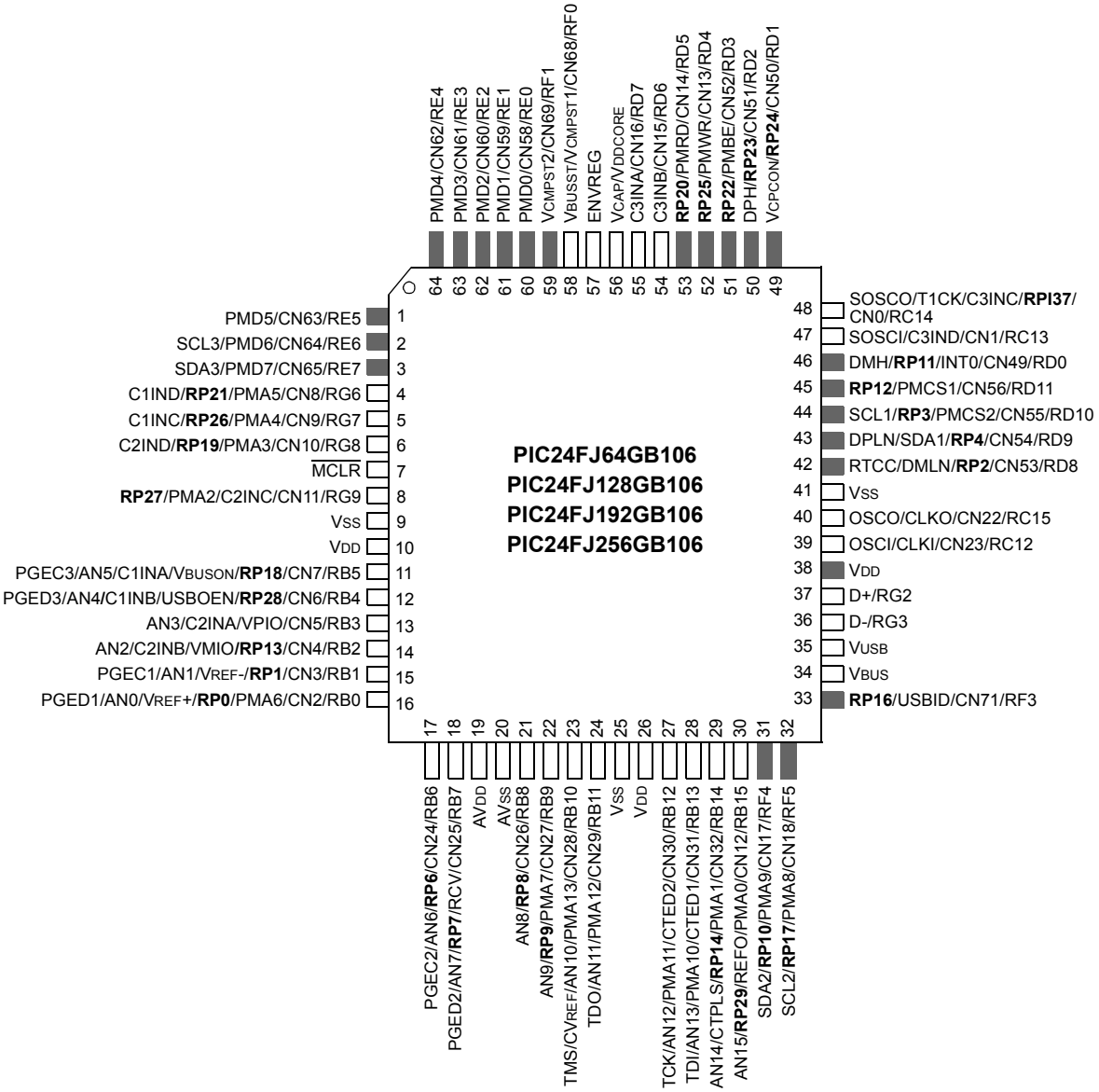
Peripheral Features:

- Peripheral Pin Select (PPS):
  - Allows independent I/O mapping of many peripherals at run time
  - Continuous hardware integrity checking and safety interlocks prevent unintentional configuration changes
  - Up to 44 available pins (100-pin devices)
- Three 3-Wire/4-Wire SPI modules (supports 4 Frame modes) with 8-Level FIFO Buffer
- Three I^2C™ modules support Multi-Master/Slave modes and 7-Bit/10-Bit Addressing
- Four UART modules:
  - Supports RS-485, RS-232, LIN/J2602 protocols and IrDA®
  - On-chip hardware encoder/decoder for IrDA
  - Auto-wake-up and Auto-Baud Detect (ABD)
  - 4-level deep FIFO buffer
- Five 16-Bit Timers/Counters with Programmable Prescaler
- Nine 16-Bit Capture Inputs, each with a Dedicated Time Base
- Nine 16-Bit Compare/PWM Outputs, each with a Dedicated Time Base
- 8-Bit Parallel Master Port (PMP/PSP):
  - Up to 16 address pins
  - Programmable polarity on control lines
- Hardware Real-Time Clock/Calendar (RTCC):
  - Provides clock, calendar and alarm functions
- Programmable Cyclic Redundancy Check (CRC) Generator
- Up to 5 External Interrupt Sources

Special Microcontroller Features:

- Operating Voltage Range of 2.0V to 3.6V
- Self-Reprogrammable under Software Control
- 5.5V Tolerant Input (digital pins only)
- Configurable Open-Drain Outputs on Digital I/O
- High-Current Sink/Source (18 mA/18 mA) on all I/O
- Selectable Power Management modes:
  - Sleep, Idle and Doze modes with fast wake-up
- Fail-Safe Clock Monitor Operation:
  - Detects clock failure and switches to on-chip, Low-Power RC Oscillator
- On-Chip LDO Regulator
- Power-on Reset (POR), Power-up Timer (PWRT), Low-Voltage Detect (LVD) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with On-Chip. Low-Power RC Oscillator for Reliable Operation
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Debug (ICD) via 2 Pins
- JTAG Boundary Scan and Programming Support
- Brown-out Reset (BOR)
- Flash Program Memory:
  - 10,000 erase/write cycle endurance (minimum)
  - 20-year data retention minimum
  - Selectable write protection boundary
  - Write protection option for Flash Configuration Words

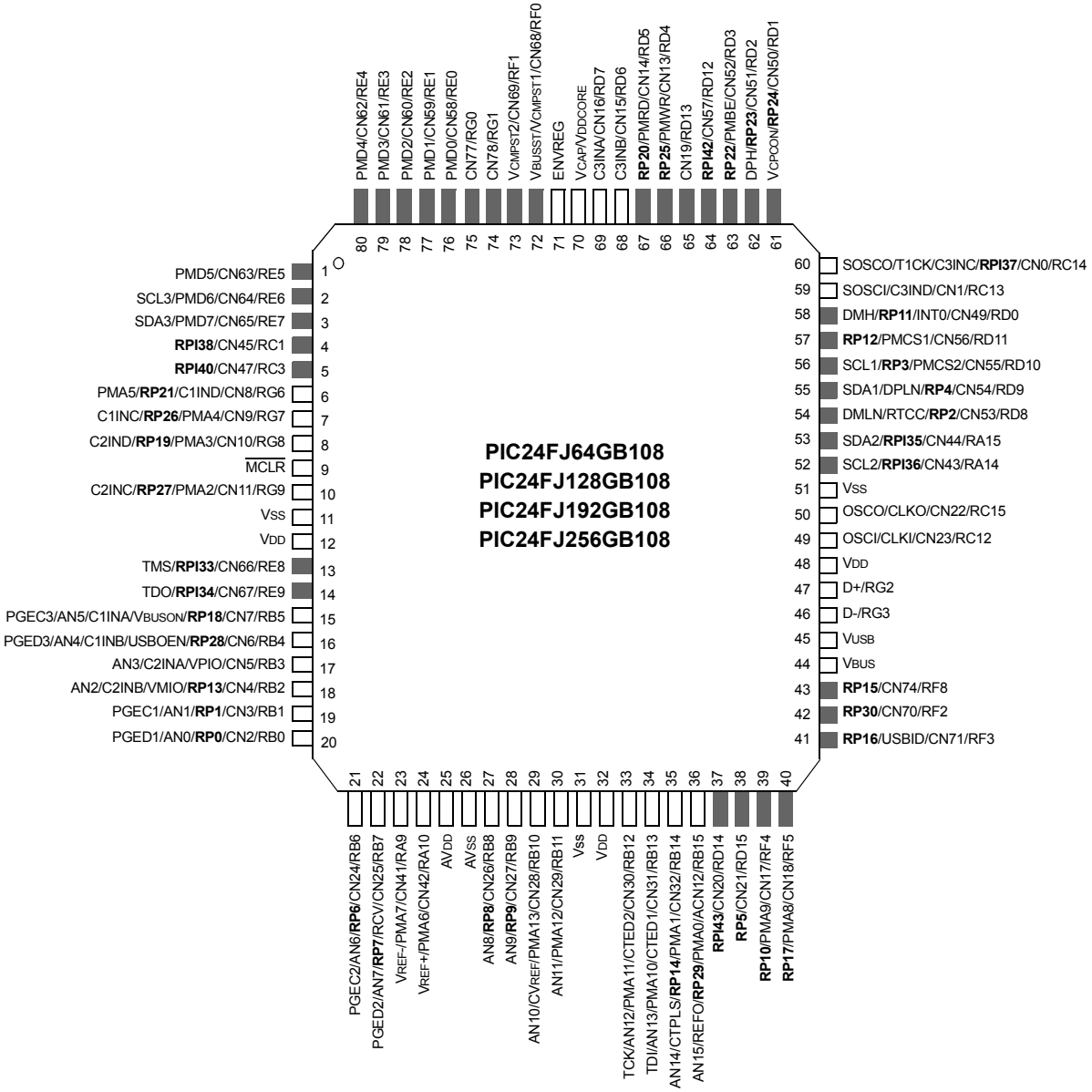
Pin Diagram (64-Pin TQFP and QFN)



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC.
RPn represents remappable pins for the Peripheral Pin Select feature.

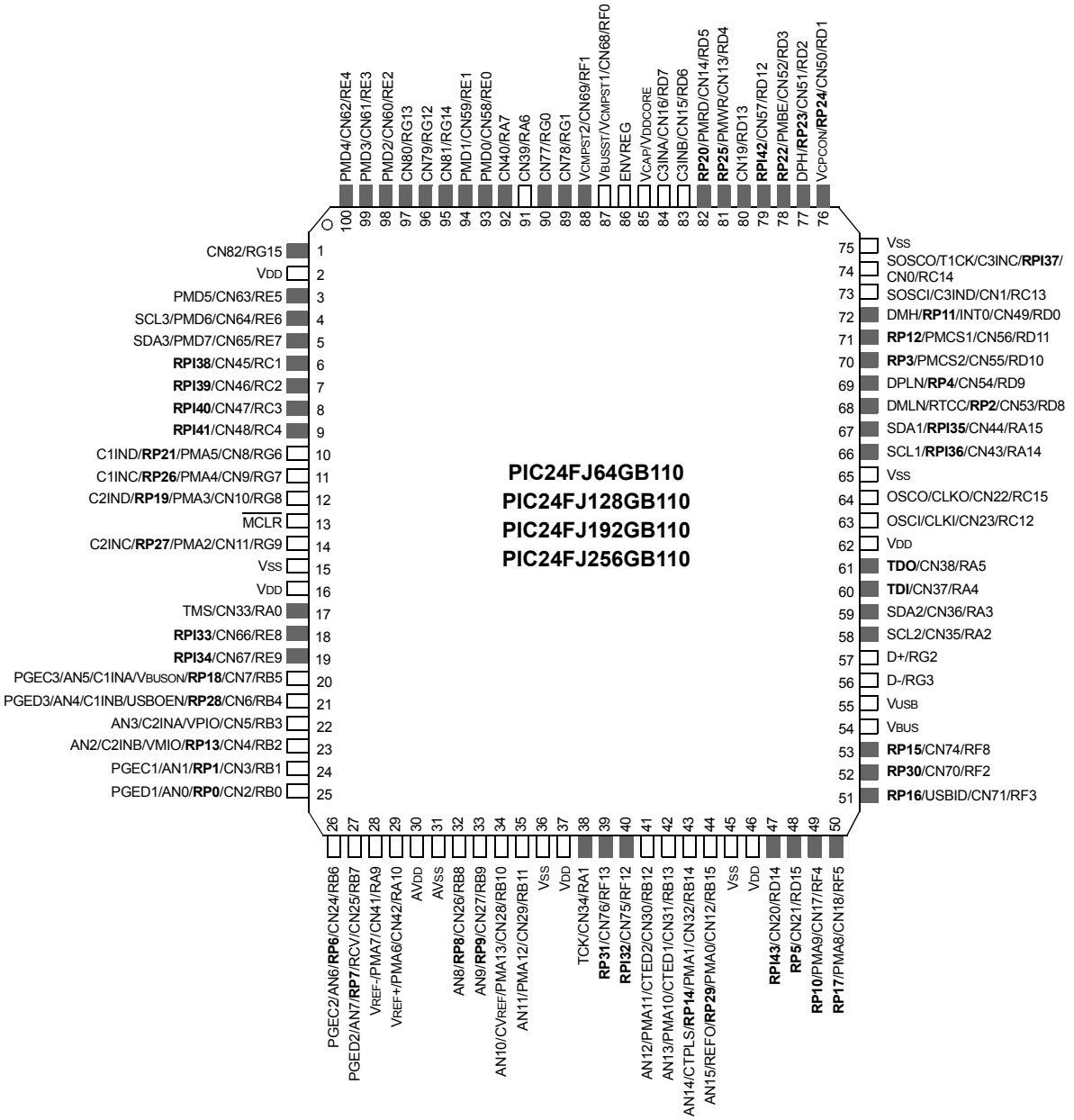
Note 1: For QFN devices, the backplane on the underside of the device must also be connected to VSS.

Pin Diagram (80-Pin TQFP)



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC.
RPn represents remappable pins for the Peripheral Pin Select feature.

Pin Diagram (100-Pin TQFP)



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC.
RPn and **RPIn** represent remappable pins for the Peripheral Pin Select features.

Table of Contents

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GB106
- PIC24FJ128GB106
- PIC24FJ192GB106
- PIC24FJ256GB106
- PIC24FJ64GB108
- PIC24FJ128GB108
- PIC24FJ192GB108
- PIC24FJ256GB108
- PIC24FJ64GB110
- PIC24FJ128GB110
- PIC24FJ192GB110
- PIC24FJ256GB110

This expands on the existing line of Microchip's 16-bit microcontrollers, combining an expanded peripheral feature set and enhanced computational performance with a new connectivity option: USB On-The-Go. The PIC24FJ256GB110 family provides a new platform for high-performance USB applications, which may need more than an 8-bit platform, but don't require the power of a digital signal processor.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® digital signal controllers. The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 64 Kbytes (data)
- A 16-element working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages such as 'C'
- Operational performance up to 16 MIPS

1.1.2 POWER-SAVING TECHNOLOGY

All of the devices in the PIC24FJ256GB110 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **On-the-Fly Clock Switching:** The device clock can be changed under software control to the Timer1 source or the internal, Low-Power RC Oscillator during operation, allowing the user to incorporate power-saving ideas into their software designs.
- **Doze Mode Operation:** When timing-sensitive applications, such as serial communications, require the uninterrupted operation of peripherals, the CPU clock speed can be selectively reduced, allowing incremental power savings without missing a beat.
- **Instruction-Based Power-Saving Modes:** The microcontroller can suspend all operations, or selectively shut down its core while leaving its peripherals active, with a single instruction in software.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ256GB110 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes using crystals or ceramic resonators.
- Two External Clock modes offering the option of a divide-by-2 clock output.
- A Fast Internal Oscillator (FRC) with a nominal 8 MHz output, which can also be divided under software control to provide clock speeds as low as 31 kHz.
- A Phase Lock Loop (PLL) frequency multiplier, available to the external oscillator modes and the FRC Oscillator, which allows clock speeds of up to 32 MHz.
- A separate internal RC Oscillator (LPRC) with a fixed 31 kHz output, which provides a low-power option for timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor. This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger, or even in jumping from 64-pin to 100-pin devices.

The PIC24F family is pin-compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

1.2 USB On-The-Go

With the PIC24FJ256GB110 family of devices, Microchip introduces USB On-The-Go functionality on a single chip to its product line. This new module provides on-chip functionality as a target device compatible with the USB 2.0 standard, as well as limited stand-alone functionality as a USB embedded host. By implementing USB Host Negotiation Protocol (HNP), the module can also dynamically switch between device and host operation, allowing for a much wider range of versatile USB-enabled applications on a microcontroller platform.

In addition to USB host functionality, PIC24FJ256GB110 family devices provide a true single-chip USB solution, including an on-chip transceiver and voltage regulator, and a voltage boost generator for sourcing bus power during host operations.

1.3 Other Special Features

- **Peripheral Pin Select:** The Peripheral Pin Select (PPS) feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ256GB110 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are three independent I^2C modules that support both Master and Slave modes of operation. Devices also have, through the Peripheral Pin Select feature, four independent UARTs with built-in IrDA encoder/decoders and three SPI modules.
- **Analog Features:** All members of the PIC24FJ256GB110 family include a 10-bit A/D Converter module and a triple comparator module. The A/D module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, as well as faster sampling speeds. The comparator module includes three analog comparators that are configurable for a wide range of operations.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ256GB110 family include the brand new CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Parallel Master/Enhanced Parallel Slave Port:** One of the general purpose I/O ports can be reconfigured for enhanced parallel data communications. In this mode, the port can be configured for both master and slave operations, and supports 8-bit and 16-bit data transfers with up to 16 external address lines in Master modes.
- **Real-Time Clock/Calendar:** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.4 Details on Individual Family Members

Devices in the PIC24FJ256GB110 family are available in 64-pin, 80-pin and 100-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in four ways:

1. Flash program memory (64 Kbytes for PIC24FJ64GB1 devices, 128 Kbytes for PIC24FJ128GB1 devices, 192 Kbytes for PIC24FJ192GB1 devices and 256 Kbytes for PIC24FJ256GB1 devices).
2. Available I/O pins and ports (51 pins on 6 ports for 64-pin devices, 65 pins on 7 ports for 80-pin devices and 83 pins on 7 ports for 100-pin devices).
3. Available Interrupt-on-Change Notification (ICN) inputs (49 on 64-pin devices, 63 on 80-pin devices and 81 on 100-pin devices).
4. Available remappable pins (29 pins on 64-pin devices, 40 pins on 80-pin devices and 44 pins on 100-pin devices)

All other features for devices in this family are identical. These are summarized in Table 1-1.

A list of the pin features available on the PIC24FJ256GB110 family devices, sorted by function, is shown in Table 1-4. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ256GB110 FAMILY: 64-PIN DEVICES

Features	64GB106	128GB106	192GB106	256GB106
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	64K	128K	192K	256K
Program Memory (instructions)	22,016	44,032	67,072	87,552
Data Memory (bytes)	16,384			
Interrupt Sources (soft vectors/NMI traps)	66 (62/4)			
I/O Ports	Ports B, C, D, E, F, G			
Total I/O Pins	51			
Remappable Pins	29 (28 I/O, 1 Input only)			
Timers: Total Number (16-bit)	5(1)			
32-Bit (from paired 16-bit timers)	2			
Input Capture Channels	9(1)			
Output Compare/PWM Channels	9(1)			
Input Change Notification Interrupt	49			
Serial Communications: UART	4(1)			
SPI (3-wire/4-wire)	3(1)			
I^2C™	3			
Parallel Communications (PMP/PSP)	Yes			
JTAG Boundary Scan/Programming	Yes			
10-Bit Analog-to-Digital Module (input channels)	16			
Analog Comparators	3			
CTMU Interface	Yes			
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	64-Pin TQFP			

Note 1: Peripherals are accessible through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ256GB110 FAMILY: 80-PIN DEVICES

Features	64GB108	128GB108	192GB108	256GB108
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	64K	128K	192K	256K
Program Memory (instructions)	22,016	44,032	67,072	87,552
Data Memory (bytes)	16,384			
Interrupt Sources (soft vectors/NMI traps)	66 (62/4)			
I/O Ports	Ports A, B, C, D, E, F, G			
Total I/O Pins	65			
Remappable Pins	40 (31 I/O, 9 Input only)			
Timers: Total Number (16-bit)	5(1)			
32-Bit (from paired 16-bit timers)	2			
Input Capture Channels	9(1)			
Output Compare/PWM Channels	9(1)			
Input Change Notification Interrupt	63			
Serial Communications: UART	4(1)			
SPI (3-wire/4-wire)	3(1)			
I^2C™	3			
Parallel Communications (PMP/PSP)	Yes			
JTAG Boundary Scan/Programming	Yes			
10-Bit Analog-to-Digital Module (input channels)	16			
Analog Comparators	3			
CTMU Interface	Yes			
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{\text{MCLR}}$, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	80-Pin TQFP			

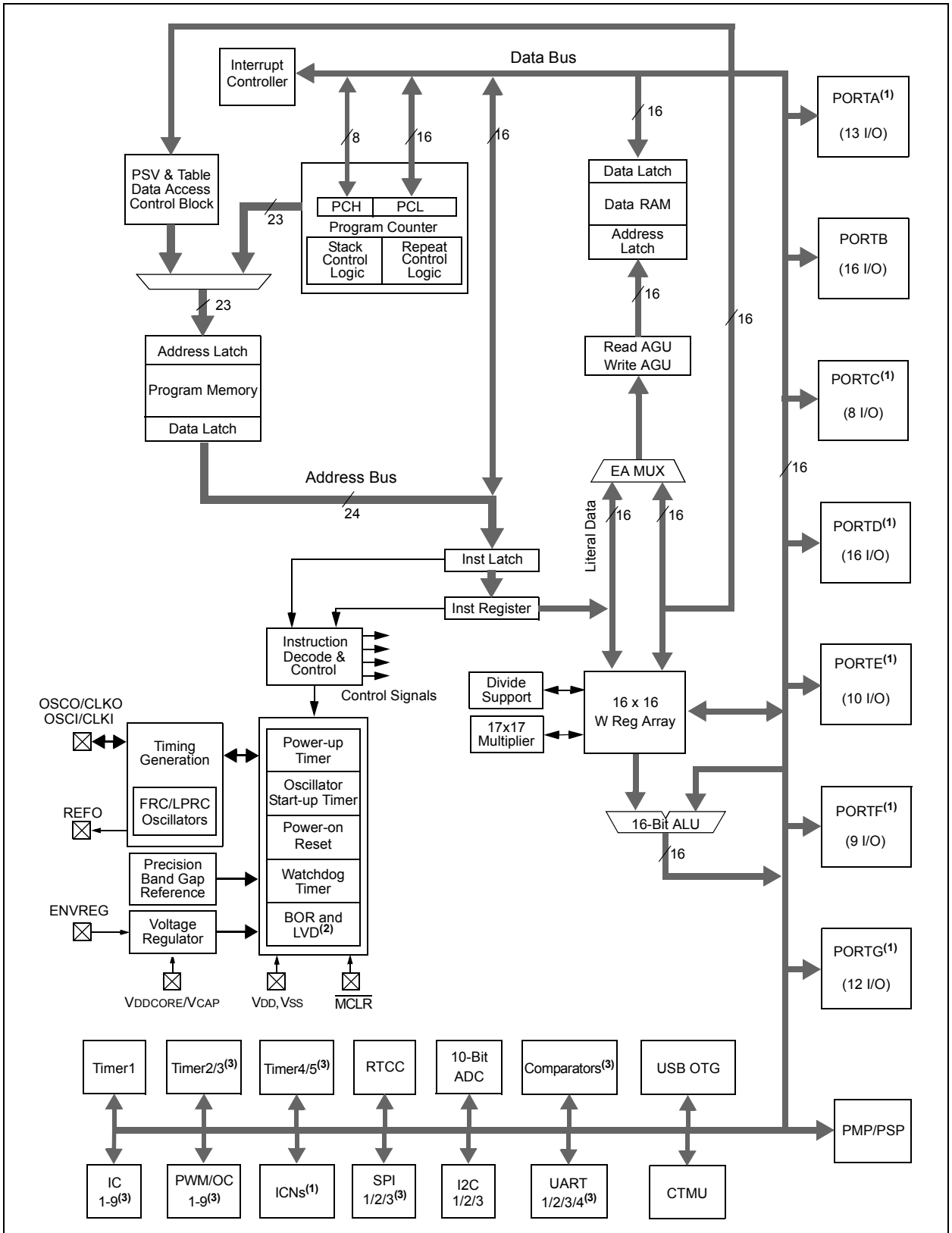
Note 1: Peripherals are accessible through remappable pins.

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ256GB110 FAMILY: 100-PIN DEVICES

Features	64GB110	128GB110	192GB110	256GB110
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	64K	128K	192K	256K
Program Memory (instructions)	22,016	44,032	67,072	87,552
Data Memory (bytes)	16,384			
Interrupt Sources (soft vectors/NMI traps)	66 (62/4)			
I/O Ports	Ports A, B, C, D, E, F, G			
Total I/O Pins	83			
Remappable Pins	44 (32 I/O, 12 Input only)			
Timers: Total Number (16-bit)	5(1)			
32-Bit (from paired 16-bit timers)	2			
Input Capture Channels	9(1)			
Output Compare/PWM Channels	9(1)			
Input Change Notification Interrupt	81			
Serial Communications: UART	4(1)			
SPI (3-wire/4-wire)	3(1)			
I^2C™	3			
Parallel Communications (PMP/PSP)	Yes			
JTAG Boundary Scan/Programming	Yes			
10-Bit Analog-to-Digital Module (input channels)	16			
Analog Comparators	3			
CTMU Interface	Yes			
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	100-Pin TQFP			

Note 1: Peripherals are accessible through remappable pins.

FIGURE 1-1: PIC24FJ256GB110 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-4 for specific implementations by pin count.
2: BOR functionality is provided when the on-board voltage regulator is enabled.
3: These peripheral I/Os are only accessible through remappable pins.

TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
AN0	16	20	25	I	ANA	A/D Analog Inputs.
AN1	15	19	24	I	ANA	
AN2	14	18	23	I	ANA	
AN3	13	17	22	I	ANA	
AN4	12	16	21	I	ANA	
AN5	11	15	20	I	ANA	
AN6	17	21	26	I	ANA	
AN7	18	22	27	I	ANA	
AN8	21	27	32	I	ANA	
AN9	22	28	33	I	ANA	
AN10	23	29	34	I	ANA	
AN11	24	30	35	I	ANA	
AN12	27	33	41	I	ANA	
AN13	28	34	42	I	ANA	
AN14	29	35	43	I	ANA	
AN15	30	36	44	I	ANA	
AVDD	19	25	30	P	—	Positive Supply for Analog modules.
AVSS	20	26	31	P	—	Ground Reference for Analog modules.
C1INA	11	15	20	I	ANA	Comparator 1 Input A.
C1INB	12	16	21	I	ANA	Comparator 1 Input B.
C1INC	5	7	11	I	ANA	Comparator 1 Input C.
C1IND	4	6	10	I	ANA	Comparator 1 Input D.
C2INA	13	17	22	I	ANA	Comparator 2 Input A.
C2INB	14	18	23	I	ANA	Comparator 2 Input B.
C2INC	8	10	14	I	ANA	Comparator 2 Input C.
C2IND	6	8	12	I	ANA	Comparator 2 Input D.
C3INA	55	69	84	I	ANA	Comparator 3 Input A.
C3INB	54	68	83	I	ANA	Comparator 3 Input B.
C3INC	48	60	74	I	ANA	Comparator 3 Input C.
C3IND	47	59	73	I	ANA	Comparator 3 Input D.
CLKI	39	49	63	I	ANA	Main Clock Input Connection.
CLKO	40	50	64	O	—	System Clock Output.

Legend: TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
CN0	48	60	74	I	ST	Interrupt-on-Change Inputs.
CN1	47	59	73	I	ST	
CN2	16	20	25	I	ST	
CN3	15	19	24	I	ST	
CN4	14	18	23	I	ST	
CN5	13	17	22	I	ST	
CN6	12	16	21	I	ST	
CN7	11	15	20	I	ST	
CN8	4	6	10	I	ST	
CN9	5	7	11	I	ST	
CN10	6	8	12	I	ST	
CN11	8	10	14	I	ST	
CN12	30	36	44	I	ST	
CN13	52	66	81	I	ST	
CN14	53	67	82	I	ST	
CN15	54	68	83	I	ST	
CN16	55	69	84	I	ST	
CN17	31	39	49	I	ST	
CN18	32	40	50	I	ST	
CN19	—	65	80	I	ST	
CN20	—	37	47	I	ST	
CN21	—	38	48	I	ST	
CN22	40	50	64	I	ST	
CN23	39	49	63	I	ST	
CN24	17	21	26	I	ST	
CN25	18	22	27	I	ST	
CN26	21	27	32	I	ST	
CN27	22	28	33	I	ST	
CN28	23	29	34	I	ST	
CN29	24	30	35	I	ST	
CN30	27	33	41	I	ST	
CN31	28	34	42	I	ST	
CN32	29	35	43	I	ST	
CN33	—	—	17	I	ST	
CN34	—	—	38	I	ST	
CN35	—	—	58	I	ST	
CN36	—	—	59	I	ST	
CN37	—	—	60	I	ST	
CN38	—	—	61	I	ST	
CN39	—	—	91	I	ST	
CN40	—	—	92	I	ST	
CN41	—	23	28	I	ST	
CN42	—	24	29	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
CN43	—	52	66	I	ST	Interrupt-on-Change Inputs.
CN44	—	53	67	I	ST	
CN45	—	4	6	I	ST	
CN46	—	—	7	I	ST	
CN47	—	5	8	I	ST	
CN48	—	—	9	I	ST	
CN49	46	58	72	I	ST	
CN50	49	61	76	I	ST	
CN51	50	62	77	I	ST	
CN52	51	63	78	I	ST	
CN53	42	54	68	I	ST	
CN54	43	55	69	I	ST	
CN55	44	56	70	I	ST	
CN56	45	57	71	I	ST	
CN57	—	64	79	I	ST	
CN58	60	76	93	I	ST	
CN59	61	77	94	I	ST	
CN60	62	78	98	I	ST	
CN61	63	79	99	I	ST	
CN62	64	80	100	I	ST	
CN63	1	1	3	I	ST	
CN64	2	2	4	I	ST	
CN65	3	3	5	I	ST	
CN66	—	13	18	I	ST	
CN67	—	14	19	I	ST	
CN68	58	72	87	I	ST	
CN69	59	73	88	I	ST	
CN70	—	42	52	I	ST	
CN71	33	41	51	I	ST	
CN74	—	43	53	I	ST	
CN75	—	—	40	I	ST	
CN76	—	—	39	I	ST	
CN77	—	75	90	I	ST	
CN78	—	74	89	I	ST	
CN79	—	—	96	I	ST	
CN80	—	—	97	I	ST	
CN81	—	—	95	I	ST	
CN82	—	—	1	I	ST	
CTED1	28	34	42	I	ANA	CTMU External Edge Input 1.
CTED2	27	33	41	I	ANA	CTMU External Edge Input 2.
CTPLS	29	35	43	O	—	CTMU Pulse Output.
CVREF	23	29	34	O	—	Comparator Voltage Reference Output.

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TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
D+	37	47	57	I/O	—	USB Differential Plus line (internal transceiver).
D-	36	46	56	I/O	—	USB Differential Minus line (internal transceiver).
DMH	46	58	72	O	—	D- External Pull-up Control Output.
DMLN	42	54	68	O	—	D- External Pull-down Control Output.
DPH	50	62	77	O	—	D+ External Pull-up Control Output.
DPLN	43	55	69	O	—	D+ External Pull-down Control Output.
ENVREG	57	71	86	I	ST	Voltage Regulator Enable.
INT0	46	58	72	I	ST	External Interrupt Input.
$\overline{\text{MCLR}}$	7	9	13	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	39	49	63	I	ANA	Main Oscillator Input Connection.
OSCO	40	50	64	O	ANA	Main Oscillator Output Connection.
PGEC1	15	19	24	I/O	ST	In-Circuit Debugger/Emulator/ICSP™ Programming Clock.
PGED1	16	20	25	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data.
PGEC2	17	21	26	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock.
PGED2	18	22	27	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data.
PGEC3	11	15	20	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock.
PGED3	12	16	21	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data.
PMA0	30	36	44	I/O	ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	35	43	I/O	ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	10	14	O	—	Parallel Master Port Address (Demultiplexed Master modes).
PMA3	6	8	12	O	—	
PMA4	5	7	11	O	—	
PMA5	4	6	10	O	—	
PMA6	16	24	29	O	—	
PMA7	22	23	28	O	—	
PMA8	32	40	50	O	—	
PMA9	31	39	49	O	—	
PMA10	28	34	42	O	—	
PMA11	27	33	41	O	—	
PMA12	24	30	35	O	—	
PMA13	23	29	34	O	—	
PMCS1	45	57	71	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe/Address Bit 15.
PMCS2	44	56	70	O	ST	Parallel Master Port Chip Select 2 Strobe/Address Bit 14.
PMBE	51	63	78	O	—	Parallel Master Port Byte Enable Strobe.

Legend: TTL = TTL input buffer
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TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
PMD0	60	76	93	I/O	ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	77	94	I/O	ST/TTL	
PMD2	62	78	98	I/O	ST/TTL	
PMD3	63	79	99	I/O	ST/TTL	
PMD4	64	80	100	I/O	ST/TTL	
PMD5	1	1	3	I/O	ST/TTL	
PMD6	2	2	4	I/O	ST/TTL	
PMD7	3	3	5	I/O	ST/TTL	
PMRD	53	67	82	O	—	Parallel Master Port Read Strobe.
PMWR	52	66	81	O	—	Parallel Master Port Write Strobe.
RA0	—	—	17	I/O	ST	PORTA Digital I/O.
RA1	—	—	38	I/O	ST	
RA2	—	—	58	I/O	ST	
RA3	—	—	59	I/O	ST	
RA4	—	—	60	I/O	ST	
RA5	—	—	61	I/O	ST	
RA6	—	—	91	I/O	ST	
RA7	—	—	92	I/O	ST	
RA9	—	23	28	I/O	ST	
RA10	—	24	29	I/O	ST	
RA14	—	52	66	I/O	ST	
RA15	—	53	67	I/O	ST	
RB0	16	20	25	I/O	ST	PORTB Digital I/O.
RB1	15	19	24	I/O	ST	
RB2	14	18	23	I/O	ST	
RB3	13	17	22	I/O	ST	
RB4	12	16	21	I/O	ST	
RB5	11	15	20	I/O	ST	
RB6	17	21	26	I/O	ST	
RB7	18	22	27	I/O	ST	
RB8	21	27	32	I/O	ST	
RB9	22	28	33	I/O	ST	
RB10	23	29	34	I/O	ST	
RB11	24	30	35	I/O	ST	
RB12	27	33	41	I/O	ST	
RB13	28	34	42	I/O	ST	
RB14	29	35	43	I/O	ST	
RB15	30	36	44	I/O	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
RC1	—	4	6	I/O	ST	PORTC Digital I/O.
RC2	—	—	7	I/O	ST	
RC3	—	5	8	I/O	ST	
RC4	—	—	9	I/O	ST	
RC12	39	49	63	I/O	ST	
RC13	47	59	73	I/O	ST	
RC14	48	60	74	I/O	ST	
RC15	40	50	64	I/O	ST	
RCV	18	22	27	I	ST	USB Receive Input (from external transceiver).
RD0	46	58	72	I/O	ST	PORTD Digital I/O.
RD1	49	61	76	I/O	ST	
RD2	50	62	77	I/O	ST	
RD3	51	63	78	I/O	ST	
RD4	52	66	81	I/O	ST	
RD5	53	67	82	I/O	ST	
RD6	54	68	83	I/O	ST	
RD7	55	69	84	I/O	ST	
RD8	42	54	68	I/O	ST	
RD9	43	55	69	I/O	ST	
RD10	44	56	70	I/O	ST	
RD11	45	57	71	I/O	ST	
RD12	—	64	79	I/O	ST	
RD13	—	65	80	I/O	ST	
RD14	—	37	47	I/O	ST	
RD15	—	38	48	I/O	ST	
RE0	60	76	93	I/O	ST	PORTE Digital I/O.
RE1	61	77	94	I/O	ST	
RE2	62	78	98	I/O	ST	
RE3	63	79	99	I/O	ST	
RE4	64	80	100	I/O	ST	
RE5	1	1	3	I/O	ST	
RE6	2	2	4	I/O	ST	
RE7	3	3	5	I/O	ST	
RE8	—	13	18	I/O	ST	
RE9	—	14	19	I/O	ST	
REFO	30	36	44	O	—	Reference Clock Output.

Legend: TTL = TTL input buffer
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TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
RF0	58	72	87	I/O	ST	PORTF Digital I/O.
RF1	59	73	88	I/O	ST	
RF2	—	42	52	I/O	ST	
RF3	33	41	51	I/O	ST	
RF4	31	39	49	I/O	ST	
RF5	32	40	50	I/O	ST	
RF8	—	43	53	I/O	ST	
RF12	—	—	40	I/O	ST	
RF13	—	—	39	I/O	ST	
RG0	—	75	90	I/O	ST	PORTG Digital I/O.
RG1	—	74	89	I/O	ST	
RG2	37	47	57	I	ST	
RG3	36	46	56	I	ST	
RG6	4	6	10	I/O	ST	
RG7	5	7	11	I/O	ST	
RG8	6	8	12	I/O	ST	
RG9	8	10	14	I/O	ST	
RG12	—	—	96	I/O	ST	
RG13	—	—	97	I/O	ST	
RG14	—	—	95	I/O	ST	
RG15	—	—	1	I/O	ST	
RP0	16	20	25	I/O	ST	Remappable Peripheral (input or output).
RP1	15	19	24	I/O	ST	
RP2	42	54	68	I/O	ST	
RP3	44	56	70	I/O	ST	
RP4	43	55	69	I/O	ST	
RP5	—	38	48	I/O	ST	
RP6	17	21	26	I/O	ST	
RP7	18	22	27	I/O	ST	
RP8	21	27	32	I/O	ST	
RP9	22	28	33	I/O	ST	
RP10	31	39	49	I/O	ST	
RP11	46	58	72	I/O	ST	
RP12	45	57	71	I/O	ST	
RP13	14	18	23	I/O	ST	
RP14	29	35	43	I/O	ST	
RP15	—	43	53	I/O	ST	
RP16	33	41	51	I/O	ST	
RP17	32	40	50	I/O	ST	
RP18	11	15	20	I/O	ST	
RP19	6	8	12	I/O	ST	

Legend: TTL = TTL input buffer
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ST = Schmitt Trigger input buffer
I^2C™ = I^2C/SMBus input buffer

TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
RP20	53	67	82	I/O	ST	Remappable Peripheral (input or output).
RP21	4	6	10	I/O	ST	
RP22	51	63	78	I/O	ST	
RP23	50	62	77	I/O	ST	
RP24	49	61	76	I/O	ST	
RP25	52	66	81	I/O	ST	
RP26	5	7	11	I/O	ST	
RP27	8	10	14	I/O	ST	
RP28	12	16	21	I/O	ST	
RP29	30	36	44	I/O	ST	
RP30	—	42	52	I/O	ST	
RP31	—	—	39	I/O	ST	
RPI32	—	—	40	I	ST	Remappable Peripheral (input only).
RPI33	—	13	18	I	ST	
RPI34	—	14	19	I	ST	
RPI35	—	53	67	I	ST	
RPI36	—	52	66	I	ST	
RPI37	48	60	74	I	ST	
RPI38	—	4	6	I	ST	
RPI39	—	—	7	I	ST	
RPI40	—	5	8	I	ST	
RPI41	—	—	9	I	ST	
RPI42	—	64	79	I	ST	
RPI43	—	37	47	I	ST	
RTCC	42	54	68	O	—	Real-Time Clock Alarm/Seconds Pulse Output.
SCL1	44	56	66	I/O	I^2C	I2C1 Synchronous Serial Clock Input/Output.
SCL2	32	52	58	I/O	I^2C	I2C2 Synchronous Serial Clock Input/Output.
SCL3	2	2	4	I/O	I^2C	I2C3 Synchronous Serial Clock Input/Output.
SDA1	43	55	67	I/O	I^2C	I2C1 Data Input/Output.
SDA2	31	53	59	I/O	I^2C	I2C2 Data Input/Output.
SDA3	3	3	5	I/O	I^2C	I2C3 Data Input/Output.
SOSCI	47	59	73	I	ANA	Secondary Oscillator/Timer1 Clock Input.
SOSCO	48	60	74	O	ANA	Secondary Oscillator/Timer1 Clock Output.
T1CK	48	60	74	I	ST	Timer1 Clock.
TCK	27	33	38	I	ST	JTAG Test Clock/Programming Clock Input.
TDI	28	34	60	I	ST	JTAG Test Data/Programming Data Input.
TDO	24	14	61	O	—	JTAG Test Data Output.
TMS	23	13	17	I	ST	JTAG Test Mode Select Input.
USBID	33	41	51	I	ST	USB OTG ID (OTG mode only).
USBOEN	12	16	21	O	—	USB Output Enable Control (for external transceiver).

Legend: TTL = TTL input buffer
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TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP			
VBUS	34	44	54	P	—	USB Voltage, Host mode (5V).
VBUSON	11	15	20	O	—	USB OTG External Charge Pump Control.
VBUSST	58	72	87	I	ANA	USB OTG Internal Charge Pump Feedback Control.
VCAP	56	70	85	P	—	External Filter Capacitor Connection (regulator enabled).
VCMPST1	58	72	87	I	ST	USB VBUS Boost Generator, Comparator Input 1.
VCMPST2	59	73	88	I	ST	USB VBUS Boost Generator, Comparator Input 2.
VCPCON	49	61	76	O	—	USB OTG VBUS PWM/Charge Output.
VDD	10, 26, 38	12, 32, 48	2, 16, 37, 46, 62	P	—	Positive Supply for Peripheral Digital Logic and I/O Pins.
VDDCORE	56	70	85	P	—	Positive Supply for Microcontroller Core Logic (regulator disabled).
VMIO	14	18	23	I/O	ST	USB Differential Minus Input/Output (external transceiver).
VPIO	13	17	22	I/O	ST	USB Differential Plus Input/Output (external transceiver).
VREF-	15	23	28	I	ANA	A/D and Comparator Reference Voltage (low) Input.
VREF+	16	24	29	I	ANA	A/D and Comparator Reference Voltage (high) Input.
VSS	9, 25, 41	11, 31, 51	15, 36, 45, 65, 75	P	—	Ground Reference for Logic and I/O Pins.
VUSB	35	45	55	P	—	USB Voltage (3.3V)

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