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PIC24FJ256GA412/GB412 FAMILY

16-Bit Flash Microcontrollers with Dual Partition Flash Memory, XLP, LCD, Cryptographic Engine and USB On-The-Go

Extreme Low-Power Features

- Multiple Power Management Options for Extreme Power Reduction:
  - VBAT allows for lowest power consumption on backup battery (with or without RTCC)
  - Deep Sleep allows near total power-down with the ability to wake-up on external triggers
  - Sleep and Idle modes selectively shut down peripherals and/or core for substantial power reduction and fast wake-up
  - Doze mode allows CPU to run at a lower clock speed than peripherals
- Alternate Clock modes allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction
- Extreme Low-Power Current Consumption for Deep Sleep:
  - WDT: 650 nA @ 2V typical
  - RTCC: 650 nA @ 32 kHz, 2V typical
  - Deep Sleep current, 60 nA typical
- 160 μA/MHz in Run mode

High-Performance CPU

- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Internal Oscillator:
  - 96 MHz PLL option
  - Multiple clock divide options
  - Run-time self-calibration capability for maintaining better than ±0.20% accuracy
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory

Cryptographic Engine

- Performs NIST Standard Encryption/Decryption Operations without CPU Intervention
- AES Cipher Support for 128, 192 and 256-Bit Keys
- DES/3DES Cipher Support, with up to Three Unique Keys for 3DES
- Supports ECB, CBC, OFB, CTR and CFB128 modes
- Programmatically Secure OTP Array for Key Storage
- True Random Number Generation
- Battery-Backed RAM Key Storage

Analog Features

- 10/12-Bit, up to 24-Channel Analog-to-Digital (A/D) Converter:
  - Conversion rate of 500 ksps (10-bit), 200 kbps (12-bit)
  - Auto-scan and threshold compare features
  - Conversion available during Sleep
- One 10-Bit Digital-to-Analog Converter (DAC):
  - 1 Msps update rate
- Three Rail-to-Rail, Enhanced Analog Comparators with Programmable Input/Output Configuration
- Charge Time Measurement Unit (CTMU):
  - Used for capacitive touch sensing, up to 24 channels
  - Time measurement down to 100 ps resolution

Dual Partition Flash with Live Update Capability

- Capable of Holding Two Independent Software Applications, including Bootloader
- Permits Simultaneous Programming of One Partition while Executing Application Code from the Other
- Allows Run-Time Switching Between Active Partitions

Universal Serial Bus Features (PIC24FJXXXGB4XX Only)

- USB v2.0 On-The-Go (OTG) Compliant
- Dual Role Capable – Can Act as Either Host or Peripheral
- Low-Speed (1.5 Mb/s) and Full-Speed (12 Mb/s) USB Operation in Host mode
- Full-Speed USB Operation in Device mode
- High-Precision PLL for USB
- USB Device mode Operation from FRC Oscillator – No Crystal Oscillator Required
- Supports up to 32 Endpoints (16 bidirectional):
  - USB module can use any RAM locations on the device as USB endpoint buffers
- On-Chip USB Transceiver with Interface for Off-Chip USB Transceiver
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- On-Chip Pull-up and Pull-Down Resistors

Special Microcontroller Features

- 20,000 Erase/Write Cycle Endurance, Typical
- Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Supply Voltage Range of 2.0V to 3.6V
- Two On-Chip Voltage Regulators (1.8V and 1.2V) for Regular and Extreme Low-Power Operation
- Programmable Reference Clock Output
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via 2 Pins
- JTAG Boundary Scan Support
- Fail-Safe Clock Monitor (FSCM) Operation:
  - Detects clock failure and switches to on-chip, Low-Power RC (LPRC) Oscillator
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Separate Brown-out Reset (BOR) and Deep Sleep Brown-out Reset (DSBOR) Circuits
- Programmable High/Low-Voltage Detect (HLVD)
- Flexible Watchdog Timer (WDT) with its Own RC Oscillator for Reliable Operation
- Standard and Ultra Low-Power Watchdog Timers (ULPW) for Reliable Operation in Standard and Deep Sleep modes
- Temperature Range: -40°C to +85°C

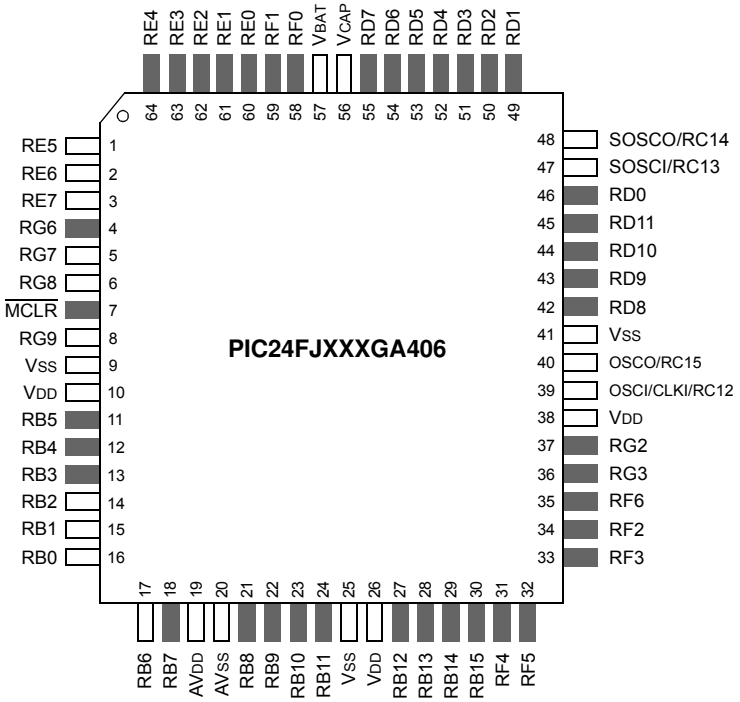
Device	Memory		Pins	Analog Peripherals				Digital Peripherals								USB OTG	Crypto Engine	LCD Controller (pixels)	Deep Sleep + VBAT
	Program (bytes)	Data (bytes)		10/12-Bit A/D (ch)	10-Bit DAC	Comparators	CTMU	MCCP/SCCP	16/32-Bit Timers	IC/OC-PWM	I2C	SPI	UART/IrDA®	EPMP/EPSP	CLC				
PIC24FJ256GA412	256K	16K	121	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	512	Y
PIC24FJ256GA410	256K	16K	100	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	480	Y
PIC24FJ256GA406	256K	16K	64	16	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	248	Y
PIC24FJ128GA412	128K	16K	121	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	512	Y
PIC24FJ128GA410	128K	16K	100	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	480	Y
PIC24FJ128GA406	128K	16K	64	16	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	248	Y
PIC24FJ64GA412	64K	8K	121	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	512	Y
PIC24FJ64GA410	64K	8K	100	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	480	Y
PIC24FJ64GA406	64K	8K	64	16	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	N	Y	248	Y
PIC24FJ256GB412	256K	16K	121	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	512	Y
PIC24FJ256GB410	256K	16K	100	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	480	Y
PIC24FJ256GB406	256K	16K	64	16	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	240	Y
PIC24FJ128GB412	128K	16K	121	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	512	Y
PIC24FJ128GB410	128K	16K	100	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	480	Y
PIC24FJ128GB406	128K	16K	64	16	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	240	Y
PIC24FJ64GB412	64K	8K	121	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	512	Y
PIC24FJ64GB410	64K	8K	100	24	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	480	Y
PIC24FJ64GB406	64K	8K	64	16	1	3	Y	1/6	31/15	6/6	3	4	6	Y	4	Y	Y	240	Y

Peripheral Features

- LCD Display Controller:
  - Up to 64 Segments by 8 Commons
  - Internal charge pump and low-power, internal resistor biasing
  - Operation in Sleep mode
- Up to Five External Interrupt Sources
- Peripheral Pin Select (PPS); allows Independent I/O Mapping of Many Peripherals
- Six-Channel DMA Supports All Peripheral modules:
  - Minimizes CPU overhead and increases data throughput
- Five 16-Bit Timers/Counters with Prescalers:
  - Can be paired as 32-bit timers/counters
- Using a combination of Timer, CCP, IC and OC Timers, the Device can be Configured to use up to 31 16-Bit Timers, and up to 15 32-Bit Timers
- Six Input Capture modules, each with a Dedicated 16-Bit Timer
- Six Output Compare/PWM modules, each with a Dedicated 16-Bit Timer
- Six Single Output CCPs (SCCP) and One Multiple Output CCP (MCCP) modules:
  - Independent 16/32-bit time base for each module
  - Internal time base and Period registers
  - Legacy PIC24F Capture and Compare modes (16 and 32-bit)
  - Special variable frequency pulse and Brushless DC Motor (BDCM) Output modes
- Enhanced Parallel Master/Slave Port (EPMP/EPSP)
- Hardware Real-Time Clock/Calendar (RTCC) with Timestamping:
  - Tamper detection with timestamping feature and tamper pin
  - Runs in Deep Sleep and VBAT modes
- Four 3-Wire/4-Wire SPI modules (support 4 Frame modes) with 8-Level FIFO Buffer
- Three I2C modules support Multi-Master/Slave mode and 7-Bit/10-Bit Addressing
- Six UART modules:
  - Support RS-485, RS-232 and LIN/J2602
  - On-chip hardware encoder/decoder for IrDA®
  - Auto-wake-up on Auto-Baud Detect (ABD)
  - 4-level deep FIFO buffer
- Programmable 32-Bit Cyclic Redundancy Check (CRC) Generator
- Four Configurable Logic Cells (CLCs):
  - Two inputs and one output, all mappable to peripherals or I/O pins
  - AND/OR/XOR logic and D/JK flip-flop functions
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Configurable Open-Drain Outputs on Digital I/O Pins
- 5.5V Tolerant Inputs on Multiple I/O Pins

Pin Diagrams

64-Pin TQFP
64-Pin QFN(1)



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 1 for a complete description of pin functions.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.

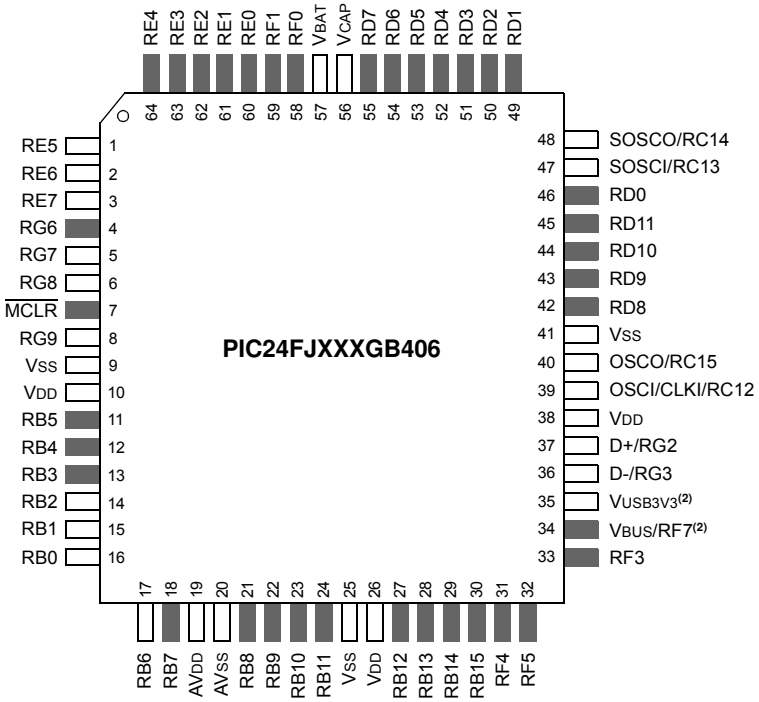
TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGA406 DEVICES

Pin	Function	Pin	Function
1	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	33	SEG12/**RP16**/IOCF3/RF3
2	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	34	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	35	IOCF6/RF6
4	SEG0/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	36	SDA1/IOCG3/RG3
5	VLCAP1/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	37	SCL1/IOCG2/RG2
6	VLCAP2/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/IOCC12/RC12
8	SEG1/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	40	OSCO/CLKO/IOCC15/RC15
9	VSS	41	VSS
10	VDD	42	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
11	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	43	SEG14/**RP4**/PMACK2/IOCD9/RD9
12	PGED3/SEG3/AN4/C1INB/**RP28**/IOCB4/RB4	44	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
13	SEG4/AN3/C2INA/IOCB3/RB3	45	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
14	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	46	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
15	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	47	SOSCI/IOCC13/RC13
16	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/PMA6/IOCB0/RB0	48	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
17	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	49	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
18	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	50	SEG21/**RP23**/PMACK1/IOCD2/RD2
19	AVDD	51	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
20	AVSS	52	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
21	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	53	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
22	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/IOCB9/RB9	54	SEG25/C3INB/U5RX/OC4/IOCD6/RD6
23	TMS/COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	55	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/IOCD7/RD7
24	TDO/AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	56	VCAP
25	VSS	57	VBAT
26	VDD	58	SEG27/$\overline{\text{U5CTS}}$/OC6/IOCF0/RF0
27	TCK/SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	59	COM4/SEG47/SCK4/IOCF1/RF1
28	TDI/SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	60	COM3/PMD0/IOCE0/RE0
29	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	61	COM2/PMD1/IOCE1/RE1
30	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	62	COM1/PMD2/IOCE2/RE2
31	SEG10/**RP10**/SDA2/PMA9/IOCF4/RF4	63	COM0/CTED9/PMD3/IOCE3/RE3
32	SEG11/**RP17**/SCL2/PMA8/IOCF5/RF5	64	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

64-Pin TQFP
64-Pin QFN(1)



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 2 for a complete description of pin functions.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.
2: PIC24FJ256GB406 devices use VUSB3V3 instead of RF6 and VBUS/RF7 instead of RF2.

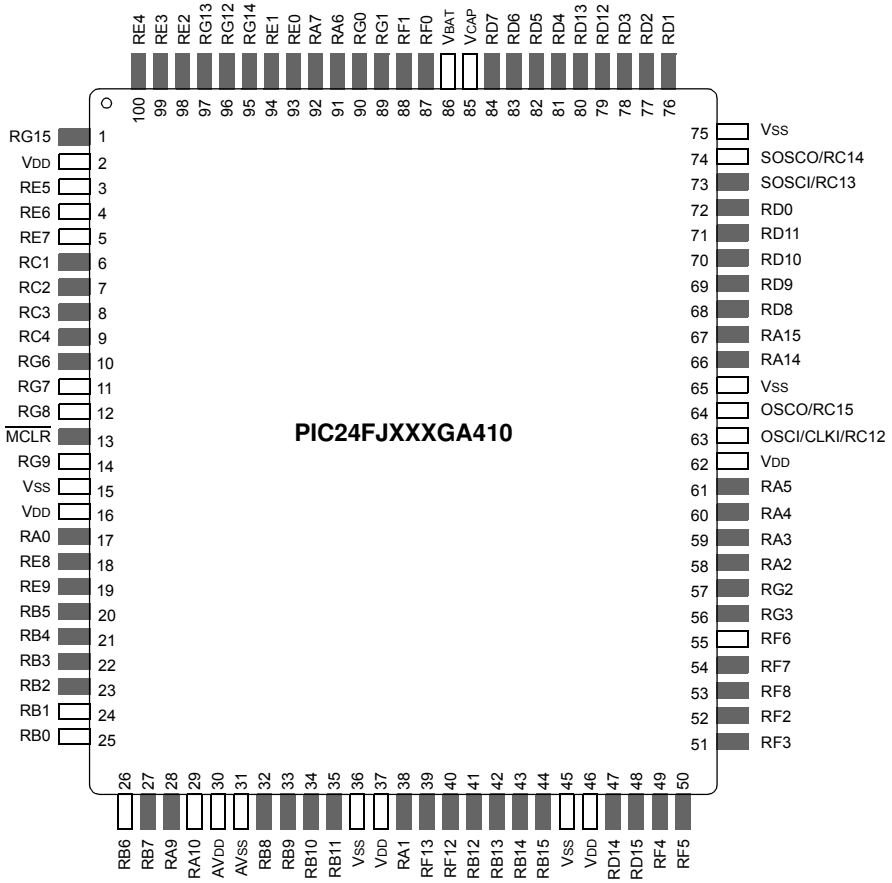
TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB406 DEVICES

Pin	Function	Pin	Function
1	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	33	SEG12/**RP16**/USBID/IOCF3/RF3
2	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	34	VBUS/IOCF7/RF7
3	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	35	VUSB3V3
4	SEG0/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	36	D-/IOCG3/RG3
5	VLCAP1/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	37	D+/IOCG2/RG2
6	VLCAP2/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/IOCC12/RC12
8	SEG1/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	40	OSCO/CLKO/IOCC15/RC15
9	VSS	41	VSS
10	VDD	42	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
11	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	43	SEG14/**RP4**/SDA1/PMACK2/IOCD9/RD9
12	PGED3/SEG3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/IOCB4/RB4	44	SEG15/C3IND/**RP3**/SCL1/PMA15/APMCS2/IOCD10/RD10
13	SEG4/AN3/C2INA/IOCB3/RB3	45	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
14	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	46	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
15	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	47	SOSCI/IOCC13/RC13
16	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/PMA6/IOCB0/RB0	48	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
17	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	49	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
18	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	50	SEG21/**RP23**/PMACK1/IOCD2/RD2
19	AVDD	51	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
20	AVSS	52	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
21	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	53	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
22	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/IOCB9/RB9	54	SEG25/C3INB/U5RX/OC4/IOCD6/RD6
23	TMS/COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	55	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/IOCD7/RD7
24	TDO/AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	56	VCAP
25	VSS	57	VBAT
26	VDD	58	SEG27/$\overline{\text{U5CTS}}$/OC6/IOCF0/RF0
27	TCK/SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	59	COM4/SEG47/SCK4/IOCF1/RF1
28	TDI/SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	60	COM3/PMD0/IOCE0/RE0
29	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	61	COM2/PMD1/IOCE1/RE1
30	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	62	COM1/PMD2/IOCE2/RE2
31	SEG10/**RP10**/SDA2/PMA9/IOCF4/RF4	63	COM0/CTED9/PMD3/IOCE3/RE3
32	SEG11/SCL2/PMA8/IOCF5/RF5	64	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

100-Pin TQFP



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 3 for a complete description of pin functions.

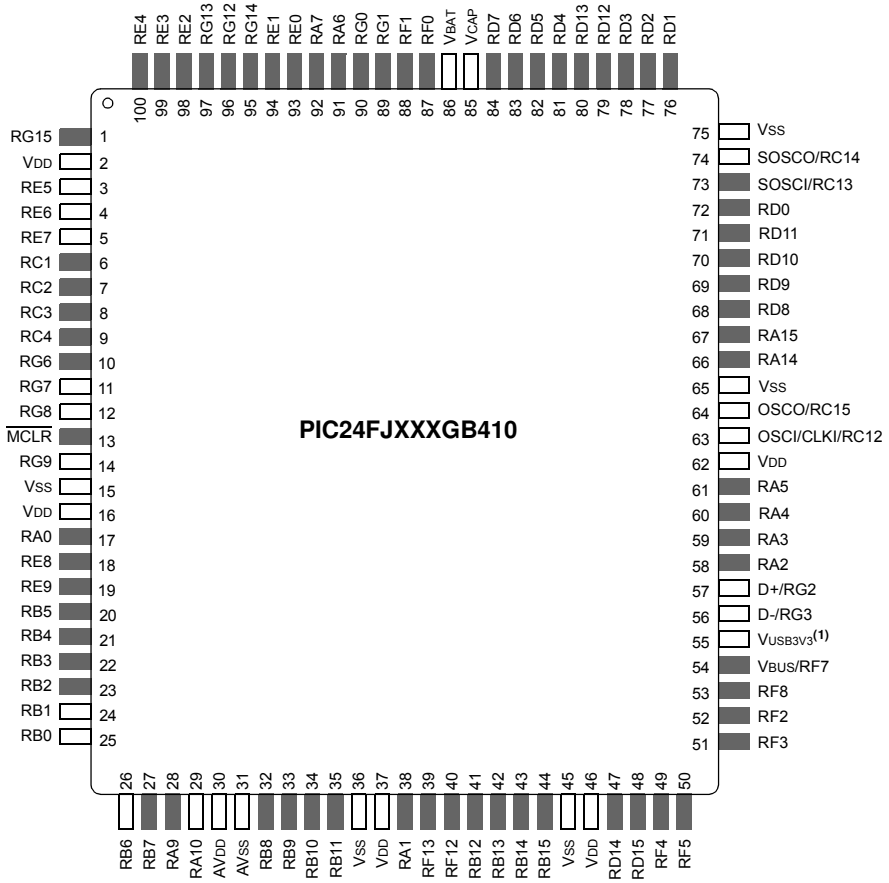
TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGA410 DEVICES

Pin	Function	Pin	Function
1	SEG50/OCM1C/CTED3/IOCG15/RG15	51	SEG12/**RP16**/IOCF3/RF3
2	VDD	52	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	53	SEG41/**RP15**/IOCF8/RF8
4	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	54	IOCF7/RF7
5	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	55	IOCF6/RF6
6	SEG32/**RPI38**/OCM1D/IOCC1/RC1	56	SDA1/IOCG3/RG3
7	SEG51/**RPI39**/IOCC2/RC2	57	SCL1/IOCG2/RG2
8	SEG33/**RPI40**/IOCC3/RC3	58	SEG55/SCL2/IOCA2/RA2
9	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4	59	SEG56/SDA2/PMA20/IOCA3/RA3
10	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	60	TDI/PMA21/IOCA4/RA4
11	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	61	TDO/SEG28/IOCA5/RA5
12	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/IOCC12/RC12
14	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	64	OSCO/CLKO/IOCC15/RC15
15	VSS	65	VSS
16	VDD	66	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
17	TMS/SEG48/CTED14/IOCA0/RA0	67	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
18	SEG34/**RPI33**/PMCS1/IOCE8/RE8	68	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
19	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9	69	SEG14/**RP4**/PMACK2/IOCD9/RD9
20	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	70	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
21	PGED3/SEG3/AN4/C1INB/**RP28**/IOCB4/RB4	71	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
22	SEG4/AN3/C2INA/IOCB3/RB3	72	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
23	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	73	SOSCI/IOCC13/RC13
24	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	74	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
25	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	75	VSS
26	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	76	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
27	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	77	SEG21/**RP23**/PMACK1/IOCD2/RD2
28	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9	78	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
29	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	79	SEG44/**RPI42**/PMD12/IOCD12/RD12
30	AVDD	80	SEG45/PMD13/IOCD13/RD13
31	AVSS	81	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
32	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	82	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
33	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9	83	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6
34	COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	84	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7
35	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	85	VCAP
36	VSS	86	VBAT
37	VDD	87	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0
38	TCK/IOCA1/RA1	88	COM4/SEG47/SCK4/PMD10/IOCF1/RF1
39	SEG53/**RP31**/IOCF13/RF13	89	SEG46/PMD9/IOCG1/RG1
40	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12	90	SEG49/PMD8/IOCG0/RG0
41	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	91	SEG57/AN23/OCM1E/IOCA6/RA6
42	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	92	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7
43	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	93	COM3/PMD0/IOCE0/RE0
44	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	94	COM2/PMD1/IOCE1/RE1
45	VSS	95	SEG59/CTED11/PMA16/IOCG14/RG14
46	VDD	96	SEG60/IOCG12/RG12
47	SEG38/**RPI43**/IOCD14/RD14	97	SEG61/CTED10/IOCG13/RG13
48	SEG39/**RP5**/IOCD15/RD15	98	COM1/PMD2/IOCE2/RE2
49	SEG10/**RP10**/PMA9/IOCF4/RF4	99	COM0/CTED9/PMD3/IOCE3/RE3
50	SEG11/**RP17**/PMA8/IOCF5/RF5	100	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

100-Pin TQFP



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 4 for a complete description of pin functions.
Note 1: PIC24FJ256GB410 devices use VUSB3V3 instead of RF6.

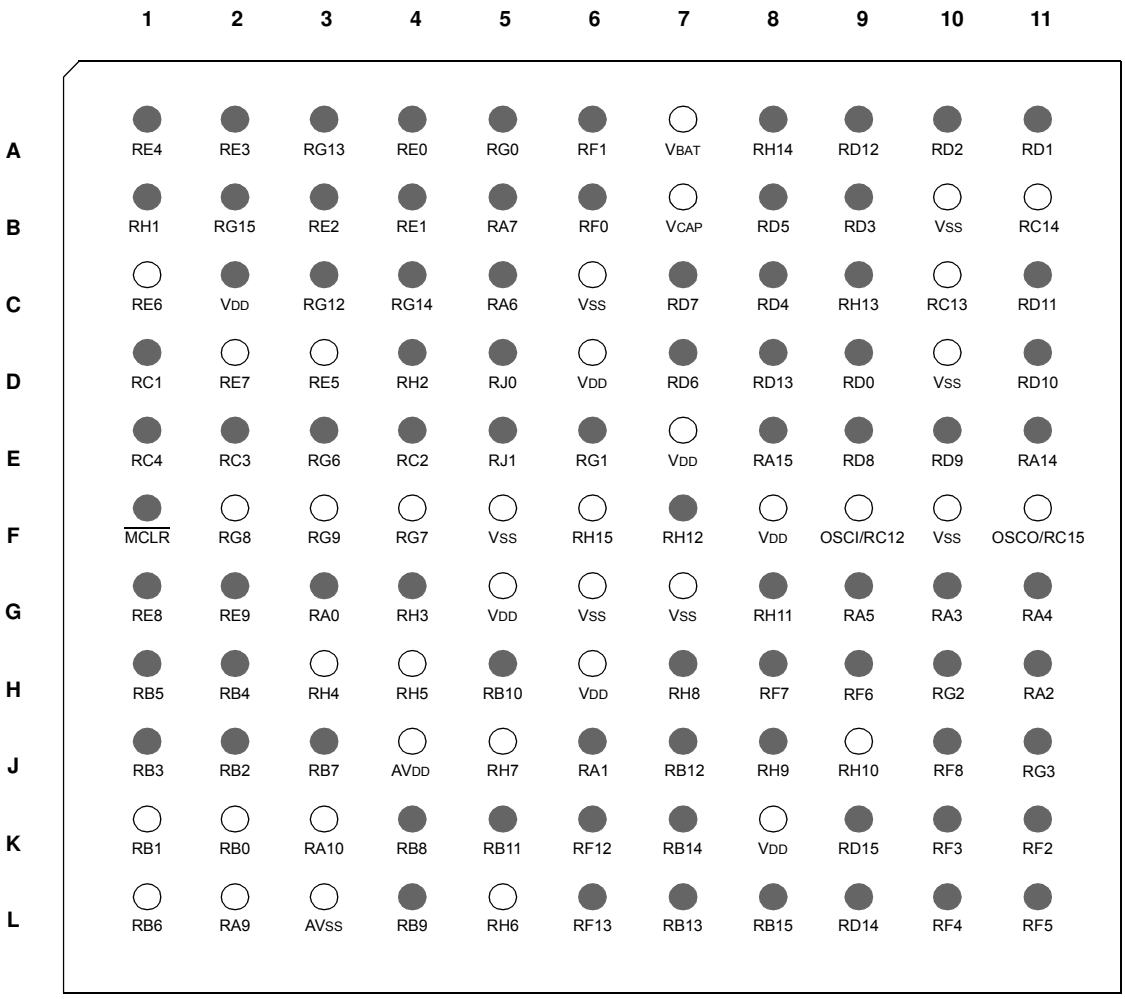
TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB410 DEVICES

Pin	Function	Pin	Function
1	SEG50/OCM1C/CTED3/IOCG15/RG15	51	SEG12/**RP16**/USBID/IOCF3/RF3
2	VDD	52	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	53	SEG41/**RP15**/IOCF8/RF8
4	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	54	VBUS/IOCF7/RF7
5	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	55	VUSB3V3
6	SEG32/**RPI38**/OCM1D/IOCC1/RC1	56	D-/IOCG3/RG3
7	SEG51/**RPI39**/IOCC2/RC2	57	D+/IOCG2/RG2
8	SEG33/**RPI40**/IOCC3/RC3	58	SEG55/SCL2/IOCA2/RA2
9	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4	59	SEG56/SDA2/PMA20/IOCA3/RA3
10	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	60	TDI/PMA21/IOCA4/RA4
11	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	61	TDO/SEG28/IOCA5/RA5
12	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/IOCC12/RC12
14	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	64	OSCO/CLKO/IOCC15/RC15
15	VSS	65	VSS
16	VDD	66	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
17	TMS/SEG48/CTED14/IOCA0/RA0	67	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
18	SEG34/**RPI33**/PMCS1/IOCE8/RE8	68	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
19	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9	69	SEG14/**RP4**/PMACK2/IOCD9/RD9
20	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	70	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
21	PGED3/SEG3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/IOCB4/RB4	71	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
22	SEG4/AN3/C2INA/IOCB3/RB3	72	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
23	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	73	SOSCI/IOCC13/RC13
24	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	74	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
25	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	75	VSS
26	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	76	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
27	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	77	SEG21/**RP23**/PMACK1/IOCD2/RD2
28	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9	78	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
29	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	79	SEG44/**RPI42**/PMD12/IOCD12/RD12
30	AVDD	80	SEG45/PMD13/IOCD13/RD13
31	AVSS	81	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
32	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	82	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
33	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9	83	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6
34	COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	84	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7
35	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	85	VCAP
36	VSS	86	VBAT
37	VDD	87	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0
38	TCK/IOCA1/RA1	88	COM4/SEG47/SCK4/PMD10/IOCF1/RF1
39	SEG53/**RP31**/IOCF13/RF13	89	SEG46/PMD9/IOCG1/RG1
40	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12	90	SEG49/PMD8/IOCG0/RG0
41	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	91	SEG57/AN23/OCM1E/IOCA6/RA6
42	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	92	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7
43	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	93	COM3/PMD0/IOCE0/RE0
44	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	94	COM2/PMD1/IOCE1/RE1
45	VSS	95	SEG59/CTED11/PMA16/IOCG14/RG14
46	VDD	96	SEG60/IOCG12/RG12
47	SEG38/**RPI43**/IOCD14/RD14	97	SEG61/CTED10/IOCG13/RG13
48	SEG39/**RP5**/IOCD15/RD15	98	COM1/PMD2/IOCE2/RE2
49	SEG10/**RP10**/PMA9/IOCF4/RF4	99	COM0/CTED9/PMD3/IOCE3/RE3
50	SEG11/**RP17**/PMA8/IOCF5/RF5	100	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

PIC24FJXXXGA412, 121-Pin TFBGA



Legend: **Shaded balls** indicate pins tolerant to up to +5.5 VDC. See Table 5 for a complete description of pin functions.

TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGA412

Pin	Function	Pin	Function
A1	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4	E1	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4
A2	COM0/CTED9/PMD3/IOCE3/RE3	E2	SEG33/**RPI40**/IOCC3/RC3
A3	SEG61/CTED10/IOCG13/RG13	E3	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6
A4	COM3/PMD0/IOCE0/RE0	E4	SEG51/**RPI39**/IOCC2/RC2
A5	SEG49/PMD8/IOCG0/RG0	E5	IOCJ1/RJ1
A6	SEG47/SCK4/PMD10/IOCF1/RF1	E6	SEG46/PMD9/IOCG1/RG1
A7	VBAT	E7	VDD
A8	IOCH14/RH14	E8	SEG43/**RPI35**/PMBE1/IOCA15/RA15
A9	SEG44/**RPI42**/PMD12/IOCD12/RD12	E9	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
A10	SEG21/**RP23**/PMACK1/IOCD2/RD2	E10	SEG14/**RP4**/PMACK2/IOCD9/RD9
A11	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1	E11	SEG42/**RPI36**/PMA22/IOCA14/RA14
B1	COM4/IOCH1/RH1	F1	$\overline{\text{MCLR}}$
B2	SEG50/OCM1C/CTED3/IOCG15/RG15	F2	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8
B3	COM1/PMD2/IOCE2/RE2	F3	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/ IOCG9/RG9
B4	COM2/PMD1/IOCE1/RE1	F4	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7
B5	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7	F5	VSS
B6	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0	F6	IOCH15/RH15
B7	VCAP	F7	IOCH12/RH12
B8	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5	F8	VDD
B9	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3	F9	OSCI/CLKI/IOCC12/RC12
B10	VSS	F10	VSS
B11	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14	F11	OSCO/CLKO/IOCC15/RC15
C1	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	G1	SEG34/**RPI33**/PMCS1/IOCE8/RE8
C2	VDD	G2	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9
C3	SEG60/IOCG12/RG12	G3	TMS/SEG48/CTED14/IOCA0/RA0
C4	SEG59/CTED11/PMA16/IOCG14/RG14	G4	COM6/IOCH3/RH3
C5	SEG57/AN23/OCM1E/IOCA6/RA6	G5	VDD
C6	VSS	G6	VSS
C7	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7	G7	VSS
C8	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4	G8	IOCH11/RH11
C9	IOCH13/RH13	G9	TDO/SEG28/IOCA5/RA5
C10	SOSCI/IOCC13/RC13	G10	SEG56/SDA2/PMA20/IOCA3/RA3
C11	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11	G11	TDI/PMA21/IOCA4/RA4
D1	SEG32/**RPI38**/OCM1D/IOCC1/RC1	H1	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5
D2	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	H2	PGED3/SEG3/AN4/C1INB/**RP28**/IOCB4/RB4
D3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	H3	COM7/IOCH4/RH4
D4	COM5/IOCH2/RH2	H4	IOCH5/RH5
D5	IOCJ0/RJ0	H5	SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10
D6	VDD	H6	VDD
D7	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6	H7	IOCH8/RH8
D8	SEG45/PMD13/IOCD13/RD13	H8	IOCF7/RF7
D9	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0	H9	IOCF6/RF6
D10	VSS	H10	SCL1/IOCG2/RG2
D11	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10	H11	SEG55/SCL2/IOCA2/RA2

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

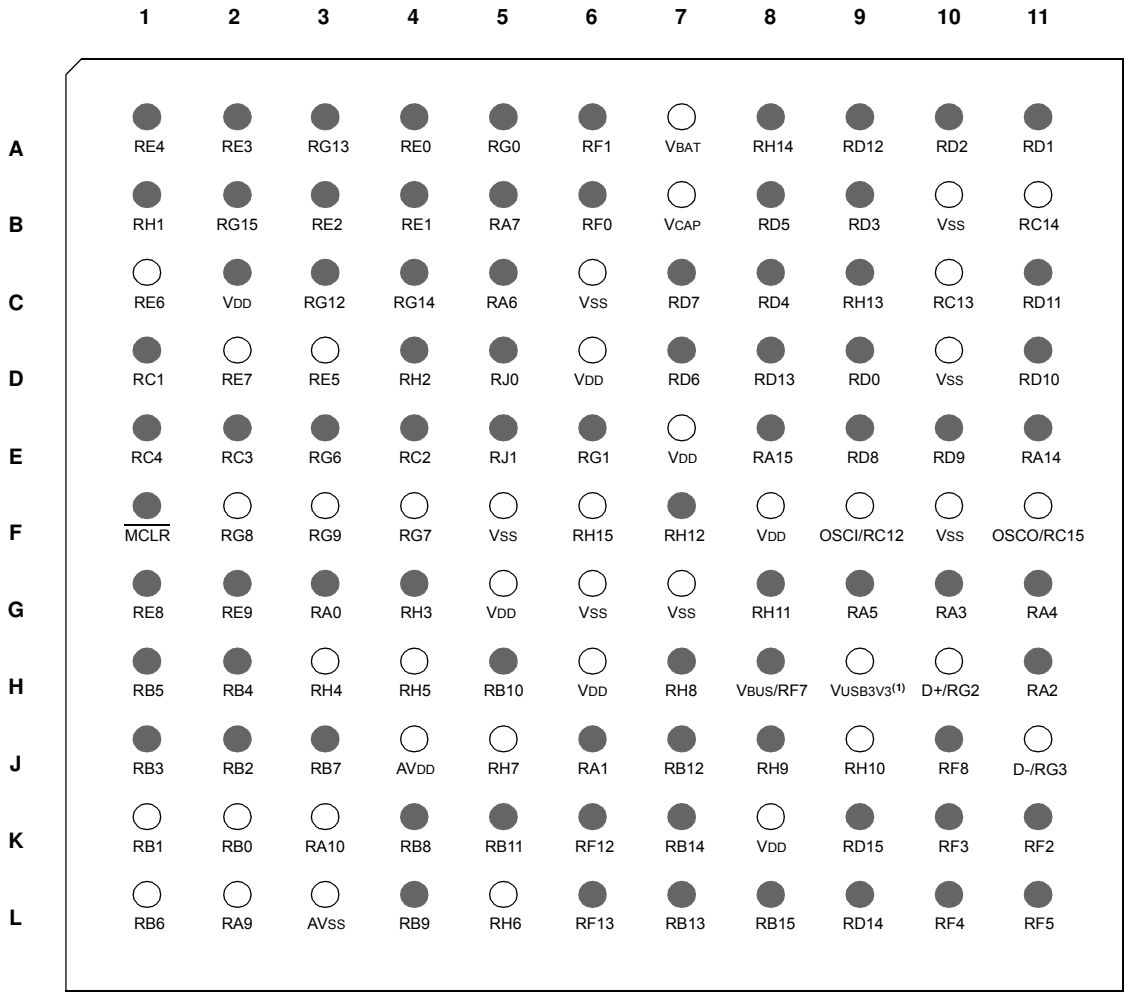
TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGA412 (CONTINUED)

Pin	Function	Pin	Function
J1	SEG4/AN3/C2INA/IOCB3/RB3	K7	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14
J2	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	K8	VDD
J3	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	K9	SEG39/**RP5**/IOCD15/RD15
J4	AVDD	K10	SEG12/**RP16**/IOCF3/RF3
J5	IOCH7/RH7	K11	SEG40/**RP30**/IOCF2/RF2
J6	TCK/IOCA1/RA1	L1	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6
J7	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	L2	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9
J8	IOCH9/RH9	L3	AVSS
J9	IOCH10/RH10	L4	SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9
J10	SEG41/**RP15**/IOCF8/RF8	L5	IOCH7/RH7
J11	SDA1/IOCG3/RG3	L6	SEG53/**RP31**/IOCF13/RF13
K1	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	L7	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13
K2	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/RP0/IOCB0/RB0	L8	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15
K3	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	L9	SEG38/**RPI43**/IOCD14/RD14
K4	SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	L10	SEG10/**RP10**/PMA9/IOCF4/RF4
K5	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	L11	SEG11/**RP17**/PMA8/IOCF5/RF5
K6	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

PIC24FJXXXGB412, 121-Pin TFBGA



Legend: **Shaded balls** indicate pins tolerant to up to +5.5 VDC. See Table 6 for a complete description of pin functions.
Note 1: PIC24FJ256GB412 devices use VUSB3V3 instead of RF6.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB412

Pin	Function	Pin	Function
A1	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4	E1	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4
A2	COM0/CTED9/PMD3/IOCE3/RE3	E2	SEG33/**RPI40**/IOCC3/RC3
A3	SEG61/CTED10/IOCG13/RG13	E3	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6
A4	COM3/PMD0/IOCE0/RE0	E4	SEG51/**RPI39**/IOCC2/RC2
A5	SEG49/PMD8/IOCG0/RG0	E5	IOCJ1/RJ1
A6	SEG47/SCK4/PMD10/IOCF1/RF1	E6	SEG46/PMD9/IOCG1/RG1
A7	VBAT	E7	VDD
A8	IOCH14/RH14	E8	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
A9	SEG44/**RPI42**/PMD12/IOCD12/RD12	E9	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
A10	SEG21/**RP23**/PMACK1/IOCD2/RD2	E10	SEG14/**RP4**/PMACK2/IOCD9/RD9
A11	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1	E11	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
B1	COM4/IOCH1/RH1	F1	$\overline{\text{MCLR}}$
B2	SEG50/OCM1C/CTED3/IOCG15/RG15	F2	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8
B3	COM1/PMD2/IOCE2/RE2	F3	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/ IOCG9/RG9
B4	COM2/PMD1/IOCE1/RE1	F4	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7
B5	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7	F5	VSS
B6	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0	F6	IOCH15/RH15
B7	VCAP	F7	IOCH12/RH12
B8	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5	F8	VDD
B9	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3	F9	OSCI/CLKI/IOCC12/RC12
B10	VSS	F10	VSS
B11	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14	F11	OSCO/CLKO/IOCC15/RC15
C1	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	G1	SEG34/**RPI33**/PMCS1/IOCE8/RE8
C2	VDD	G2	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9
C3	SEG60/IOCG12/RG12	G3	TMS/SEG48/CTED14/IOCA0/RA0
C4	SEG59/CTED11/PMA16/IOCG14/RG14	G4	COM6/IOCH3/RH3
C5	SEG57/AN23/OCM1E/IOCA6/RA6	G5	VDD
C6	VSS	G6	VSS
C7	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7	G7	VSS
C8	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4	G8	IOCH11/RH11
C9	IOCH13/RH13	G9	TDO/SEG28/IOCA5/RA5
C10	SOSCI/IOCC13/RC13	G10	SEG56/SDA2/PMA20/IOCA3/RA3
C11	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11	G11	TDI/PMA21/IOCA4/RA4
D1	SEG32/**RPI38**/OCM1D/IOCC1/RC1	H1	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5
D2	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	H2	PGED3/SEG3/AN4/C1INB/**RP28**/$\overline{\text{USBOE}}$/IOCB4/RB4
D3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	H3	COM7/IOCH4/RH4
D4	COM5/IOCH2/RH2	H4	IOCH5/RH5
D5	IOCJ0/RJ0	H5	SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10
D6	VDD	H6	VDD
D7	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6	H7	IOCH8/RH8
D8	SEG45/PMD13/IOCD13/RD13	H8	VBUS/IOCF7/RF7
D9	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0	H9	VUSB3V3
D10	VSS	H10	D+/IOCG2/RG2
D11	SEG15/C3IND/RP3/PMA15/APMCS2/IOCD10/RD10	H11	SEG55/SCL2/IOCA2/RA2

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB412 (CONTINUED)

Pin	Function	Pin	Function
J1	SEG4/AN3/C2INA/IOCB3/RB3	K7	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14
J2	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	K8	VDD
J3	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	K9	SEG39/**RP5**/IOCD15/RD15
J4	AVDD	K10	SEG12/**RP16**/USBID/IOCF3/RF3
J5	IOCH7/RH7	K11	SEG40/**RP30**/IOCF2/RF2
J6	TCK/IOCA1/RA1	L1	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6
J7	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	L2	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9
J8	IOCH9/RH9	L3	AVSS
J9	IOCH10/RH10	L4	SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9
J10	SEG41/**RP15**/IOCF8/RF8	L5	IOCH6/RH6
J11	D-/IOCG3/RG3	L6	SEG53/**RP31**/IOCF13/RF13
K1	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	L7	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13
K2	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	L8	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15
K3	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	L9	SEG38/**RPI43**/IOCD14/RD14
K4	SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	L10	SEG10/**RP10**/PMA9/IOCF4/RF4
K5	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	L11	SEG11/**RP17**/PMA8/IOCF5/RF5
K6	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GA406
- PIC24FJ128GA406
- PIC24FJ256GA406
- PIC24FJ64GA410
- PIC24FJ128GA410
- PIC24FJ256GA410
- PIC24FJ64GA412
- PIC24FJ128GA412
- PIC24FJ256GA412
- PIC24FJ64GB406
- PIC24FJ128GB406
- PIC24FJ256GB406
- PIC24FJ64GB410
- PIC24FJ128GB410
- PIC24FJ256GB410
- PIC24FJ64GB412
- PIC24FJ128GB412
- PIC24FJ256GB412

The PIC24FJ256GA412/GB412 family expands the capabilities of the PIC24F family by adding a complete selection of advanced analog peripherals to its existing digital features. This combination, along with its ultra low-power features, Direct Memory Access (DMA) for peripherals, USB On-The-Go (OTG) and a built-in LCD Controller and driver, makes this family the new standard for mixed-signal PIC® microcontrollers in one economical and power-saving package.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 XLP POWER-SAVING TECHNOLOGY

The PIC24FJ256GA412/GB412 family of devices incorporates a greatly expanded range of power-saving operating modes for the ultimate in power conservation. The new modes include:

- Retention Sleep, with essential circuits being powered from a separate low-voltage regulator
- Deep Sleep without RTCC, for the lowest possible power consumption under software control
- V_{BAT} mode (with or without RTCC), to continue limited operation from a backup battery when V_{DD} is removed

Many of these new low-power modes also support the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from these new features, the PIC24FJ256GA412/GB412 devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of Idle and the many Sleep modes

1.1.3 DUAL PARTITION FLASH PROGRAM MEMORY

A brand new feature to the PIC24F family is the use of Dual Partition Flash program memory technology. This allows PIC24FJ256GA412/GB412 family devices a range of new operating options not available before:

- Dual Partition Operation, which can store two different applications in their own code partition, and allows for the support of robust bootloader applications and enhanced security
- Live Update Operation, which allows the main application to continue operation while the second Flash partition is being reprogrammed – all without adding Wait states to code execution
- Direct Run-Time Programming from Data RAM, with the option of data compression in the RAM image

PIC24FJ256GA412/GB412 family devices can also operate with their two Flash partitions as one large program memory, providing space for large and complex applications.

1.1.4 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ256GA412/GB412 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- Two External Clock modes
- A Phase-Locked Loop (PLL) frequency multiplier, which allows clock speeds of up to 32 MHz
- A Fast Internal Oscillator (FRC) – nominal 8 MHz output with multiple frequency divider options and automatic frequency self-calibration during run time
- A separate Low-Power Internal RC Oscillator (LPRC) – 31 kHz nominal for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, while still selecting a Microchip device.

1.2 Cryptographic Engine

The Cryptographic Engine provides a new set of data security options. Using its own free-standing math engine, the module can independently perform NIST standard encryption and decryption of data, independently of the CPU. The Cryptographic Engine supports AES and DES/3DES encryption ciphers in up to 5 modes, and supports key lengths from 128 to 256 bits. Additional features include True Random Number Generation (TRNG) within the engine, multiple encryption/decryption key storage options and secure data handling that prevents data in the engine from being compromised by external reads.

1.3 USB On-The-Go (OTG)

USB On-The-Go provides on-chip functionality as a target device compatible with the USB 2.0 standard, as well as limited stand-alone functionality as a USB embedded host. By implementing USB Host Negotiation Protocol (HNP), the module can also dynamically switch between device and host operation, allowing for a much wider range of versatile USB-enabled applications on a microcontroller platform.

PIC24FJ256GA412/GB412 family devices also incorporate an integrated USB transceiver and precision oscillator, minimizing the required complexity of implementing a complete USB device, embedded host, dual role or On-The-Go application.

1.4 DMA Controller

PIC24FJ256GA412/GB412 family devices also add a Direct Memory Access (DMA) Controller to the existing PIC24F architecture. The DMA acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Six independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.5 LCD Controller

The versatile on-chip LCD Controller includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump and an integrated internal resistor ladder that allows contrast control in software, and display operation above device V_{DD}.

1.6 Other Special Features

- **Integrated Interrupt-on-Change:** All digital I/O ports now feature Interrupt-on-Change (IOC) functionality for convenient Change Notification interrupt generation on any I/O pin. IOC can be individually enabled or disabled on each pin, and configured for both edge detection polarity and the use of pull-ups or pull-downs.
- **Peripheral Pin Select (PPS):** The Peripheral Pin Select feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ256GA412/GB412 family incorporates multiple serial communication peripherals to handle a range of application requirements. All devices have six independent UARTs with built-in IrDA® encoders/decoders. There are also three independent I^2C modules that support both Master and Slave modes of operation, and three SPI modules with I^2S and variable data width support.
- **Analog Features:** All members of the PIC24FJ256GA412/GB412 family include a 12-bit A/D Converter module, a triple comparator module and the CTMU interface. The A/D module incorporates a range of features that allow the converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions.
  The comparator module includes three analog comparators that are configurable for a wide range of operations. The CTMU provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits, and address widths of up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.7 Details on Individual Family Members

Devices in the PIC24FJ256GA412/GB412 family are available in 64-pin, 100-pin and 121-pin packages. General block diagrams for general purpose and USB devices are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in five ways:

1. USB On-The-Go functionality (present only in PIC24FJXXXGB4XX devices).
2. Available I/O pins and ports (up to 53 pins on 6 ports for 64-pin devices, up to 85 pins on 7 ports for 100-pin devices and up to 102 pins on 9 ports for 121-pin devices).
3. Available remappable pins (29 pins on 64-pin devices and 44 pins on 100/121-pin devices).
4. Maximum available drivable LCD pixels (up to 248 for 64-pin devices and 512 on 100/121-pin devices.)
5. Analog input channels for the A/D Converter (16 channels for 64-pin devices and 24 channels for 100/121-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

A list of pin features available on the PIC24FJ256GA412/GB412 family devices, sorted by function, is shown in Table 1-4 (for general purpose devices) or Table 1-5 (for USB devices). Note that these tables show the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 64-PIN

Features	PIC24FJXXXGA/GB406					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports B, C, D, E, F, G					
Total I/O Pins	53			52		
Remappable Pins	30 (29 I/Os, 1 input only)			29 (28 I/Os, 1 input only)		
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Capture/Compare/PWM/Timer:						
Single Output (SCCP)	6(2)					
Multiple Output (MCCP)	1(2)					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	16					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	248 (35 SEG x 8 COM)			240 (34 SEG x 8 COM)		
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	64-Pin TQFP and QFN					

Note 1: Includes the Timer modes of the SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 100-PIN

Features	PIC24FJXXXGA/GB410					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G					
Total I/O Pins	85			84		
Remappable Pins	44 (32 I/Os, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Capture/Compare/PWM/Timer:						
Single Output (SCCP)	6(2)					
Multiple Output (MCCP)	1(2)					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	100-Pin TQFP					

Note 1: Includes the Timer modes of the SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

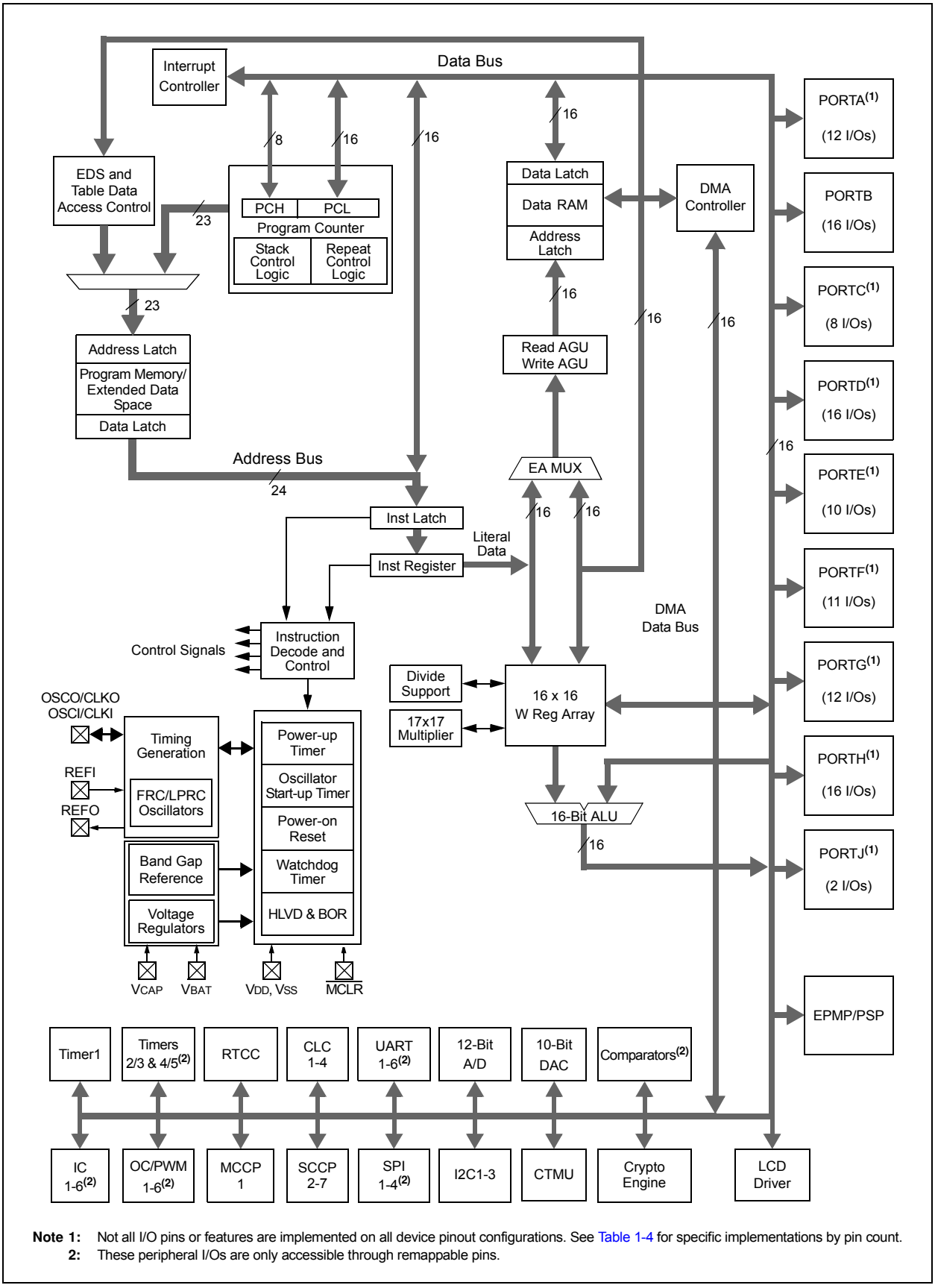
TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 121-PIN

Features	PIC24FJXXXGA/GB412					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G, H, J					
Total I/O Pins	102			101		
Remappable Pins	44 (32 I/O, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Single Output CCP (SCCP)	6					
Multiple Output CCP (MCCP)	1					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	121-Pin TFBGA					

Note 1: Includes the Timer modes of SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

FIGURE 1-1: PIC24FJ256GA412 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-4 for specific implementations by pin count.
2: These peripheral I/Os are only accessible through remappable pins.