Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC24FJ128GC010 FAMILY

16-Bit Flash Microcontrollers with 12-Bit Pipeline A/D, Sigma-Delta A/D, USB On-The-Go and XLP Technology

Advanced Analog Features

- 12-Bit, up to 50-Channel, High-Speed, Pipeline Analog-to-Digital Converter (A/D):
  - Conversion rates up to 10 Msps
  - Compatibility features for low conversion rates
  - Flexible operating modes with auto-accumulate, Threshold Detect and channel scan using sample lists
  - Conversion available during Sleep and Idle
- 16-Bit Sigma-Delta Analog-to-Digital Converter (A/D):
  - Programmable data rate with dithering option and adjustable oversampling ratios
  - Two differential channels
  - Configurable input gain stage
- Two 10-Bit Digital-to-Analog Converters (DAC):
  - Fast settling time supports 1 Msps update rate
- Two Rail-to-Rail, Input/Output, General Purpose Operational Amplifiers:
  - 2.5 MHz gain bandwidth product (typical)
  - Flexible input multiplexing options
  - Optional Comparator mode
- Three Rail-to-Rail, Enhanced Analog Comparators with Programmable Input/Output Configuration
- Three On-Chip Programmable Voltage References
- Charge Time Measurement Unit (CTMU):
  - Used for capacitive touch sensing, up to 50 channels
  - Time measurement down to 100 ps resolution
  - Operation in Sleep mode

Extreme Low-Power Features

- Multiple Power Management Options for Extreme Power Reduction:
  - VBAT allows for lowest power consumption on backup battery (with or without RTCC)
  - Deep Sleep allows near total power-down, with the ability to wake-up on internal or external triggers
  - Full RAM and state retention in select Deep Sleep and VBAT modes
  - Sleep and Idle modes selectively shut down peripherals and/or core for substantial power reduction and fast wake-up
  - Doze mode allows CPU to run at a lower clock speed than peripherals
- Alternate Clock modes allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction
- Extreme Low-Power Current Consumption for Deep Sleep:
  - WDT: 270 nA @ 3.3V, typical
  - RTCC: 350 nA @ 32 kHz, 3.3V, typical
  - Deep Sleep current, 75 nA, 3.3V, typical

Device	Memory		Pins	Analog Peripherals						Digital Peripherals							LCD Controller (pixels)	USB OTG	Deep Sleep w/VBAT
	Program Flash (bytes)	Data RAM (bytes)		12-Bit HS A/D (ch)	16-Bit ΣΔ A/D (diff ch)	10-Bit DAC	Op Amps	Comparators	CTMU (ch)	Input Capture	Output Compare/PWM	I2C	SPI	UART w/IrDA®	EPMP/PSP	16-Bit Timers			
PIC24FJ128GC010	128K	8K	100	50	2	2	2	3	50	9	9	2	2	4	Y	5	472	Y	Y
PIC24FJ128GC006	128K	8K	64	30	2	2	2	3	30	9	9	2	2	4	Y	5	248	Y	Y
PIC24FJ64GC010	64K	8K	100	50	2	2	2	3	50	9	9	2	2	4	Y	5	472	Y	Y
PIC24FJ64GC006	64K	8K	64	30	2	2	2	3	30	9	9	2	2	4	Y	5	248	Y	Y

Universal Serial Bus Features

- USB v2.0 On-The-Go (OTG) Compliant
- USB Device mode Operation from FRC Oscillator – No Crystal Oscillator Required
- Dual Role Capable – Can Act as Either Host or Peripheral
- Low-Speed (1.5 Mb/s) and Full-Speed (12 Mb/s) USB Operation in Host mode
- Full-Speed USB Operation in Device mode
- Low Jitter PLL for USB
- Supports up to 32 Endpoints (16 bidirectional):
  - USB module can use any RAM location on the device as USB endpoint buffers
- On-Chip USB Transceiver with Interface for Off-Chip USB Transceiver
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- On-Chip Pull-up and Pull-Down Resistors

Peripheral Features

- LCD Display Controller:
  - Up to 59 segments by 8 commons
  - Internal charge pump and low-power, internal resistor biasing
  - Operation in Sleep mode
- Up to Five External Interrupt Sources
- Peripheral Pin Select (PPS); Allows Independent I/O Mapping of Many Peripherals
- Five 16-Bit Timers/Counters with Prescaler:
  - Can be paired as 32-bit timers/counters
- Six-Channel DMA Supports All Peripheral modules:
  - Minimizes CPU overhead, increases data throughput and lowers power consumption
- Nine Input Capture modules, each with a Dedicated 16-Bit Timer
- Nine Output Compare/PWM modules, each with a Dedicated 16-Bit Timer
- Enhanced Parallel Master/Slave Port (EPMP/EPSP)
- Hardware Real-Time Clock and Calendar (RTCC):
  - Run, Sleep, Deep Sleep and V_{BAT} modes
- Two 3-Wire/4-Wire SPI modules (support 4 Frame modes) with 8-Level FIFO Buffer
- Two I^2C modules Support Multi-Master/Slave mode and 7-Bit/10-Bit Addressing
- Four UART modules:
  - Support RS-485, RS-232 and LIN/J2602
  - On-chip hardware encoder/decoder for IrDA®
  - Auto-wake-up on Auto-Baud Detect (ABD)
  - 4-level deep FIFO buffer
- Programmable, 32-Bit Cyclic Redundancy Check (CRC) Generator
- Digital Signal Modulator (DSM) Provides On-Chip FSK and PSK Modulation for a Digital Signal Stream
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Configurable Open-Drain Outputs on Digital I/O Pins
- 5.5V Tolerant Inputs on Select Pins

High-Performance CPU

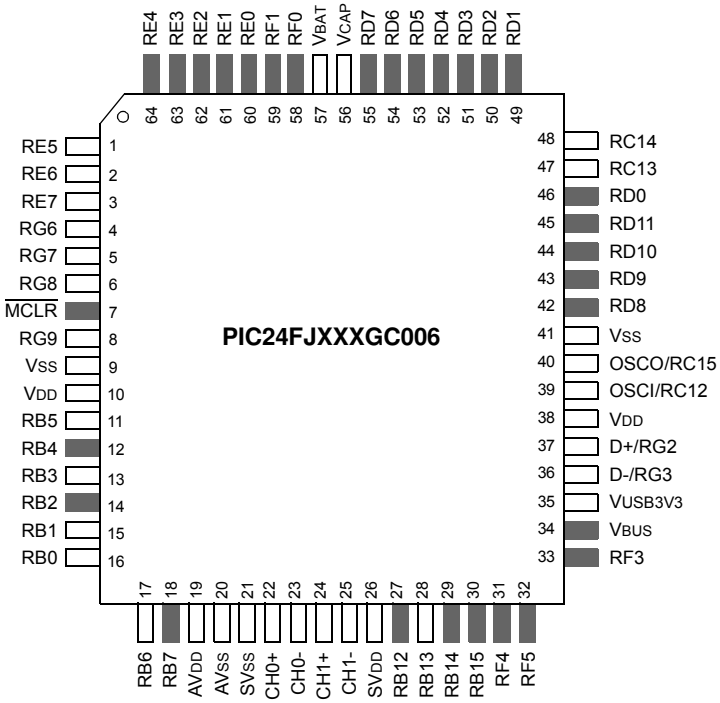
- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- C Compiler Optimized Instruction Set Architecture (ISA)
- 8 MHz Internal Oscillator:
  - 96 MHz PLL option for USB clocking
  - Multiple clock divide options
  - Run-time self-calibration capability for maintaining better than ±0.20% accuracy
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- Two Address Generation Units (AGUs) for Separate Read and Write Addressing of Data Memory

Special Microcontroller Features

- Supply Voltage Range of 2.0V to 3.6V
- Two On-Chip Voltage Regulators (1.8V and 1.2V) for Regular and eXtreme Low-Power Operation
- 20,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- Flash Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Programmable Reference Clock Output
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via 2 Pins
- JTAG Boundary Scan Support
- Fail-Safe Clock Monitor Operation:
  - Detects clock failure and switches to on-chip, low-power RC Oscillator
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Separate Brown-out Reset (BOR) and Deep Sleep Brown-out Reset (DSBOR) Circuits
- Programmable High/Low-Voltage Detect (HLVD)
- Flexible Watchdog Timer (WDT) with its Own RC Oscillator for Reliable Operation
- Standard and Ultra Low-Power Watchdog Timers for Reliable Operation in Standard and Deep Sleep modes

Pin Diagrams

64-Pin TQFP (10 mm x 10 mm)
64-Pin QFN (9 mm x 9 mm)(1)



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 1 for a complete description of pin functions.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.

TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 64-PIN DEVICES

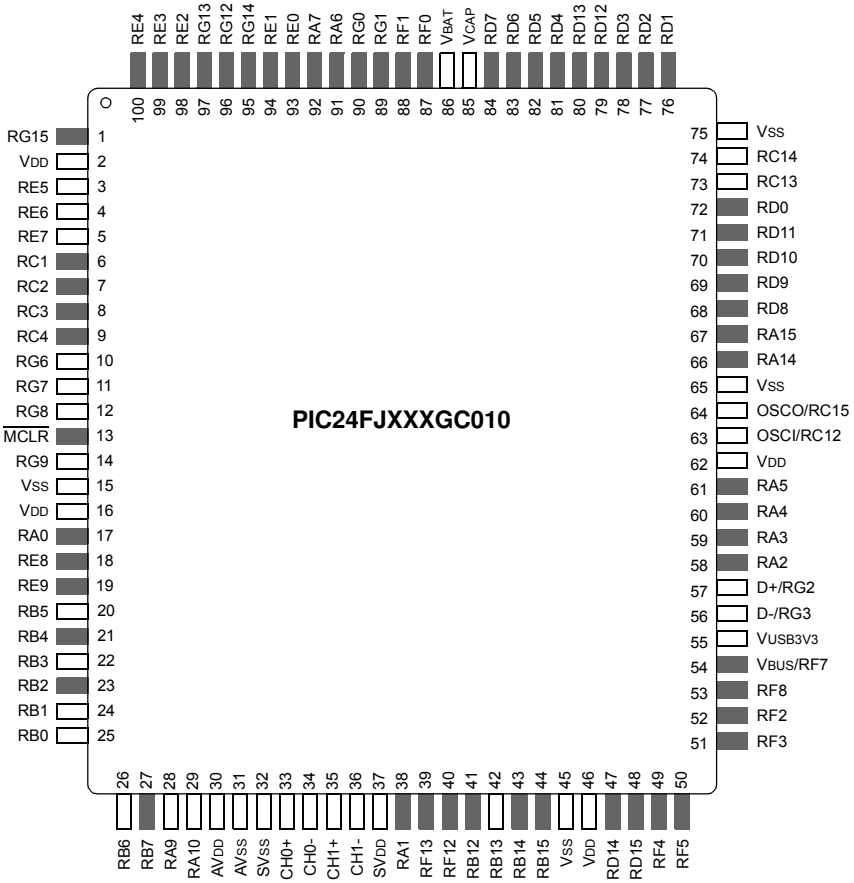
Pin	Function	Pin	Function
1	CTED4/PMD5/LCDBIAS2/CN63/RE5	33	AN30/SEG12/**RP16**/USBID/PMA12/CN71/RF3
2	PMD6/LCDBIAS1/CN64/RE6	34	VBUS/CN83
3	PMD7/LCDBIAS0/CN65/RE7	35	VUSB3V3
4	BGBUF2/AN17/OA1P1/C1IND/SEG0/**RP21**/T5CK/PMA5/CN8/RG6	36	D-/CN73/RG3
5	VLCAP1/AN18/OA1N4/C1INC/**RP26**/PMA4/CN9/RG7	37	D+/CN72/RG2
6	VLCAP2/AN19/OA1N3/C2IND/**RP19**/PMA3/CN10/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/CN23/RC12
8	AN49/OA1P0/C2INC/SEG1/DAC1/**RP27**/PMA2/CN11/RG9	40	OSCO/CLKO/CN22/RC15
9	VSS	41	VSS
10	VDD	42	AN40/SEG13/**RP2**/RTCC/DMLN/OCTRIG1/PMA13/CN53/RD8
11	PGEC3/AN5/OA1OUT/C1INA/SEG2/**RP18**/CN7/RB5	43	AN24/SEG14/**RP4**/SDA1/DPLN/PMACK2/CN54/RD9
12	PGED3/AN4/OA1N0/C1INB/SEG3/**RP28**/USBOEN/CN6/RB4	44	AN41/C3IND/SEG15/**RP3**/SCL1/PMA15/CS2/CN55/RD10
13	AN3/OA2OUT/C2INA/SEG4/VPIO/CN5/RB3	45	TMS/AN42/OA2P0/C3INC/SEG16/**RP12**/PMA14/CS1/CN56/RD11
14	AN2/OA2N2/CTCMP/C2INB/SEG5/**RP13**/T4CK/VMIO/CTED13/PMA7/CN4/RB2	46	AN43/OA2N0/SEG17/**RP11**/VCMPST3/DMH/INT0/CN49/RD0
15	PGEC1/CVREF-/AVREF-/AN1/OA2P1/SEG6/**RP1**/CTED12/CN3/RB1	47	SOSCI/RC13
16	PGED1/CVREF+/AVREF+/DVREF+/BGBUF1/AN0/SEG7/**RP0**/PMA6/CN2/RB0	48	PWRLCLK/SOSCO/**RPI37**/SCLKI/RC14
17	PGEC2/AN6/OA1P3/**RP6**/LCDBIAS3/CN24/RB6	49	AN35/SEG20/**RP24**/CN50/RD1(1)
18	PGED2/AN7/COM6/SEG30/**RP7**/CN25/RB7	50	AN25/OA2N1/SEG21/**RP23**/DPH/PMACK1/CN51/RD2
19	AVDD	51	AN44/OA2P4/SEG22/**RP22**/PMBE0/CN52/RD3
20	AVSS	52	AN47/OA1P4/SEG23/**RP25**/PMWR/CN13/RD4
21	SVSS	53	AN48/OA1N1/SEG24/**RP20**/PMRD/CN14/RD5
22	CH0+	54	AN34/OA1P2/C3INB/SEG25/CN15/RD6
23	CH0-	55	AN20/C3INA/SEG26/CN16/RD7
24	CH1+/SVREF+	56	VCAP
25	CH1-/CH1SE/SVREF-	57	VBAT
26	SVDD	58	COM7/SEG27/VCMPST1/CN68/RF0
27	TCK/AN12/COM5/SEG18/T1CK/CTED2/PMA11/CN30/RB12	59	COM4/SEG47/VCMPST2/CN69/RF1
28	TDI/AN13/OA2P3/SEG19/DAC2/CTED1/PMA10/CN31/RB13	60	COM3/PMD0/CN58/RE0
29	TDO/AN14/OA2N4/SEG8/**RP14**/CTED5/CTPLS/PMA1/CN32/RB14	61	COM2/PMD1/CN59/RE1
30	AN15/SEG9/**RP29**/T2CK/REFO/CTED6/PMA0/CN12/RB15	62	COM1/PMD2/CN60/RE2
31	AN11/OA2N3/SEG10/**RP10**/SDA2/T3CK/PMA9/CN17/RF4	63	COM0/CTED9/PMD3/CN61/RE3
32	CVREF/AN10/OA2P2/SEG11/**RP17**/SCL2/PMA8/CN18/RF5	64	HLVDIN/SEG62/CTED8/PMD4/CN62/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: RD1 is an analog pin and implements the AN35/SEG20/RP24/CN50/RD1 functions. However, there is not an ANSx bit associated with the RD1 port. Using the RD1 pin for the AN35 function would cause a worst-case increase in device current consumption of 500 µA.

Pin Diagrams (Continued)

100-Pin TQFP (12 mm x 12 mm)



Legend: Shaded pins indicate pins tolerant to up to +5.5 VDC. See Table 2 for a complete description of pin functions.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 100-PIN DEVICES

Pin	Function	Pin	Function
1	AN33/SEG50/CTED3/CN82/RG15	41	AN12/COM5/SEG18/T1CK/CTED2/PMA11/CN30/RB12
2	VDD	42	AN13/OA2P3/SEG19/DAC2/CTED1/PMA10/CN31/RB13
3	CTED4/PMD5/LCDBIAS2/CN63/RE5	43	AN14/OA2N4/SEG8/**RP14**/CTED5/CTPLS/PMA1/CN32/RB14
4	PMD6/LCDBIAS1/CN64/RE6	44	AN15/SEG9/**RP29**/T2CK/REFO/CTED6/PMA0/CN12/RB15
5	PMD7/LCDBIAS0/CN65/RE7	45	VSS
6	AN8/OA1N1/SEG32/**RPI38**/CN45/RC1	46	VDD
7	SEG51/**RPI39**/CN46/RC2	47	AN28/SEG38/**RPI43**/CN20/RD14
8	AN9/SEG33/**RPI40**/CN47/RC3	48	AN29/SEG39/**RP5**/CN21/RD15
9	AN16/SEG52/**RPI41**/PMCS2/CN48/RC4	49	AN11/OA2N3/SEG10/**RP10**/SDA2(3)/T3CK/PMA9/CN17/RF4
10	BGBUF2/AN17/OA1P1/C1IND/SEG0/**RP21**/T5CK/PMA5/CN8/RG6	50	CVREF/AN10/OA2P2/SEG11/**RP17**/SCL2(3)/PMA8/CN18/RF5
11	VLCAP1/AN18/OA1N4/C1INC/**RP26**/PMA4/CN9/RG7	51	AN30/SEG12/**RP16**/USBID/PMA12/CN71/RF3
12	VLCAP2/AN19/OA1N2/C2IND/**RP19**/PMA3/CN10/RG8	52	AN31/SEG40/**RP30**/CN70/RF2
13	$\overline{\text{MCLR}}$	53	AN32/SEG41/**RP15**/CN74/RF8
14	AN49/OA1P0/C2INC/SEG1/DAC1/**RP27**/PMA2/CN11/RG9	54	VBUS/CN83/RF7
15	VSS	55	VUSB3V3
16	VDD	56	D-/CN73/RG3
17	TMS/SEG48/CTED0/CN33/RA0	57	D+/CN72/RG2
18	SEG34/**RPI33**/PMCS1/CN66/RE8	58	SEG55/SCL2/CN35/RA2
19	AN21/SEG35/**RPI34**/PMA19/CN67/RE9	59	SEG56/SDA2/PMA20/CN36/RA3
20	PGEC3/AN5/OA1OUT/C1INA/SEG2/**RP18**/CN7/RB5	60	TDI/AN36/SEG29/PMA21/CN37/RA4
21	PGED3/AN4/OA1N0/C1INB/SEG3/**RP28**/USBOEN/CN6/RB4	61	TDO/AN37/SEG28/CN38/RA5
22	AN3/OA2OUT/C2INA/SEG4/VPIO/CN5/RB3	62	VDD
23	AN2/OA2N2/CTCMP/C2INB/SEG5/**RP13**/T4CK/VMIO/CTED13/CN4/RB2	63	OSCI/CLKI/CN23/RC12
24	PGEC1/CVREF-/AVREF-/AN1/OA2P1/SEG6/**RP1**/CTED12/CN3/RB1	64	OSCO/CLKO/CN22/RC15
25	PGED1/CVREF+/AVREF+/DVREF+/BGBUF1/AN0/SEG7/**RP0**/CN2/RB0	65	VSS
26	PGEC2/AN6/OA1P3/**RP6**/LCDBIAS3/CN24/RB6	66	AN38/SEG42/**RPI36**/SCL1/OCTRIG2/PMA22/CN43/RA14
27	PGED2/AN7/COM6/SEG30/**RP7**/CN25/RB7	67	AN39/SEG43/**RPI35**/SDA1/PMBE1/CN44/RA15
28	CVREF-(1)/AVREF-(2)/SEG36/PMA7/CN41/RA9	68	AN40/SEG13/**RP2**/RTCC/DMLN/OCTRIG1/PMA13/CN53/RD8
29	CVREF+(1)/AVREF+(2)/SEG37/PMA6/CN42/RA10	69	AN24/SEG14/**RP4**/DPLN/PMACK2/CN54/RD9
30	AVDD	70	AN41/C3IND/SEG15/**RP3**/PMA15/CS2/CN55/RD10
31	AVSS	71	AN42/OA2P0/C3INC/SEG16/**RP12**/PMA14/CS1/CN56/RD11
32	SVSS	72	AN43/OA2N0/SEG17/**RP11**/VCMPST3/DMH/INT0/CN49/RD0
33	CH0+	73	SOSCI/RC13
34	CH0-	74	PWRLCLK/SOSCO/SCLKI/**RPI37**/RC14
35	CH1+/SVREF+	75	VSS
36	CH1-/CH1SE/SVREF-	76	AN35/SEG20/**RP24**/CN50/RD1(4)
37	SVDD	77	AN25/OA2N1/SEG21/**RP23**/DPH/PMACK1/CN51/RD2
38	TCK/AN26/SEG31/CN34/RA1	78	AN44/OA2P4/SEG22/**RP22**/PMBE0/CN52/RD3
39	AN27/SEG53/**RP31**/CN76/RF13	79	AN45/SEG44/**RPI42**/PMD12/CN57/RD12
40	SEG54/**RPI32**/CTED7/PMA18/CN75/RF12	80	AN46/SEG45/PMD13/CN19/RD13

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: Alternate pin assignments for the external comparator voltage references as determined by the ALTCVREF Configuration bit.

2: Alternate pin assignments for the external A/D voltage references as determined by the ALTADREF Configuration bit.

3: Alternate pin assignments for I2C2 as determined by the $\overline{\text{I2C2SEL}}$ Configuration bit.

4: RD1 is an analog pin and implements the AN35/SEG20/RP24/CN50/RD1 functions. However, there is not an ANSx bit associated with the RD1 port. Using the RD1 pin for the AN35 function would cause a worst-case increase in device current consumption of 500 µA.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 100-PIN DEVICES (CONTINUED)

Pin	Function	Pin	Function
81	AN47/OA1P4/SEG23/**RP25**/PMWR/CN13/RD4	91	AN23/SEG57/CN39/RA6
82	AN48/OA1N1/SEG24/**RP20**/PMRD/CN14/RD5	92	AN22/SEG58/PMA17/CN40/RA7
83	AN34/OA1P2/C3INB/SEG25/PMD14/CN15/RD6	93	COM3/PMD0/CN58/RE0
84	AN20/C3INA/SEG26/PMD15/CN16/RD7	94	COM2/PMD1/CN59/RE1
85	VCAP	95	SEG59/CTED11/PMA16/CN81/RG14
86	VBAT	96	SEG60/CN79/RG12
87	COM7/SEG27/VCMPST1/PMD11/CN68/RF0	97	SEG61/CTED10/CN80/RG13
88	COM4/SEG47/VCMPST2/PMD10/CN69/RF1	98	COM1/PMD2/CN60/RE2
89	SEG46/PMD9/CN78/RG1	99	COM0/CTED9/PMD3/CN61/RE3
90	SEG49/PMD8/CN77/RG0	100	HLVDIN/SEG62/CTED8/PMD4/CN62/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: Alternate pin assignments for the external comparator voltage references as determined by the ALTCVREF Configuration bit.

2: Alternate pin assignments for the external A/D voltage references as determined by the ALTADREF Configuration bit.

3: Alternate pin assignments for I2C2 as determined by the $\overline{\text{I2C2SEL}}$ Configuration bit.

4: RD1 is an analog pin and implements the AN35/SEG20/RP24/CN50/RD1 functions. However, there is not an ANSx bit associated with the RD1 port. Using the RD1 pin for the AN35 function would cause a worst-case increase in device current consumption of 500 µA.

Pin Diagrams (Continued)

121-Pin BGA (10 mm x 10 mm, Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VBAT	N/C	RD12	RD2	RD1
B	N/C	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	N/C	RD7	RD4	N/C	RC13	RD11
D	RC1	RE7	RE5	N/C	N/C	N/C	RD6	RD13	RD0	N/C	RD10
E	RC4	RC3	RG6	RC2	N/C	RG1	N/C	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	N/C	N/C	VDD	OSCI/ RC12	VSS	OSCO/ RC15
G	RE8	RE9	RA0	N/C	VDD	VDD	VSS	N/C	RA5	RA3	RA4
H	RB5	RB4	N/C	N/C	CH0-	N/C	N/C	VBUS/ RF7	VUSB3V3	D+/RG2	RA2
J	RB3	RB2	RB7	AVDD	SVDD	RA1	RB12	N/C	N/C	RF8	D-/RG3
K	RB1	RB0	RA10	SVSS	CH1+	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	CH0+	CH1-	RF13	RB13	RB15	RD14	RF4	RF5

Legend: **Shaded balls** indicate pins tolerant to up to +5.5 VDC. See Table 3 for complete pinout descriptions.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 121-PIN DEVICES

Pin	Function	Pin	Function
A1	HLVDIN/SEG62/CTED8/PMD4/CN62/RE4	E1	AN16/SEG52/**RPI41**/PMCS2/CN48/RC4
A2	COM0/CTED9/PMD3/CN61/RE3	E2	AN9/OA1N2/SEG33/**RPI40**/CN47/RC3
A3	SEG61/CTED10/CN80/RG13	E3	BGBUF2/AN17/OA1P1/C1IND/SEG0/**RP21**/T5CK/PMA5/CN8/RG6
A4	COM3/PMD0/CN58/RE0	E4	SEG51/**RPI39**/CN46/RC2
A5	SEG49/PMD8/CN77/RG0	E5	N/C
A6	COM4/SEG47/VCMPST2/PMD10/CN69/RF1	E6	SEG46/PMD9/CN78/RG1
A7	VBAT	E7	N/C
A8	N/C	E8	AN39/SEG43/**RPI35**/SDA1/PMBE1/CN44/RA15
A9	AN45/SEG44/**RPI42**/PMD12/CN57/RD12	E9	AN40/SEG13/**RP2**/RTCC/DMLN/OCTRIG1/PMA13/CN53/RD8
A10	AN25/OA2N1/SEG21/**RP23**/DPH/PMACK1/CN51/RD2	E10	AN24/SEG14/**RP4**/DPLN/PMACK2/CN54/RD9
A11	AN35/SEG20/**RP24**/CN50/RD1	E11	AN38/SEG42/**RPI36**/SCL1/OCTRIG2/PMA22/CN43/RA14
B1	N/C	F1	$\overline{\text{MCLR}}$
B2	AN33/SEG50/CTED3/CN82/RG15	F2	VLCAP2/AN19/OA1N3/C2IND/**RP19**/PMA3/CN10/RG8
B3	COM1/PMD2/CN60/RE2	F3	AN49/C2INC/SEG1/DAC1/**RP27**/PMA2/CN11/RG9
B4	COM2/PMD1/CN59/RE1	F4	VLCAP1/AN18/OA1N4/C1INC/**RP26**/PMA4/CN9/RG7
B5	AN22/SEG58/PMA17/CN40/RA7	F5	VSS
B6	COM7/SEG27/VCMPST1/PMD11/CN68/RF0	F6	N/C
B7	VCAP	F7	N/C
B8	AN48/OA1N1/SEG24/**RP20**/PMRD/CN14/RD5	F8	VDD
B9	AN44/OA2P4/SEG22/**RP22**/PMBE0/CN52/RD3	F9	OSCI/CLKI/CN23/RC12
B10	VSS	F10	VSS
B11	PWRLCLK/SOSCO/SCLKI/**RPI37**/RC14	F11	OSCO/CLKO/CN22/RC15
C1	PMD6/LCDBIAS1/CN64/RE6	G1	SEG34/**RPI33**/PMCS1/CN66/RE8
C2	VDD	G2	AN21/SEG35/**RPI34**/PMA19/CN67/RE9
C3	SEG60/CN79/RG12	G3	TMS/SEG48/CTED0/CN33/RA0
C4	SEG59/CTED11/PMA16/CN81/RG14	G4	N/C
C5	AN23/SEG57/CN39/RA6	G5	VDD
C6	N/C	G6	VDD
C7	AN20/C3INA/SEG26/PMD15/CN16/RD7	G7	VSS
C8	AN47/OA1P4/SEG23/**RP25**/PMWR/CN13/RD4	G8	N/C
C9	N/C	G9	TDO/AN37/SEG28/CN38/RA5
C10	SOSCI/RC13	G10	SEG56/SDA2/PMA20/CN36/RA3
C11	AN42/OA2P0/C3INC/SEG16/**RP12**/PMA14/CS1/CN56/RD11	G11	TDI/AN36/SEG29/PMA21/CN37/RA4
D1	AN8/OA1N1/SEG32/**RPI38**/CN45/RC1	H1	PGEC3/AN5/OA1OUT/C1INA/SEG2/**RP18**/CN7/RB5
D2	PMD7/LCDBIAS0/CN65/RE7	H2	PGED3/AN4/OA1N0/C1INB/SEG3/**RP28**/USBOEN/CN6/RB4
D3	CTED4/PMD5/LCDBIAS2/CN63/RE5	H3	N/C
D4	N/C	H4	N/C
D5	N/C	H5	CH0-
D6	N/C	H6	N/C
D7	AN34/OA1P2/C3INB/SEG25/PMD14/CN15/RD6	H7	N/C
D8	AN46/SEG45/PMD13/CN19/RD13	H8	VBUS/CN83/RF7
D9	AN43/OA2N0/SEG17/**RP11**/VCMPST3/DMH/INT0/CN49/RD0	H9	VUSB3V3
D10	N/C	H10	D+/CN72/RG2
D11	AN41/C3IND/SEG15/**RP3**/PMA15/CS2/CN55/RD10	H11	SEG55/SCL2/CN35/RA2

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: Alternate pin assignments for the external comparator voltage references as determined by the ALTCVREF Configuration bit.

2: Alternate pin assignments for the external A/D voltage references as determined by the ALTADREF Configuration bit.

3: Alternate pin assignments for I2C2 as determined by the $\overline{\text{I2C2SEL}}$ Configuration bit.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 121-PIN DEVICES (CONTINUED)

Pin	Function	Pin	Function
J1	AN3/OA2OUT/C2INA/SEG4/VPIO/CN5/RB3	K7	AN14/OA2N4/SEG8/**RP14**/CTED5/CTPLS/PMA1/CN32/RB14
J2	AN2/OA2N2/CTCMP/C2INB/SEG5/**RP13**/T4CK/VMIO/ CTED13/CN4/RB2	K8	VDD
J3	PGED2/AN7/COM6/SEG30/**RP7**/CN25/RB7	K9	AN29/SEG39/**RP5**/CN21/RD15
J4	AVDD	K10	AN30/SEG12/**RP16**/USBID/PMA12/CN71/RF3
J5	SVDD	K11	AN31/SEG40/**RP30**/CN70/RF2
J6	TCK/AN26/SEG31/CN34/RA1	L1	PGEC2/AN6/OA1P3/**RP6**/LCDBIAS3/CN24/RB6
J7	AN12/COM5/SEG18/T1CK/CTED2/PMA11/CN30/RB12	L2	CVREF-(1)/AVREF-(2)/SEG36/PMA7/CN41/RA9
J8	N/C	L3	AVSS
J9	N/C	L4	CH0+
J10	AN32/SEG41/**RP15**/CN74/RF8	L5	CH1-/CH1SE/SVREF-
J11	D-/CN73/RG3	L6	AN27/SEG53/**RP31**/CN76/RF13
K1	PGEC1/CVREF-/AVREF-/AN1/OA2P1/SEG6/**RP1**/CTED12/ CN3/RB1	L7	AN13/OA2P3/SEG19/DAC2/CTED1/PMA10/CN31/RB13
K2	PGED1/CVREF+/AVREF+/DVREF+/BGBUF1/AN0/SEG7/**RP0**/ CN2/RB0	L8	AN15/SEG9/**RP29**/T2CK/REFO/CTED6/PMA0/CN12/RB15
K3	CVREF+(1)/AVREF+(2)/SEG37/PMA6/CN42/RA10	L9	AN28/SEG38/**RPI43**/CN20/RD14
K4	SVSS	L10	AN11/OA2N3/SEG10/**RP10**/SDA2(3)/T3CK/PMA9/CN17/RF4
K5	CH1+/SVREF+	L11	CVREF/AN10/OA2P2/SEG11/**RP17**/SCL2(3)/PMA8/CN18/RF5
K6	SEG54/**RPI32**/CTED7/PMA18/CN75/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: Alternate pin assignments for the external comparator voltage references as determined by the ALTCVREF Configuration bit.

2: Alternate pin assignments for the external A/D voltage references as determined by the ALTADREF Configuration bit.

3: Alternate pin assignments for I2C2 as determined by the $\overline{\text{I2C2SEL}}$ Configuration bit.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GC006
- PIC24FJ128GC006
- PIC24FJ64GC010
- PIC24FJ128GC010

The PIC24FJ128GC010 family expands the capabilities of the PIC24F family by adding a complete selection of advanced analog peripherals to its existing digital features. This combination, along with its ultra low-power features, Direct Memory Access (DMA) for peripherals, USB On-The-Go (OTG) and a built-in LCD controller and driver, makes this family the new standard for mixed-signal PIC® microcontrollers in one economical and power-saving package.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear Addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 XLP POWER-SAVING TECHNOLOGY

The PIC24FJ128GC010 family of devices introduces a greatly expanded range of power-saving operating modes for the ultimate in power conservation. The new modes include:

- Retention Sleep with essential circuits being powered from a separate low-voltage regulator
- Retention Deep Sleep, a lower power mode that maintains data RAM for fast start-up
- Deep Sleep without RTCC for the lowest possible power consumption under software control
- V_{BAT} mode (with or without RTCC) to continue limited operation from a backup battery when V_{DD} is removed

Many of these new low-power modes also support the continuous operation of the low-power, on-chip Real-Time Clock and Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from these new features, PIC24FJ128GC010 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving modes, for quick invocation of Idle and the many Sleep modes

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ128GC010 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- Two External Clock modes
- A Phase-Locked Loop (PLL) frequency multiplier, which allows clock speeds of up to 32 MHz
- A Fast Internal Oscillator (FRC) – nominal 8 MHz output, with multiple frequency divider options and automatic frequency self-calibration during run time
- A separate Low-Power Internal RC Oscillator (LPRC) – 31 kHz nominal, for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, while still selecting a Microchip device.

1.2 Advanced Analog Features

The centerpiece of the PIC24FJ128GC010 family is the advanced analog block. This feature set provides application developers with all the tools they need for single chip applications that demand high analog performance. Included in the advanced analog block are:

- A new 12-bit Pipeline A/D Converter (A/D) module. A major departure from previous PIC24F A/D Converters, this module offers up to 50 single-ended input channels (or up to 25 differential channel pairs) and conversion rates of up to ten million samples per second. It also provides a wider range of new features that allow the converter to assess and make decisions on incoming data without CPU intervention.
- A dual differential channel, Sigma-Delta A/D Converter, for applications requiring high-precision conversions (up to 16-bit resolution). The Sigma-Delta Converter also offers programmable gain on each channel pair and user-configurable data rate, between 244 samples per second and 62.5 ksps.
- Two independent, 10-bit Digital-to-Analog Converters (DACs), each capable of conversion rates up to one million samples per second.
- A comparator module with three analog comparators that are configurable for a wide range of operations. The comparators also have their own independent, configurable voltage reference.
- A dual operational amplifier module with multiple input options, selectable power modes, and rail-to-rail operation on the inputs and outputs. Each of the op amps can also be configured to function as a comparator, complete with interrupt generation.
- A dedicated, integrated band gap voltage reference for all analog modules, providing a range of on-chip reference voltages and two buffered reference outputs.
- Flexible multiplexing options for the entire analog block, allowing for the convenient sharing of signals between the analog modules.

1.3 DMA Controller

PIC24FJ128GC010 family devices also add a Direct Memory Access (DMA) controller to the existing PIC24F architecture. The DMA acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput, and decreasing execution time overhead. Six independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.4 USB On-The-Go (OTG)

USB On-The-Go provides on-chip functionality as a target device compatible with the USB 2.0 standard, as well as limited stand-alone functionality as a USB embedded host. By implementing the USB Host Negotiation Protocol (HNP), the module can also dynamically switch between device and host operation, allowing for a much wider range of versatile USB-enabled applications on a microcontroller platform.

PIC24FJ128GC010 family devices also incorporate an integrated USB transceiver and precision oscillator, minimizing the required complexity of implementing a complete USB device, embedded host, dual role or On-The-Go application.

1.5 LCD Controller

With the PIC24FJ128GC010 family of devices, Microchip introduces its versatile Liquid Crystal Display (LCD) controller and driver to the PIC24F family. The on-chip LCD driver includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump and an integrated internal resistor ladder that allows contrast control in software, and display operation above device V_{DD}.

1.6 Other Special Features

- **Peripheral Pin Select (PPS):** The Peripheral Pin Select feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ128GC010 family incorporates several different serial communication peripherals to handle a range of application requirements. There are two independent I^2C modules that support both Master and Slave modes of operation. Devices also have, through the PPS feature, four independent UARTs with built-in IrDA® encoders/decoders and two SPI modules.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ128GC010 family include the CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits, and address widths of up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- **Data Signal Modulator (DSM):** The Data Signal Modulator (DSM) allows the user to mix a digital data stream (the “modulator signal”) with a carrier signal to produce a modulated output.

1.7 Details on Individual Family Members

Devices in the PIC24FJ128GC010 family are available in 64-pin and 100/121-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in six ways:

1. Flash program memory (64 Kbytes for PIC24FJ64GC0XX devices and 128 Kbytes for PIC24FJ128GC0XX devices).
2. Available I/O pins and ports (53 pins on 6 ports for 64-pin devices and 85 pins on 7 ports for 100/121-pin devices).
3. Available Interrupt-on-Change Notification (ICN) inputs (52 on 64-pin devices and 82 on 100/121-pin devices).
4. Available remappable pins (29 pins on 64-pin devices and 44 pins on 100/121-pin devices).
5. Maximum available drivable LCD pixels (248 for 64-pin devices and 472 on 100/121-pin devices.)
6. Analog input channels for the Pipeline A/D Converter (29 channels for 64-pin devices and 50 channels for 100/121-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

A list of pin features available on the PIC24FJ128GC010 family devices, sorted by function, is shown in Table 1-3. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GC010 FAMILY: 64-PIN DEVICES

Features	PIC24FJ64GC006	PIC24FJ128GC006
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	65 (61/4)	
I/O Ports	Ports B, C, D, E, F, G	
Total I/O Pins	53	
Remappable Pins	30 (29 I/Os, 1 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture w/Timer Channels	9(1)	
Output Compare/PWM Channels	9(1)	
Input Change Notification Interrupt	52	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12-Bit Pipeline Analog-to-Digital Converter (A/D) (input channels)	29	
Sigma-Delta Analog-to-Digital Converter (A/D) (differential channels)	2	
Digital-to-Analog Converter (DAC)	2	
Operational Amplifiers	2	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	196 (28 SEG x 7 COM)	
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	64-Pin TQFP and QFN	

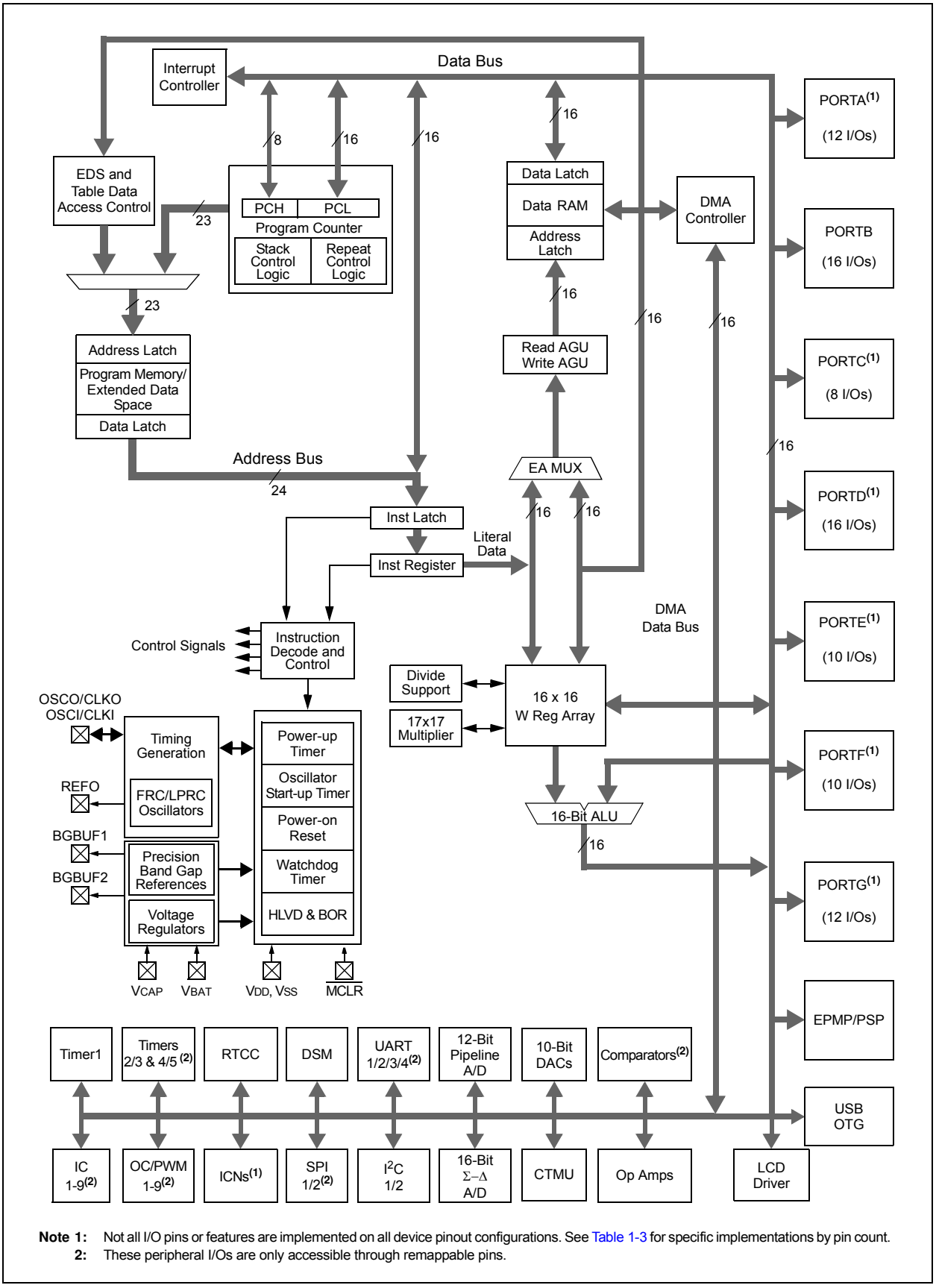
Note 1: Peripherals are accessible through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ128GC010 FAMILY: 100/121-PIN DEVICES

Features	PIC24FJ64GC010	PIC24FJ128GC010
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	66 (62/4)	
I/O Ports	Ports A, B, C, D, E, F, G	
Total I/O Pins	85	
Remappable Pins	44 (32 I/Os, 12 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture w/Timer Channels	9(1)	
Output Compare/PWM Channels	9(1)	
Input Change Notification Interrupt	82	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12-Bit Pipeline Analog-to-Digital Converter (A/D) (input channels)	50	
Sigma-Delta Analog-to-Digital Converter (A/D) (differential channels)	2	
Digital-to-Analog Converter (DAC)	2	
Operational Amplifiers	2	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	472 (59 SEG x 8 COM)	
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	100-Pin TQFP and 121-Pin BGA	

Note 1: Peripherals are accessible through remappable pins.

FIGURE 1-1: PIC24FJ128GC010 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-3 for specific implementations by pin count.
2: These peripheral I/Os are only accessible through remappable pins.

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
AN0	16	25	K2	I	ANA	12-Bit Pipeline A/D Converter Inputs.
AN1	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	—	6	D1	I	ANA	
AN9	—	8	E2	I	ANA	
AN10	32	50	L11	I	ANA	
AN11	31	49	L10	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	4	10	E3	I	ANA	
AN18	5	11	F4	I	ANA	
AN19	6	12	F2	I	ANA	
AN20	55	84	C7	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	B5	I	ANA	
AN23	—	91	C5	I	ANA	
AN24	43	69	E10	I	ANA	
AN25	50	77	A10	I	ANA	
AN26	—	38	J6	I	ANA	
AN27	—	39	L6	I	ANA	
AN28	—	47	L9	I	ANA	
AN29	—	48	K9	I	ANA	
AN30	33	51	K10	I	ANA	
AN31	—	52	K11	I	ANA	
AN32	—	53	J10	I	ANA	
AN33	—	1	B2	I	ANA	
AN34	54	83	D7	I	ANA	
AN35	49	76	A11	I	ANA	
AN36	—	60	G11	I	ANA	
AN37	—	61	G9	I	ANA	
AN38	—	66	E11	I	ANA	
AN39	—	67	E8	I	ANA	
AN40	42	68	E9	I	ANA	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
AN41	44	70	D11	I	ANA	12-Bit Pipeline A/D Converter Inputs.
AN42	45	71	C11	I	ANA	
AN43	46	72	D9	I	ANA	
AN44	51	78	B9	I	ANA	
AN45	—	79	A9	I	ANA	
AN46	—	80	D8	I	ANA	
AN47	52	81	C8	I	ANA	
AN48	53	82	B8	I	ANA	
AN49	8	14	F3	I	ANA	
AVDD	19	30	J4	P	—	Positive Supply for Analog modules.
AVREF+	16	25, 29	K2, K3	I	ANA	Pipeline A/D Reference Voltage (high) Input.
AVREF-	15	24, 28	K1, L2	I	ANA	Pipeline A/D Reference Voltage (low) Input.
AVss	20	31	L3	P	—	Ground Reference for Analog modules.
BGBUF1	16	25	K2	O	—	Buffered Band Gap Reference 1 Voltage Output.
BGBUF2	4	10	E3	O	—	Buffered Band Gap Reference 2 Voltage Output.
C1INA	11	20	H1	I	ANA	Comparator 1 Input A.
C1INB	12	21	H2	I	ANA	Comparator 1 Input B.
C1INC	5	11	F4	I	ANA	Comparator 1 Input C.
C1IND	4	10	E3	I	ANA	Comparator 1 Input D.
C2INA	13	22	J1	I	ANA	Comparator 2 Input A.
C2INB	14	23	J2	I	ANA	Comparator 2 Input B.
C2INC	8	14	F3	I	ANA	Comparator 2 Input C.
C2IND	6	12	F2	I	ANA	Comparator 2 Input D.
C3INA	55	84	C7	I	ANA	Comparator 3 Input A.
C3INB	54	83	D7	I	ANA	Comparator 3 Input B.
C3INC	45	71	C11	I	ANA	Comparator 3 Input C.
C3IND	44	70	D11	I	ANA	Comparator 3 Input D.
CH0+	22	33	L4	I	ANA	Sigma-Delta A/D Converter Channel 0 Non-Inverting Analog Input.
CH0-	23	34	H5	I	ANA	Sigma-Delta A/D Converter Channel 0 Inverting Analog Input.
CH1+	24	35	K5	I	ANA	Sigma-Delta A/D Converter Channel 1 Non-Inverting Analog Input.
CH1-	25	36	L5	I	ANA	Sigma-Delta A/D Converter Channel 1 Inverting Analog Input.
CH1SE	25	36	L5	I	ANA	Sigma-Delta A/D Converter Single-Ended Channel 1 Analog Input.
CLKI	39	63	F9	I	ANA	Main Clock Input Connection.
CLKO	40	64	F11	O	—	System Clock Output.

Legend: TTL = TTL input buffer ANA = Analog level input/output ST = Schmitt Trigger input buffer I^2C = I^2C/SMBus input buffer

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
CN2	16	25	K2	I	ST	Interrupt-on-Change Inputs.
CN3	15	24	K1	I	ST	
CN4	14	23	J2	I	ST	
CN5	13	22	J1	I	ST	
CN6	12	21	H2	I	ST	
CN7	11	20	H1	I	ST	
CN8	4	10	E3	I	ST	
CN9	5	11	F4	I	ST	
CN10	6	12	F2	I	ST	
CN11	8	14	F3	I	ST	
CN12	30	44	L8	I	ST	
CN13	52	81	C8	I	ST	
CN14	53	82	B8	I	ST	
CN15	54	83	D7	I	ST	
CN16	55	84	C7	I	ST	
CN17	31	49	L10	I	ST	
CN18	32	50	L11	I	ST	
CN19	—	80	D8	I	ST	
CN20	—	47	L9	I	ST	
CN21	—	48	K9	I	ST	
CN22	40	64	F11	I	ST	
CN23	39	63	F9	I	ST	
CN24	17	26	L1	I	ST	
CN25	18	27	J3	I	ST	
CN30	27	41	J7	I	ST	
CN31	28	42	L7	I	ST	
CN32	29	43	K7	I	ST	
CN33	—	17	G3	I	ST	
CN34	—	38	J6	I	ST	
CN35	—	58	H11	I	ST	
CN36	—	59	G10	I	ST	
CN37	—	60	G11	I	ST	
CN38	—	61	G9	I	ST	
CN39	—	91	C5	I	ST	
CN40	—	92	B5	I	ST	
CN41	—	28	L2	I	ST	
CN42	—	29	K3	I	ST	
CN43	—	66	E11	I	ST	
CN44	—	67	E8	I	ST	
CN45	—	6	D1	I	ST	
CN46	—	7	E4	I	ST	
CN47	—	8	L11	I	ST	
CN48	—	9	E1	I	ST	
CN49	46	72	D9	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
CN50	49	76	A11	I	ST	Interrupt-on-Change Inputs.
CN51	50	77	A10	I	ST	
CN52	51	78	B9	I	ST	
CN53	42	68	E9	I	ST	
CN54	43	69	E10	I	ST	
CN55	44	70	D11	I	ST	
CN56	45	71	C11	I	ST	
CN57	—	79	A9	I	ST	
CN58	60	93	A4	I	ST	
CN59	61	94	B4	I	ST	
CN60	62	98	B3	I	ST	
CN61	63	99	A2	I	ST	
CN62	64	100	A1	I	ST	
CN63	1	3	D3	I	ST	
CN64	2	4	C1	I	ST	
CN65	3	5	D2	I	ST	
CN66	—	18	G1	I	ST	
CN67	—	19	G2	I	ST	
CN68	58	87	B6	I	ST	
CN69	59	88	A6	I	ST	
CN70	—	52	K11	I	ST	
CN71	33	51	K10	I	ST	
CN72	37	57	H10	I	ST	
CN73	36	56	J11	I	ST	
CN74	—	53	J10	I	ST	
CN75	—	40	K6	I	ST	
CN76	—	39	L6	I	ST	
CN77	—	90	A5	I	ST	
CN78	—	89	E6	I	ST	
CN79	—	96	C3	I	ST	
CN80	—	97	A3	I	ST	
CN81	—	95	C4	I	ST	
CN82	—	1	B2	I	ST	
CN83	34	54	H8	I	ST	
COM0	63	99	A2	O	—	LCD Driver Common Outputs.
COM1	62	98	B3	O	—	
COM2	61	94	B4	O	—	
COM3	60	93	A4	O	—	
COM4	59	88	A6	O	—	
COM5	27	41	J7	O	—	
COM6	18	27	J3	O	—	
COM7	58	87	B6	O	—	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C = I^2C/SMBus input buffer

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
CS1	45	71	C11	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe (shared with PMA14).
CS2	44	70	D11	O	—	Parallel Master Port Chip Select 2 Strobe (shared with PMA15).
CTCMP	14	23	J2	I	ANA	CTMU Comparator 2 Input (Pulse mode).
CTED0	—	17	G3	I	ST	CTMU External Edge Inputs.
CTED1	28	42	L7	I	ST	
CTED2	27	41	J7	I	ST	
CTED3	—	1	B2	I	ST	
CTED4	1	3	D3	I	ST	
CTED5	29	43	K7	I	ST	
CTED6	30	44	L8	I	ST	
CTED7	—	40	K6	I	ST	
CTED8	64	100	A1	I	ST	
CTED9	63	99	A2	I	ST	
CTED10	—	97	A3	I	ST	
CTED11	—	95	C4	I	ST	
CTED12	15	24	K1	I	ST	
CTED13	14	23	J2	I	ST	
CTPLS	29	43	K7	O	—	CTMU Pulse Output.
CV_{REF}	32	50	L11	O	—	Comparator Voltage Reference Output.
CV_{REF+}	16	25, 29	K2, K3	I	ANA	Comparator Reference Voltage (high) Input.
CV_{REF-}	15	24, 28	K1, L2	I	ANA	Comparator Reference Voltage (low) Input.
D+	37	57	H10	I/O	—	USB Differential Plus Line (internal transceiver).
D-	36	56	J11	I/O	—	USB Differential Minus Line (internal transceiver).
DAC1	8	14	F3	O	—	DAC Converter 1 Analog Output.
DAC2	28	42	L7	O	—	DAC Converter 2 Analog Output.
DMH	46	72	D9	O	—	D- External Pull-up Control Output.
DMLN	42	68	E9	O	—	D- External Pull-Down Control Output.
DPH	50	77	A10	O	—	D+ External Pull-up Control Output.
DPLN	43	69	E10	O	—	D+ External Pull-Down Control Output.
DV_{REF+}	16	25	K2	I	ANA	DAC Positive Reference Input.
INT0	46	72	D9	I	ST	External Interrupt Input 0.
LCDBIAS0	3	5	D2	I	ANA	Bias Inputs for LCD Driver Charge Pump.
LCDBIAS1	2	4	C1	I	ANA	
LCDBIAS2	1	3	D3	I	ANA	
LCDBIAS3	17	26	L1	I	ANA	
HLVDIN	64	100	A1	I	ANA	High/Low-Voltage Detect Input.
$\overline{MCLR}$	7	13	F1	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OCTRIG1	42	68	E9	I	ST	Output Compare External Trigger 1 Input.
OCTRIG2	—	66	E11	I	ST	Output Compare External Trigger 2 Input.

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C = I^2C/SMBus input buffer

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
OA1N0	12	21	H2	I	ANA	Op Amp 1 Negative (inverting) Inputs.
OA1N1	53	82	B8	I	ANA	
OA1N2	—	8	E2	I	ANA	
OA1N3	6	12	F2	I	ANA	
OA1N4	5	11	F4	I	ANA	
OA1OUT	11	20	H1	O	—	Op Amp 1 (analog) Output (digital output in Comparator mode).
OA1P0	8	14	F3	I	ANA	Op Amp 1 Positive (non-inverting) Inputs.
OA1P1	4	10	E3	I	ANA	
OA1P2	54	83	D7	I	ANA	
OA1P3	17	26	L1	I	ANA	
OA1P4	52	81	C8	I	ANA	
OA2N0	46	72	D9	I	ANA	Op Amp 2 Negative (inverting) Inputs.
OA2N1	50	77	A10	I	ANA	
OA2N2	14	23	J2	I	ANA	
OA2N3	31	49	L10	I	ANA	
OA2N4	29	43	K7	I	ANA	
OA2OUT	13	22	J1	O	—	Op Amp 2 (analog) Output (digital output in Comparator mode).
OA2P0	45	71	C11	I	ANA	Op Amp 2 Positive (non-inverting) Inputs.
OA2P1	15	24	K1	I	ANA	
OA2P2	32	50	L11	I	ANA	
OA2P3	28	42	L7	I	ANA	
OA2P4	51	78	B9	I	ANA	
OSCI	39	63	F9	I	ANA	Main Oscillator Input Connection.
OSCO	40	64	F11	O	—	Main Oscillator Output Connection.
PGEC1	15	24	K1	I/O	ST	In-Circuit Debugger/Emulator/ICSP™ Programming Clock.
PGEC2	17	26	L1	I/O	ST	
PGEC3	11	20	H1	I/O	ST	
PGED1	16	25	K2	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data.
PGED2	18	27	J3	I/O	ST	
PGED3	12	21	H2	I/O	ST	
PMA0	30	44	L8	I/O	ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	43	K7	I/O	ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	14	F3	O	—	Parallel Master Port Address (bits<22:2>).
PMA3	6	12	F2	O	—	
PMA4	5	11	F4	O	—	
PMA5	4	10	E3	O	—	
PMA6	16	29	K3	O	—	
PMA7	14	28	L2	O	—	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C = I^2C/SMBus input buffer

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
PMA8	32	50	L11	O	—	Parallel Master Port Address (bits<22:2>).
PMA9	31	49	L10	O	—	
PMA10	28	42	L7	O	—	
PMA11	27	41	J7	O	—	
PMA12	33	51	K10	O	—	
PMA13	42	68	E9	O	—	
PMA14	45	71	C11	O	—	
PMA15	44	70	D11	O	—	
PMA16	—	95	C4	O	—	
PMA17	—	92	B5	O	—	
PMA18	—	40	K6	O	—	
PMA19	—	19	G2	O	—	
PMA20	—	59	G10	O	—	
PMA21	—	60	G11	O	—	
PMA22	—	66	E11	O	—	
PMACK1	50	77	A10	I	ST/TTL	Parallel Master Port Acknowledge Input 1.
PMACK2	43	69	E10	I	ST/TTL	Parallel Master Port Acknowledge Input 2.
PMBE0	51	78	B9	O	—	Parallel Master Port Byte Enable 0 Strobe.
PMBE1	—	67	E8	O	—	Parallel Master Port Byte Enable 1 Strobe.
PMCS1	—	18	G1	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe.
PMCS2	—	9	K10	O	—	Parallel Master Port Chip Select 2 Strobe.
PMD0	60	93	A4	I/O	ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	94	B4	I/O	ST/TTL	
PMD2	62	98	B3	I/O	ST/TTL	
PMD3	63	99	A2	I/O	ST/TTL	
PMD4	64	100	A1	I/O	ST/TTL	
PMD5	1	3	D3	I/O	ST/TTL	
PMD6	2	4	C1	I/O	ST/TTL	
PMD7	3	5	D2	I/O	ST/TTL	
PMD8	—	90	A5	I/O	ST/TTL	
PMD9	—	89	E6	I/O	ST/TTL	
PMD10	—	88	A6	I/O	ST/TTL	
PMD11	—	87	B6	I/O	ST/TTL	
PMD12	—	79	A9	I/O	ST/TTL	
PMD13	—	80	D8	I/O	ST/TTL	
PMD14	—	83	D7	I/O	ST/TTL	
PMD15	—	84	C7	I/O	ST/TTL	
PMRD	53	82	B8	O	—	Parallel Master Port Read Strobe.
PMWR	52	81	C8	O	—	Parallel Master Port Write Strobe.
PWRLCLK	48	74	B11	I	ST/TTL	Power Line (50 Hz/60 Hz) External Clock Input for RTCC.

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C = I^2C/SMBus input buffer