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PIC24FJ256GA705 FAMILY

16-Bit General Purpose Microcontrollers with 256-Kbyte Flash and 16-Kbyte RAM in Low Pin Count Packages

High-Performance CPU

- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Fast RC Internal Oscillator:
  - 96 MHz PLL option
  - Multiple clock divide options
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16-Bit x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory
- Six-Channel DMA Controller

Analog Features

- Up to 14-Channel, Software Selectable, 10/12-Bit Analog-to-Digital Converter:
  - 12-bit, 200K samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Charge pump for operating at lower AV_{DD}
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Three Analog Comparators with Input Multiplexing:
  - Programmable reference voltage for comparators
- LVD Interrupt Above/Below Programmable V_{LVD} Level
- Charge Time Measurement Unit (CTMU):
  - Allows measurement of capacitance and time
  - Operational in Sleep

Low-Power Features

- Sleep and Idle modes Selectively Shut Down Peripherals and/or Core for Substantial Power Reduction and Fast Wake-up
- Doze mode allows CPU to Run at a Lower Clock Speed than Peripherals
- Alternate Clock modes allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction

Special Microcontroller Features

- Supply Voltage Range of 2.0V to 3.6V
- Dual Voltage Regulators:
  - 1.8V core regulator
  - 1.2V regulator for Retention Sleep mode
- Operating Ambient Temperature Range of -40°C to +85°C
- ECC Flash Memory (256 Kbytes):
  - Single Error Correction (SEC)
  - Double Error Detection (DED)
  - 10,000 erase/write cycle endurance, typical
  - Data retention: 20 years minimum
  - Self-programmable under software control
- 16-Kbyte SRAM
- Programmable Reference Clock Output
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via 2 Pins
- JTAG Boundary Scan Support
- Fail-Safe Clock Monitor Operation:
  - Detects clock failure and switches to on-chip, Low-Power RC (LPRC) Oscillator
- Power-on Reset (POR), Brown-out Reset (BOR) and Oscillator Start-up Timer (OST)
- Programmable Low-Voltage Detect (LVD)
- Flexible Watchdog Timer (WDT) with its Own RC Oscillator for Reliable Operation

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Peripheral Features

- High-Current Sink/Source 18 mA/18 mA on All I/O Pins
- Independent, Low-Power 32 kHz Timer Oscillator
- Timer1: 16-Bit Timer/Counter with External Crystal Oscillator; Timer1 can Provide an A/D Trigger
- Timer2,3: 16-Bit Timer/Counter, can Create 32-Bit Timer; Timer3 can Provide an A/D Trigger
- Three Input Capture modules, Each with a 16-Bit Timer
- Three Output Compare/PWM modules, Each with a 16-Bit Timer
- Four MCCP modules, Each with a Dedicated 16/32-Bit Timer:
  - One 6-output MCCP module
  - Three 2-output MCCP modules
- Three Variable Width, Synchronous Peripheral Interface (SPI) Ports on All Devices; 3 Operation modes:
  - 3-wire SPI (supports all 4 SPI modes)
  - 8 by 16-bit or 8 by 8-bit FIFO
  - I^2S mode
- Two I^2C Master and Slave w/Address Masking, and IPMI Support
- Two UART modules:
  - LIN/J2602 bus support (auto-wake-up, Auto-Baud Detect (ABD), Break character support)
  - RS-232 and RS-485 support
  - IrDA® mode (hardware encoder/decoder functions)
- Five External Interrupt Pins
- Parallel Master Port/Enhanced Parallel Slave Port (PMP/EPSP), 8-Bit Data with External Programmable Control (polarity and protocol)
- Enhanced CRC module
- Reference Clock Output with Programmable Divider
- Two Configurable Logic Cell (CLC) Blocks:
  - Two inputs and one output, all mappable to peripherals or I/O pins
  - AND/OR/XOR logic and D/JK flip-flop functions
- Peripheral Pin Select (PPS) with Independent I/O Mapping of Many Peripherals

Device	Memory		Pins	GPIO	DMA Channels	Peripherals													JTAG
	Program (bytes)	SRAM (bytes)				10/12-Bit A/D Channels	Comparators	CRC	MCCP 6-Output/2-Output	IC/OC PWM	16-Bit Timers	I^2C	Variable Width SPI	LIN-USART/IrDA®	CTMU Channels	EPMP (Address/Data Line)	CLC	RTCC	
PIC24FJ64GA705	64K	16K	48	40	6	14	3	Yes	1/3	3/3	3	2	3	2	13	10/8	2	Yes	Yes
PIC24FJ128GA705	128K	16K	48	40	6	14	3	Yes	1/3	3/3	3	2	3	2	13	10/8	2	Yes	Yes
PIC24FJ256GA705	256K	16K	48	40	6	14	3	Yes	1/3	3/3	3	2	3	2	13	10/8	2	Yes	Yes
PIC24FJ64GA704	64K	16K	44	36	6	14	3	Yes	1/3	3/3	3	2	3	2	13	10/8	2	Yes	Yes
PIC24FJ128GA704	128K	16K	44	36	6	14	3	Yes	1/3	3/3	3	2	3	2	13	10/8	2	Yes	Yes
PIC24FJ256GA704	256K	16K	44	36	6	14	3	Yes	1/3	3/3	3	2	3	2	13	10/8	2	Yes	Yes
PIC24FJ64GA702	64K	16K	28	22	6	10	3	Yes	1/3	3/3	3	2	3	2	12	No	2	Yes	Yes
PIC24FJ128GA702	128K	16K	28	22	6	10	3	Yes	1/3	3/3	3	2	3	2	12	No	2	Yes	Yes
PIC24FJ256GA702	256K	16K	28	22	6	10	3	Yes	1/3	3/3	3	2	3	2	12	No	2	Yes	Yes

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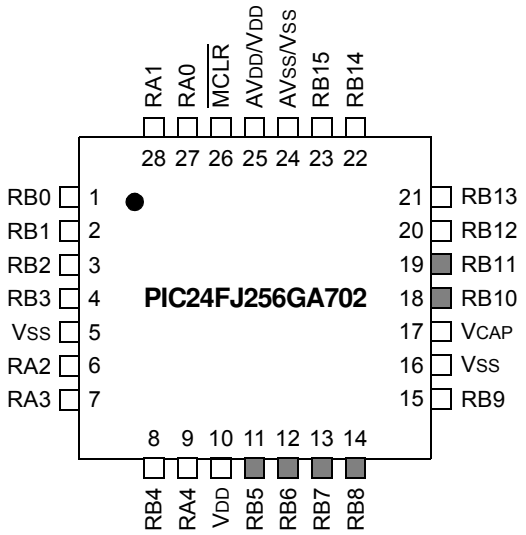
Pin Diagrams (PIC24FJ256GA702 Devices)

28-Pin QFN, UQFN



Legend: See Table 1 for a complete description of pin functions. Pinouts are subject to change.

Note: Gray shading indicates 5.5V tolerant input pins.

TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJ256GA702 QFN, UQFN)

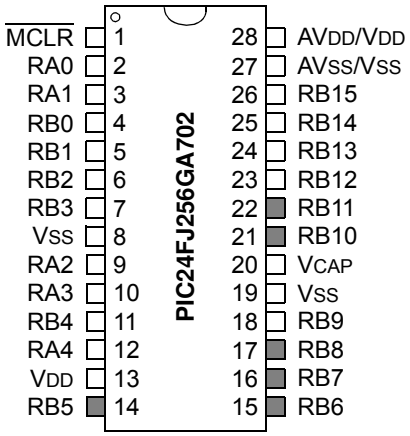
Pin	Function	Pin	Function
1	PGD1/AN2/CTCMP/C2INB/**RP0**/RB0	15	TDO/C1INC/C2INC/C3INC/$\overline{\text{TMPRN}}$/**RP9**/SDA1/T1CK/CTED4/RB9
2	PGC1/AN1-/AN3/C2INA/**RP1**/CTED12/RB1	16	Vss
3	AN4/C1INB/**RP2**/SDA2/CTED13/RB2	17	VCAP
4	AN5/C1INA/**RP3**/SCL2/CTED8/RB3	18	PGD2/TDI/**RP10**/OCM1C/CTED11/RB10
5	Vss	19	PGC2/TMS/REFI1/**RP11**/CTED9/RB11
6	OSCI/CLKI/C1IND/RA2	20	AN8/LVDIN/**RP12**/RB12
7	OSCO/CLKO/C2IND/RA3	21	AN7/C1INC/**RP13**/OCM1D/CTPLS/RB13
8	SOSCI/**RP4**/RB4	22	CVREF/AN6/C3INB/**RP14**/CTED5/RB14
9	SOSCO/PWRLCLK/RA4	23	AN9/C3INA/**RP15**/CTED6/RB15
10	VDD	24	AVSS/VSS
11	PGD3/**RP5**/ASDA1/OCM1E/RB5	25	AVDD/VDD
12	PGC3/**RP6**/ASCL1/OCM1F/RB6	26	$\overline{\text{MCLR}}$
13	**RP7**/OCM1A/CTED3/INT0/RB7	27	VREF+/CVREF+/AN0/C3INC/**RP26**/CTED1/RA0
14	TCK/**RP8**/SCL1/OCM1B/CTED10/RB8	28	VREF-/CVREF-/AN1/C3IND/**RP27**/CTED2/RA1

Legend: **RPn** represents remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams (PIC24FJ256GA702 Devices)

28-Pin SOIC, SSOP, SPDIP



Legend: See Table 2 for a complete description of pin functions. Pinouts are subject to change.

Note: Gray shading indicates 5.5V tolerant input pins.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJ256GA702 SOIC, SSOP, SPDIP)

Pin	Function	Pin	Function
1	MCLR	15	PGC3/**RP6**/ASCL1/OCM1F/RB6
2	VREF+/CVREF+/AN0/C3INC/**RP26**/CTED1/RA0	16	**RP7**/OCM1A/CTED3/INT0/RB7
3	VREF-/CVREF-/AN1/C3IND/**RP27**/CTED2/RA1	17	TCK/**RP8**/SCL1/OCM1B/CTED10/RB8
4	PGD1/AN2/CTCMP/C2INB/**RP0**/RB0	18	TDO/C1INC/C2INC/C3INC/TMPRN/**RP9**/SDA1/T1CK/CTED4/RB9
5	PGC1/AN1-/AN3/C2INA/**RP1**/CTED12/RB1	19	VSS
6	AN4/C1INB/**RP2**/SDA2/CTED13/RB2	20	VCAP
7	AN5/C1INA/**RP3**/SCL2/CTED8/RB3	21	PGD2/TDI/**RP10**/OCM1C/CTED11/RB10
8	VSS	22	PGC2/TMS/REFI1/**RP11**/CTED9/RB11
9	OSCI/CLKI/C1IND/RA2	23	AN8/LVDIN/**RP12**/RB12
10	OSCO/CLKO/C2IND/RA3	24	AN7/C1INC/**RP13**/OCM1D/CTPLS/RB13
11	SOSCI/**RP4**/RB4	25	CVREF/AN6/C3INB/**RP14**/CTED5/RB14
12	SOSCO/PWRLCLK/RA4	26	AN9/C3INA/**RP15**/CTED6/RB15
13	VDD	27	AVSS/VSS
14	PGD3/**RP5**/ASDA1/OCM1E/RB5	28	AVDD/VDD

Legend: **RPn** represents remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

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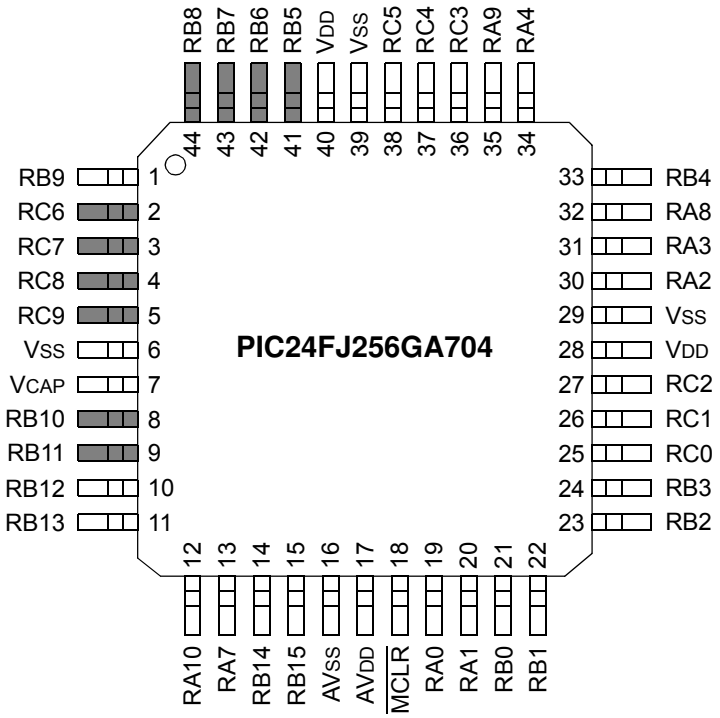
Pin Diagrams (PIC24FJ256GA704 Devices)

44-Pin TQFP



Legend: See Table 3 for a complete description of pin functions. Pinouts are subject to change.

Note: Gray shading indicates 5.5V tolerant input pins.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJ256GA704 TQFP)

Pin	Function	Pin	Function
1	C1INC/C2INC/C3INC/$\overline{\text{TMPRN}}$/**RP9**/SDA1/T1CK/CTED4/PMD3/RB9	23	AN4/C1INB/**RP2**/SDA2/CTED13/RB2
2	**RP22**/PMA1/PMALH/RC6	24	AN5/C1INA/**RP3**/SCL2/CTED8/RB3
3	**RP23**/PMA0/PMALL/RC7	25	AN10/**RP16**/PMBE1/RC0
4	**RP24**/PMA5/RC8	26	AN11/**RP17**/PMA15/PMCS2/RC1
5	**RP25**/CTED7/PMA6/RC9	27	AN12/**RP18**/PMACK1/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGD2/**RP10**/OCM1C/CTED11/PMD2/RB10	30	OSCI/CLKI/C1IND/RA2
9	PGC2/REFI1/**RP11**/CTED9/PMD1/RB11	31	OSCO/CLKO/C2IND/RA3
10	AN8/LVDIN/**RP12**/PMD0/RB12	32	TDO/PMA8/RA8
11	AN7/C1INC/**RP13**/OCM1D/CTPLS/PMRD/$\overline{\text{PMWR}}$/RB13	33	SOSCI/**RP4**/RB4
12	TMS/**RP28**/PMA2/PMALU/RA10	34	SOSCO/PWRLCLK/RA4
13	TCK/PMA7/RA7	35	TDI/PMA9/RA9
14	CVREF/AN6/C3INB/**RP14**/CTED5/PMWR/PMENB/RB14	36	AN13/**RP19**/PMBE0/RC3
15	AN9/C3INA/**RP15**/CTED6/PMA14/PMCS/PMCS1/RB15	37	**RP20**/PMA4/RC4
16	AVSS	38	**RP21**/PMA3/RC5
17	AVDD	39	Vss
18	$\overline{\text{MCLR}}$	40	VDD
19	VREF+/CVREF+/AN0/C3INC/**RP26**/CTED1/RA0	41	PGD3/**RP5**/ASDA1/OCM1E/PMD7/RB5
20	VREF-/CVREF-/AN1/C3IND/**RP27**/CTED2/RA1	42	PGC3/**RP6**/ASCL1/OCM1F/PMD6/RB6
21	PGD1/AN2/CTCMP/C2INB/**RP0**/RB0	43	**RP7**/OCM1A/CTED3/PMD5/INT0/RB7
22	PGC1/AN1-/AN3/C2INA/**RP1**/CTED12/RB1	44	**RP8**/SCL1/OCM1B/CTED10/PMD4/RB8

Legend: **RPn** represents remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

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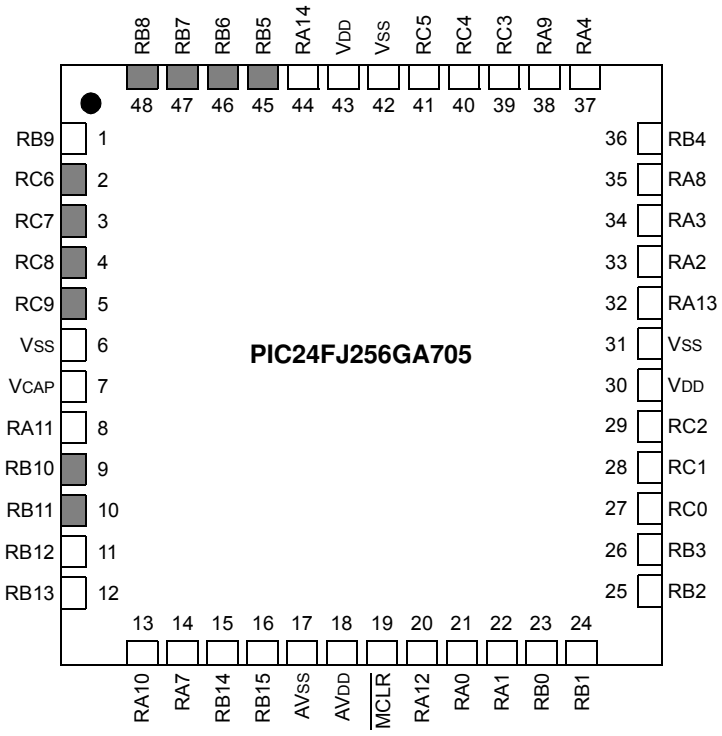
Pin Diagrams (PIC24FJ256GA705 Devices)

48-Pin UQFN



Legend: See Table 4 for a complete description of pin functions. Pinouts are subject to change.

Note: Gray shading indicates 5.5V tolerant input pins.

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJ256GA705 UQFN)

Pin	Function	Pin	Function
1	C1INC/C2INC/C3INC/$\overline{\text{TMPRN}}$/**RP9**/SDA1/T1CK/CTED4/PMD3/RB9	25	AN4/C1INB/**RP2**/SDA2/CTED13/RB2
2	**RP22**/PMA1/PMALH/RC6	26	AN5/C1INA/**RP3**/SCL2/CTED8/RB3
3	**RP23**/PMA0/PMALL/RC7	27	AN10/**RP16**/PMBE1/RC0
4	**RP24**/PMA5/RC8	28	AN11/**RP17**/PMA15/PMCS2/RC1
5	**RP25**/CTED7/PMA6/RC9	29	AN12/**RP18**/PMACK1/RC2
6	VSS	30	VDD
7	VCAP	31	VSS
8	**RPI29**/RA11	32	**RPI31**/RA13
9	PGD2/**RP10**/OCM1C/CTED11/PMD2/RB10	33	OSCI/CLKI/C1IND/RA2
10	PGC2/REFI1/**RP11**/CTED9/PMD1/RB11	34	OSCO/CLKO/C2IND/RA3
11	AN8/LVDIN/**RP12**/PMD0/RB12	35	TDO/PMA8/RA8
12	AN7/C1INC/**RP13**/OCM1D/CTPLS/PMRD/$\overline{\text{PMWR}}$/RB13	36	SOSCI/**RP4**/RB4
13	TMS/**RP28**/PMA2/PMALU/RA10	37	SOSCO/PWRLCLK/RA4
14	TCK/PMA7/RA7	38	TDI/PMA9/RA9
15	CVREF/AN6/C3INB/**RP14**/CTED5/PMWR/PMENB/RB14	39	AN13/**RP19**/PMBE0/RC3
16	AN9/C3INA/**RP15**/CTED6/PMA14/PMCS/PMCS1/RB15	40	**RP20**/PMA4/RC4
17	AVSS	41	**RP21**/PMA3/RC5
18	AVDD	42	VSS
19	$\overline{\text{MCLR}}$	43	VDD
20	**RPI30**/RA12	44	**RPI32**/RA14
21	VREF+/CVREF+/AN0/C3INC/**RP26**/CTED1/RA0	45	PGD3/**RP5**/ASDA1/OCM1E/PMD7/RB5
22	VREF-/CVREF-/AN1/C3IND/**RP27**/CTED2/RA1	46	PGC3/**RP6**/ASCL1/OCM1F/PMD6/RB6
23	PGD1/AN2/CTCMP/C2INB/**RP0**/RB0	47	**RP7**/OCM1A/CTED3/PMD5/INT0/RB7
24	PGC1/AN1-/AN3/C2INA/**RP1**/CTED12/RB1	48	**RP8**/SCL1/OCM1B/CTED10/PMD4/RB8

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

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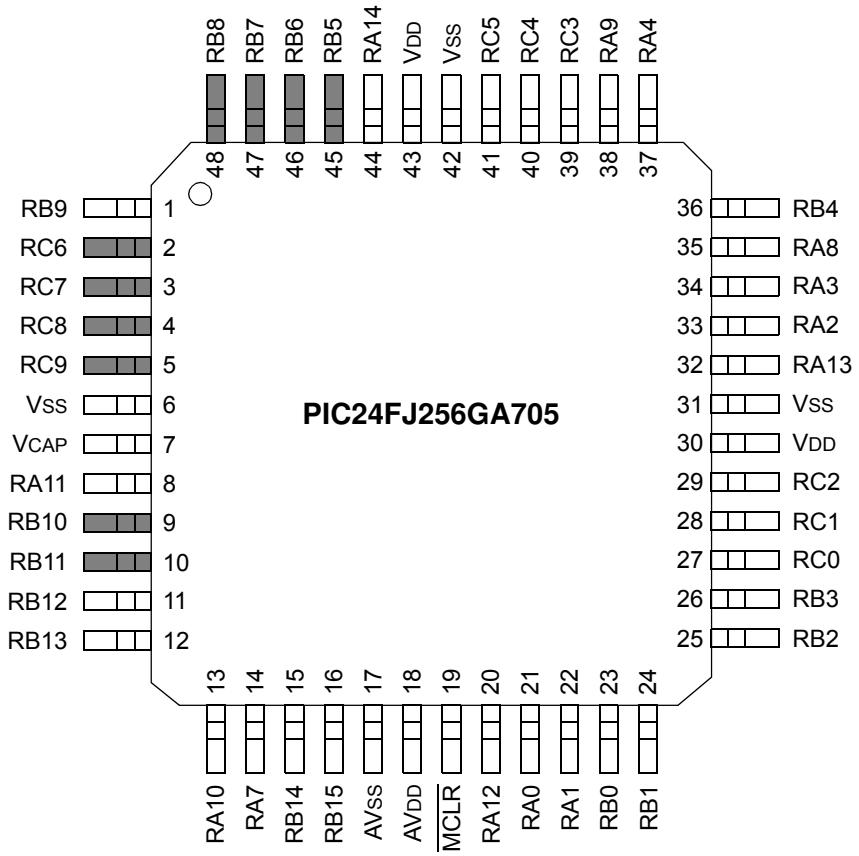
Pin Diagrams (PIC24FJ256GA705 Devices)

48-Pin TQFP



Legend: See Table 5 for a complete description of pin functions. Pinouts are subject to change.

Note: Gray shading indicates 5.5V tolerant input pins.

TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJ256GA705 TQFP)

Pin	Function	Pin	Function
1	C1INC/C2INC/C3INC/$\overline{\text{TMPRN}}$/**RP9**/SDA1/T1CK/CTED4/PMD3/RB9	25	AN4/C1INB/**RP2**/SDA2/CTED13/RB2
2	**RP22**/PMA1/PMALH/RC6	26	AN5/C1INA/**RP3**/SCL2/CTED8/RB3
3	**RP23**/PMA0/PMALL/RC7	27	AN10/**RP16**/PMBE1/RC0
4	**RP24**/PMA5/RC8	28	AN11/**RP17**/PMA15/PMCS2/RC1
5	**RP25**/CTED7/PMA6/RC9	29	AN12/**RP18**/PMACK1/RC2
6	VSS	30	VDD
7	VCAP	31	VSS
8	**RPI29**/RA11	32	**RPI31**/RA13
9	PGD2/**RP10**/OCM1C/CTED11/PMD2/RB10	33	OSCI/CLKI/C1IND/RA2
10	PGC2/REFI1/**RP11**/CTED9/PMD1/RB11	34	OSCO/CLKO/C2IND/RA3
11	AN8/LVDIN/**RP12**/PMD0//RB12	35	TDO/PMA8/RA8
12	AN7/C1INC/**RP13**/OCM1D/CTPLS/PMRD/$\overline{\text{PMWR}}$/RB13	36	SOSCI/**RP4**/RB4
13	TMS/**RP28**/PMA2/PMALU/RA10	37	SOSCO/PWRLCLK/RA4
14	TCK/PMA7/RA7	38	TDI/PMA9/RA9
15	CVREF/AN6/C3INB/**RP14**/CTED5/PMWR/PMENB/RB14	39	AN13/**RP19**/PMBE0/RC3
16	AN9/C3INA/**RP15**/CTED6/PMA14/PMCS/PMCS1/RB15	40	**RP20**/PMA4/RC4
17	AVSS	41	**RP21**/PMA3/RC5
18	AVDD	42	VSS
19	$\overline{\text{MCLR}}$	43	VDD
20	**RPI30**/RA12	44	**RPI32**/RA14
21	VREF+/CVREF+/AN0/C3INC/**RP26**/CTED1/RA0	45	PGD3/**RP5**/ASDA1/OCM1E/PMD7/RB5
22	VREF-/CVREF-/AN1/C3IND/**RP27**/CTED2/RA1	46	PGC3/**RP6**/ASCL1/OCM1F/PMD6/RB6
23	PGD1/AN2/CTCMP/C2INB/**RP0**/RB0	47	**RP7**/OCM1A/CTED3/PMD5/INT0/RB7
24	PGC1/AN1-/AN3/C2INA/**RP1**/CTED12/RB1	48	**RP8**/SCL1/OCM1B/CTED10/PMD4/RB8

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the PIC24FJ256GA705 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"CPU with Extended Data Space (EDS)"** (DS39732)
- **"PIC24F Data Memory"** (DS30009717)
- **"Direct Memory Access Controller (DMA)"** (DS39742)
- **"PIC24F Flash Program Memory"** (DS30009715)
- **"Data Memory with Extended Data Space (EDS)"** (DS39733)
- **"Reset"** (DS39712)
- **"Interrupts"** (DS70000600)
- **"Oscillator"** (DS39700)
- **"Power-Saving Features"** (DS39698)
- **"I/O Ports with Peripheral Pin Select (PPS)"** (DS39711)
- **"Timers"** (DS39704)
- **"Input Capture with Dedicated Timer"** (DS70000352)
- **"Output Compare with Dedicated Timer"** (DS70005159)
- **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035)
- **"Serial Peripheral Interface (SPI)"** (DS70005185)
- **"Inter-Integrated Circuit (I^2C)"** (DS70000195)
- **"UART"** (DS39708)
- **"Enhanced Parallel Master Port (EPMP)"** (DS39730)
- **"RTCC with Timestamp"** (DS70005193)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729)
- **"Configurable Logic Cell (CLC)"** (DS33949)
- **"12-Bit A/D Converter with Threshold Detect"** (DS39739)
- **"Scalable Comparator Module"** (DS39734)
- **"Dual Comparator Module"** (DS39710)
- **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (DS30009743)
- **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725)
- **"Watchdog Timer (WDT)"** (DS39697)
- **"CodeGuard™ Intermediate Security"** (DS70005182)
- **"High-Level Device Integration"** (DS39719)
- **"Programming and Diagnostics"** (DS39716)

NOTES:

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GA705
- PIC24FJ128GA705
- PIC24FJ256GA705
- PIC24FJ64GA704
- PIC24FJ128GA704
- PIC24FJ256GA704
- PIC24FJ64GA702
- PIC24FJ128GA702
- PIC24FJ256GA702

The PIC24FJ256GA705 family introduces large Flash and SRAM memory in smaller package sizes. This is a 16-bit microcontroller family with a broad peripheral feature set and enhanced computational performance. This family also offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but do not require the numerical processing power of a Digital Signal Processor (DSP).

Table 1-3 lists the functions of the various pins shown in the pinout diagrams.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 POWER-SAVING TECHNOLOGY

The PIC24FJ256GA705 family of devices includes Retention Sleep, a low-power mode with essential circuits being powered from a separate low-voltage regulator.

This new low-power mode also supports the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from this new feature, PIC24FJ256GA705 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of the Idle and Sleep modes

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ256GA705 family offer six different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- External Clock (EC) mode
- A Phase-Locked Loop (PLL) frequency multiplier, which allows processor speeds up to 32 MHz
- An internal Fast RC Oscillator (FRC), a nominal 8 MHz output with multiple frequency divider options
- A separate internal Low-Power RC Oscillator (LPRC), 31 kHz nominal for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger device.

The PIC24F family is pin-compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

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1.2 DMA Controller

PIC24FJ256GA705 family devices have a Direct Memory Access (DMA) Controller. This module acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Six independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.3 Other Special Features

- **Peripheral Pin Select:** The Peripheral Pin Select (PPS) feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Configurable Logic Cell:** The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins.
- **Timing Modules:** The PIC24FJ256GA705 family provides three independent, general purpose, 16-bit timers (two of which can be combined into a 32-bit timer). The devices also include 4 multiple output advanced Capture/Compare/PWM/Timer peripherals, and 3 independent legacy Input Capture and 3 independent legacy Output Compare modules.
- **Communications:** The PIC24FJ256GA705 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are 2 independent I^2C modules that support both Master and Slave modes of operation. Devices also have, through the PPS feature, 2 independent UARTs with built-in IrDA® encoders/decoders and 3 SPI modules.
- **Analog Features:** All members of the PIC24FJ256GA705 family include a 12-bit A/D Converter (A/D) module and a triple comparator module. The A/D module incorporates a range of new features that allow the converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions. The comparator module includes three analog comparators that are configurable for a wide range of operations.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ256GA705 family include the CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4 or 8 bits and address widths of up to 10 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.4 Details on Individual Family Members

Devices in the PIC24FJ256GA705 family are available in 28-pin, 44-pin and 48-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in five ways:

1. Flash program memory (64 Kbytes for PIC24FJ64GA70X devices, 128 Kbytes for PIC24FJ128GA70X devices, 256 Kbytes for PIC24FJ256GA70X devices).
2. Available I/O pins and ports (22 pins on 2 ports for 28-pin devices, and 36 and 40 pins on 3 ports for 44-pin/48-pin devices).
3. Enhanced Parallel Master Port (EPMP) is only available on 44-pin/48-pin devices.
4. Analog input channels (10 channels for 28-pin devices and 14 channels for 44-pin/48-pin devices).
5. CTMU input channels (12 channels for 28-pin devices and 13 channels for 44-pin/48-pin devices)

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

A list of the pin features available on the PIC24FJ256GA705 family devices, sorted by function, is shown in Table 1-3. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

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TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJXXXGA702: 28-PIN DEVICES

Features	PIC24FJ64GA702	PIC24FJ128GA702	PIC24FJ256GA702
Operating Frequency	DC – 32 MHz		
Program Memory (bytes)	64K	128K	256K
Program Memory (instruction words, 24 bits)	22,528	45,056	88,064
Data Memory (bytes)	16K		
Interrupt Sources (soft vectors/NMI traps)	124		
I/O Ports	Ports A, B		
Total I/O Pins	22		
Remappable Pins	18 (18 I/Os, 0 input only)		
DMA	1 6-channel		
16-Bit Timers	3(1)		
Real-Time Clock and Calendar (RTCC)	Yes		
Cyclic Redundancy Check (CRC)	Yes		
Input Capture Channels	3(1)		
Output Compare/PWM Channels	3(1)		
Input Change Notification Interrupt	21 (remappable pins)		
Serial Communications:			
UART	2(1)		
SPI (3-wire/4-wire)	3(1)		
I^2C	2		
Configurable Logic Cell (CLC)	2(1)		
Parallel Communications (EPMP/PSP)	No		
Capture/Compare/PWM/Timer Modules	4 Multiple CCPs 1 (6-output), 3 (2-output)		
JTAG Boundary Scan	Yes		
10/12-Bit Analog-to-Digital Converter (A/D) Module (input channels)	10		
Analog Comparators	3		
CTMU Interface	Yes		
Universal Serial Bus Controller	No		
Resets (and Delays)	Core POR, VDD POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)		
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations		
Packages	28-Pin QFN, UQFN, SOIC, SSOP and SPDIP		

Note 1: Some peripherals are accessible through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJXXXGA70X: 44-PIN AND 48-PIN DEVICES

Features	PIC24FJ64GA70X	PIC24FJ128GA70X	PIC24FJ256GA70X
Operating Frequency	DC – 32 MHz		
Program Memory (bytes)	64K	128K	256K
Program Memory (instruction words, 24 bits)	22,528	45,056	88,064
Data Memory (bytes)	16K		
Interrupt Sources (soft vectors/NMI traps)	124		
I/O Ports	Ports A, B, C		
Total I/O Pins:			
44-pin	35	35	35
48-pin	39	39	39
Remappable Pins:			
44-pin	29 (29 I/Os, 0 input only)		
48-pin	33 (29 I/Os, 4 input only)		
DMA (6-channel)	1		
16-Bit Timers	3(1)		
Real-Time Clock and Calendar (RTCC)	Yes		
Cyclic Redundancy Check (CRC)	Yes		
Input Capture Channels	3(1)		
Output Compare/PWM Channels	3(1)		
Input Change Notification Interrupt	25 (remappable pins)		
Serial Communications:			
UART	2(1)		
SPI (3-wire/4-wire)	3(1)		
I^2C	2		
Configurable Logic Cell (CLC)	2(1)		
Parallel Communications (EPMP/PSP)	Yes		
Capture/Compare/PWM/Timer Modules (MCCP)	4 Modules 1 (6-output), 3 (2-output)		
JTAG Boundary Scan	Yes		
10/12-Bit Analog-to-Digital Converter (A/D) Module (input channels)	14		
Analog Comparators	3		
CTMU Interface	Yes		
Universal Serial Bus Controller	No		
Resets (and delays)	Core POR, VDD POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)		
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations		
Packages	44-Pin TQFP, 48-Pin TQFP and QFN		

Note 1: Some peripherals are accessible through remappable pins.

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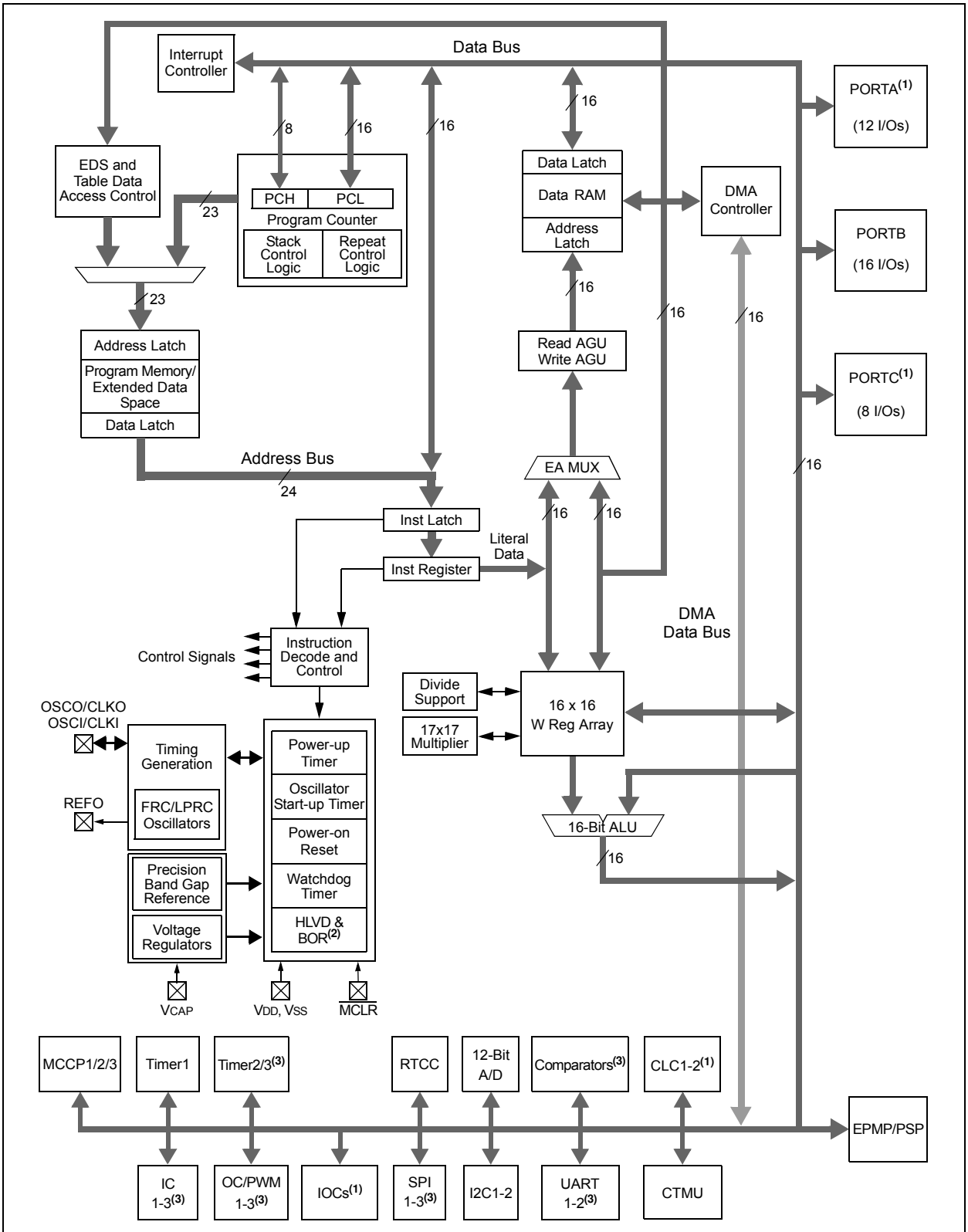
FIGURE 1-1: PIC24FJ256GA705 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-3 for specific implementations by pin count.
2: BOR functionality is provided when the on-board voltage regulator is enabled.
3: Some peripheral I/Os are only accessible through remappable pins.

TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
AN0	2	27	19	21	I	ANA	A/D Analog Inputs
AN1	3	28	20	22	I	ANA	
AN2	4	1	21	23	I	ANA	
AN3	5	2	22	24	I	ANA	
AN4	6	3	23	25	I	ANA	
AN5	7	4	24	26	I	ANA	
AN6	25	22	14	15	I	ANA	
AN7	24	21	11	12	I	ANA	
AN8	23	20	10	11	I	ANA	
AN9	26	23	15	16	I	ANA	
AN10	—	—	25	27	I	ANA	
AN11	—	—	26	28	I	ANA	
AN12	—	—	27	29	I	ANA	
AN13	—	—	36	39	I	ANA	
AV_{DD}	28	25	17	18	P	—	Positive Supply for Analog modules
AV_{SS}	27	24	16	17	P	—	Ground Reference for Analog modules
C1INA	7	4	24	26	I	ANA	Comparator 1 Input A
C1INB	6	3	23	25	I	ANA	Comparator 1 Input B
C1INC	18, 24	15, 21	1, 11	1, 12	I	ANA	Comparator 1 Input C
C1IND	9	6	30	33	I	ANA	Comparator 1 Input D
C2INA	5	2	22	24	I	ANA	Comparator 2 Input A
C2INB	4	1	21	23	I	ANA	Comparator 2 Input B
C2INC	18	15	1	1	I	ANA	Comparator 2 Input C
C2IND	10	7	31	34	I	ANA	Comparator 2 Input D
C3INA	26	23	15	16	I	ANA	Comparator 3 Input A
C3INB	25	22	14	15	I	ANA	Comparator 3 Input B
C3INC	2, 18	15, 27	1, 19	1, 21	I	ANA	Comparator 3 Input C
C3IND	3	28	20	22	I	ANA	Comparator 3 Input D
CLKI	9	6	30	33	—	—	Main Clock Input Connection
CLKO	10	7	31	34	O	DIG	System Clock Output
CTCMP	4	1	21	23	O	ANA	CTMU Comparator 2 Input (Pulse mode)

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

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TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
CTED1	2	27	19	21	I	ST	CTMU External Edge Inputs
CTED2	3	28	20	22	I	ST	
CTED3	16	13	43	47	I	ST	
CTED4	18	15	1	1	I	ST	
CTED5	25	22	14	15	I	ST	
CTED6	26	23	15	16	I	ST	
CTED7	—	—	5	5	I	ST	
CTED8	7	4	24	26	I	ST	
CTED9	22	19	9	10	I	ST	
CTED10	17	14	44	48	I	ST	
CTED11	21	18	8	9	I	ST	
CTED12	5	2	22	24	I	ST	
CTED13	6	3	23	25	I	ST	
CTPLS	24	21	11	12	O	DIG	CTMU Pulse Output
CV_{REF}	25	22	14	15	O	ANA	Comparator Voltage Reference Output
CV_{REF+}	2	27	19	21	I	ANA	Comparator Voltage Reference (high) Input
CV_{REF-}	3	28	20	22	I	ANA	Comparator Voltage Reference (low) Input
INT0	16	13	43	47	I	ST	External Interrupt Input 0
IOCA0	2	27	19	21	I	ST	PORTA Interrupt-on-Change
IOCA1	3	28	20	22	I	ST	
IOCA2	9	6	30	33	I	ST	
IOCA3	10	7	31	34	I	ST	
IOCA4	12	9	34	37	I	ST	
IOCA7	—	—	13	14	I	ST	
IOCA8	—	—	32	35	I	ST	
IOCA9	—	—	35	38	I	ST	
IOCA10	—	—	12	13	I	ST	
IOCA11	—	—	—	8	I	ST	
IOCA12	—	—	—	20	I	ST	
IOCA13	—	—	—	32	I	ST	
IOCA14	—	—	—	44	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
IOCB0	4	1	21	23	I	ST	PORTB Interrupt-on-Change
IOCB1	5	2	22	24	I	ST	
IOCB2	6	3	23	25	I	ST	
IOCB3	7	4	24	26	I	ST	
IOCB4	11	8	33	36	I	ST	
IOCB5	14	11	41	45	I	ST	
IOCB6	15	12	42	46	I	ST	
IOCB7	16	13	43	47	I	ST	
IOCB8	17	14	44	48	I	ST	
IOCB9	18	15	1	1	I	ST	
IOCB10	21	18	8	9	I	ST	
IOCB11	22	19	9	10	I	ST	
IOCB12	23	20	10	11	I	ST	
IOCB13	24	21	11	12	I	ST	
IOCB14	25	22	14	15	I	ST	
IOCB15	26	23	15	16	I	ST	
IOCC1	—	—	26	28	I	ST	PORTC Interrupt-on-Change
IOCC2	—	—	27	29	I	ST	
IOCC3	—	—	36	39	I	ST	
IOCC4	—	—	37	40	I	ST	
IOCC5	—	—	38	41	I	ST	
IOCC6	—	—	2	2	I	ST	
IOCC7	—	—	3	3	I	ST	
IOCC8	—	—	4	4	I	ST	
IOCC9	—	—	5	5	I	ST	
$\overline{MCLR}$	1	26	18	19	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OCM1A	16	13	43	47	O	DIG	MCCP1 Outputs
OCM1B	17	14	44	48	O	DIG	
OCM1C	21	18	8	9	O	DIG	
OCM1D	24	21	11	12	O	DIG	
OCM1E	14	11	41	45	O	DIG	
OCM1F	15	12	42	46	O	DIG	
OSCI	9	6	30	33	I	ANA/ST	Main Oscillator Input Connection
OSCO	10	7	31	34	O	ANA	Main Oscillator Output Connection

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

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TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
PGC1	5	2	22	24	I	ST	ICSP™ Programming Clock
PGC2	22	19	9	10	I	ST	
PGC3	15	12	42	46	I	ST	
PGD1	4	1	21	23	I/O	DIG/ST	ICSP Programming Data
PGD2	21	18	8	9	I/O	DIG/ST	
PGD3	14	11	41	45	I/O	DIG/ST	
PMA0	—	—	3	3	I/O	DIG/ST/ TTL	Parallel Master Port Address<0>/ Address Latch Low
PMA1	—	—	2	2	I/O	DIG/ST/ TTL	Parallel Master Port Address<1>/ Address Latch High
PMA2	—	—	12	13	I/O	DIG/ST/ TTL	Parallel Master Port Address<2>
PMA3	—	—	38	41	I/O	DIG/ST/ TTL	Parallel Master Port Address<3>
PMA4	—	—	37	40	I/O	DIG/ST/ TTL	Parallel Master Port Address<4>
PMA5	—	—	4	4	I/O	DIG/ST/ TTL	Parallel Master Port Address<5>
PMA6	—	—	5	5	I/O	DIG/ST/ TTL	Parallel Master Port Address<6>
PMA7	—	—	13	14	I/O	DIG/ST/ TTL	Parallel Master Port Address<7>
PMA8	—	—	32	35	I/O	DIG/ST/ TTL	Parallel Master Port Address<8>
PMA9	—	—	35	38	I/O	DIG/ST/ TTL	Parallel Master Port Address<9>
PMA14/PMCS/ PMCS1	—	—	15	16	I/O	DIG/ST/ TTL	Parallel Master Port Address<14>/ Slave Chip Select/Chip Select 1 Strobe

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
PMD0	—	—	10	11	I/O	DIG/ST/ TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	—	—	9	10	I/O	DIG/ST/ TTL	
PMD2	—	—	8	9	I/O	DIG/ST/ TTL	
PMD3	—	—	1	1	I/O	DIG/ST/ TTL	
PMD4	—	—	44	48	I/O	DIG/ST/ TTL	
PMD5	—	—	43	47	I/O	DIG/ST/ TTL	
PMD6	—	—	42	46	I/O	DIG/ST/ TTL	
PMD7	—	—	41	45	I/O	DIG/ST/ TTL	
PMRD/$\overline{\text{PMWR}}$	—	—	11	12	I/O	DIG/ST/ TTL	Parallel Master Port Read Strobe/ Write Strobe
PMWR/PMENB	—	—	14	15	I/O	DIG/ST/ TTL	Parallel Master Port Write Strobe/ Enable Strobe
PWRGT	—	—	—	—	O	DIG	Real-Time Clock Power Control Output
PWRLCLK	12	9	34	37	I	ST	Real-Time Clock 50/60 Hz Clock Input

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

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TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
RA0	2	27	19	21	I/O	DIG/ST	PORTA Digital I/Os
RA1	3	28	20	22	I/O	DIG/ST	
RA2	9	6	30	33	I/O	DIG/ST	
RA3	10	7	31	34	I/O	DIG/ST	
RA4	12	9	34	37	I/O	DIG/ST	
RA7	—	—	13	14	I/O	DIG/ST	
RA8	—	—	32	35	I/O	DIG/ST	
RA9	—	—	35	38	I/O	DIG/ST	
RA10	—	—	12	13	I/O	DIG/ST	
RA11	—	—	—	8	I/O	DIG/ST	
RA12	—	—	—	20	I/O	DIG/ST	
RA13	—	—	—	32	I/O	DIG/ST	
RA14	—	—	—	44	I/O	DIG/ST	
RB0	4	1	21	23	I/O	DIG/ST	PORTB Digital I/Os
RB1	5	2	22	24	I/O	DIG/ST	
RB2	6	3	23	25	I/O	DIG/ST	
RB3	7	4	24	26	I/O	DIG/ST	
RB4	11	8	33	36	I/O	DIG/ST	
RB5	14	11	41	45	I/O	DIG/ST	
RB6	15	12	42	46	I/O	DIG/ST	
RB7	16	13	43	47	I/O	DIG/ST	
RB8	17	14	44	48	I/O	DIG/ST	
RB9	18	15	1	1	I/O	DIG/ST	
RB10	21	18	8	9	I/O	DIG/ST	
RB11	22	19	9	10	I/O	DIG/ST	
RB12	23	20	10	11	I/O	DIG/ST	
RB13	24	21	11	12	I/O	DIG/ST	
RB14	25	22	14	15	I/O	DIG/ST	
RB15	26	23	15	16	I/O	DIG/ST	
RC1	—	—	26	28	I/O	DIG/ST	PORTC Digital I/Os
RC2	—	—	27	29	I/O	DIG/ST	
RC3	—	—	36	39	I/O	DIG/ST	
RC4	—	—	37	40	I/O	DIG/ST	
RC5	—	—	38	41	I/O	DIG/ST	
RC6	—	—	2	2	I/O	DIG/ST	
RC7	—	—	3	3	I/O	DIG/ST	
RC8	—	—	4	4	I/O	DIG/ST	
RC9	—	—	5	5	I/O	DIG/ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver