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PIC24FJ256GB210 Family Data Sheet

64/100-Pin, 16-Bit Flash Microcontrollers with USB On-The-Go (OTG)

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QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

PIC24FJ256GB210 FAMILY

64/100-Pin, 16-Bit Flash Microcontrollers with USB On-The-Go (OTG)

Universal Serial Bus Features:

- USB v2.0 On-The-Go (OTG) Compliant
- Dual Role Capable – Can act as either Host or Peripheral
- Low-Speed (1.5 Mbps) and Full-Speed (12 Mbps) USB Operation in Host mode
- Full-Speed USB Operation in Device mode
- High-Precision PLL for USB
- Supports up to 32 Endpoints (16 bidirectional):
  - USB module can use the internal RAM location from 0x800 to 0xFFFF as USB endpoint buffers
- On-Chip USB Transceiver with Interface for Off-Chip Transceiver
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- On-Chip Pull-up and Pull-Down Resistors

Peripheral Features:

- Enhanced Parallel Master Port/Parallel Slave Port (EPMP/PSP):
  - Direct access from CPU with an Extended Data Space (EDS) interface
  - 4, 8 and 16-bit wide data bus
  - Up to 23 programmable address lines
  - Up to 2 chip select lines
  - Up to 2 Acknowledgement lines (one per chip select)
  - Programmable address/data multiplexing
  - Programmable address and data Wait states
  - Programmable polarity on control signals

Peripheral Features (Continued):

- Peripheral Pin Select:
  - Up to 44 available pins (100-pin devices)
- Three 3-Wire/4-Wire SPI modules (supports 4 Frame modes)
- Three I^2C™ modules Supporting Multi-Master/Slave modes and 7-Bit/10-Bit Addressing
- Four UART modules:
  - Supports RS-485, RS-232, LIN/J2602 protocols and IrDA®
- Five 16-Bit Timers/Counters with Programmable Prescaler
- Nine 16-Bit Capture Inputs, each with a Dedicated Time Base
- Nine 16-Bit Compare/PWM Outputs, each with a Dedicated Time Base
- Hardware Real-Time Clock and Calendar (RTCC)
- Enhanced Programmable Cyclic Redundancy Check (CRC) Generator
- Up to 5 External Interrupt Sources

PIC24FJ Device	Pins	Program Memory (bytes)	SRAM (bytes)	Remappable Peripherals					I^2C™	10-Bit A/D (ch)	Comparators	CTMU	EPMP/PSP	RTCC	USB OTG
				Remappable Pins	16-Bit Timers	IC/OC PWM	UART w/IrDA®	SPI							
PIC24FJ128GB206	64	128K	96K	29	5	9/9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ256GB206	64	256K	96K	29	5	9/9	4	3	3	16	3	Y	Y	Y	Y
PIC24FJ128GB210	100/121	128K	96K	44	5	9/9	4	3	3	24	3	Y	Y	Y	Y
PIC24FJ256GB210	100/121	256K	96K	44	5	9/9	4	3	3	24	3	Y	Y	Y	Y

High-Performance CPU

- Modified Harvard Architecture
- Up to 16 MIPS Operation at 32 MHz
- 8 MHz Internal Oscillator
- 17-Bit x 17-Bit Single-Cycle Hardware Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture with Flexible Addressing modes
- Linear Program Memory Addressing, up to 12 Mbytes
- Data Memory Addressing, up to 16 Mbytes:
  - 2K SFR space
  - 30K linear data memory
  - 66K extended data memory
  - Remaining (from 16 Mbytes) memory (external) can be accessed using extended data Memory (EDS) and EPMP (EDS is divided into 32-Kbyte pages)
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory

Power Management:

- On-Chip Voltage Regulator of 1.8V
- Switch between Clock Sources in Real Time
- Idle, Sleep and Doze modes with Fast Wake-up and Two-Speed Start-up
- Run Mode: 800 μA/MIPS, 3.3V Typical
- Sleep mode Current Down to 20 μA, 3.3V Typical
- Standby Current with 32 kHz Oscillator: 22 μA, 3.3V Typical

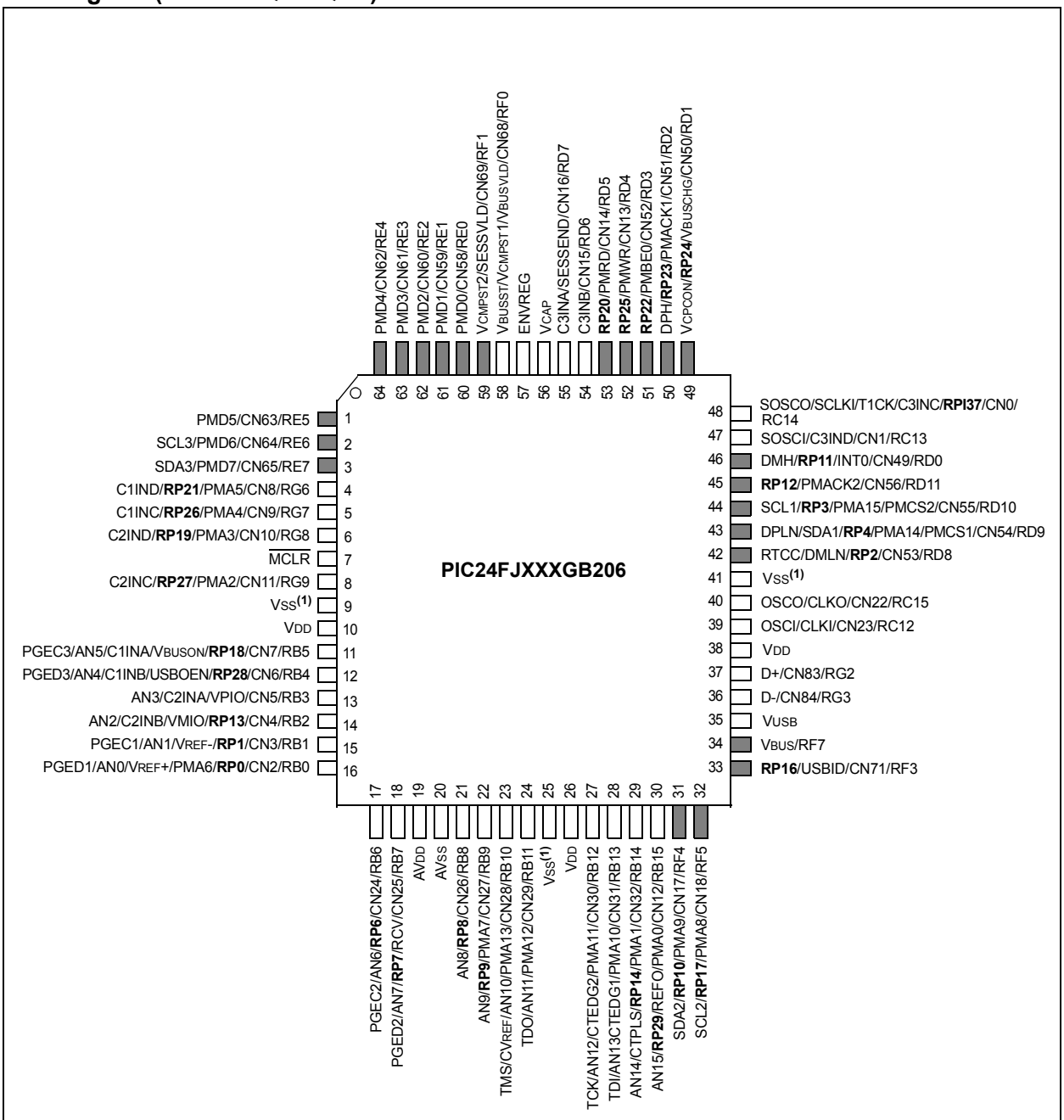
Analog Features:

- 10-Bit, up to 24-Channel Analog-to-Digital (A/D) Converter at 500 ksps:
  - Operation is possible in Sleep mode
  - Band gap reference input feature
- Three Analog Comparators with Programmable Input/Output Configuration
- Charge Time Measurement Unit (CTMU):
  - Supports capacitive touch sensing for touch screens and capacitive switches
  - Minimum time measurement setting at 100 ps
- Available LVD Interrupt V_{LVD} Level

Special Microcontroller Features:

- Operating Voltage Range of 2.2V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- Configurable Open-Drain Outputs on Digital I/O Ports
- High-Current Sink/Source (18 mA/18 mA) on all I/O Ports
- Selectable Power Management modes:
  - Sleep, Idle and Doze modes with fast wake-up
- Fail-Safe Clock Monitor (FSCM) Operation:
  - Detects clock failure and switches to on-chip, FRC oscillator
- On-Chip LDO Regulator
- Power-on Reset (POR) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Flexible Watchdog Timer (WDT) with On-Chip Low-Power RC Oscillator for Reliable Operation
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Debug (ICD) via 2 Pins
- JTAG Boundary Scan Support
- Flash Program Memory:
  - 10,000 erase/write cycle endurance (minimum)
  - 20-year data retention minimum
  - Selectable write protection boundary
  - Self-reprogrammable under software control
  - Write protection option for Configuration Words

Pin Diagram (64-Pin TQFP/QFN)



Note 1: The back pad on QFN devices should be connected to VSS.

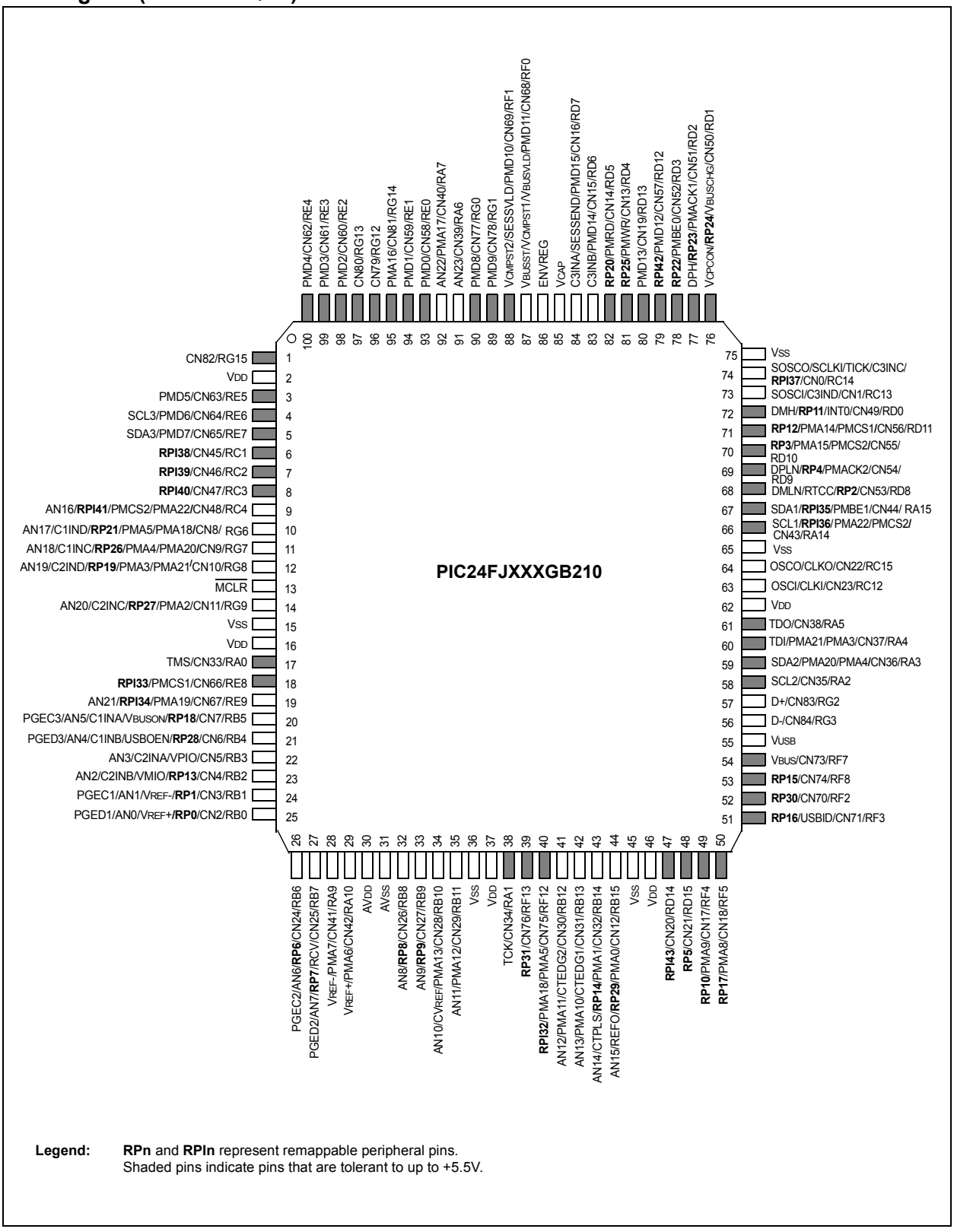
Legend: **RPn** and **RPIn** represents remappable peripheral pins.
Shaded pins indicate pins that are tolerant to up to +5.5V.

TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 64-PIN DEVICES

Pin	Function	Pin	Function
1	PMD5/CN63/RE5	33	**RP16**/USBID/CN71/RF3
2	SCL3/PMD6/CN64/RE6	34	VBUS/RF7
3	SDA3/PMD7/CN65/RE7	35	VUSB
4	C1IND/**RP21**/PMA5/CN8/RG6	36	D-/CN84/RG3
5	C1INC/**RP26**/PMA4/CN9/RG7	37	D+/CN83/RG2
6	C2IND/**RP19**/PMA3/CN10/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/CN23/RC12
8	C2INC/**RP27**/PMA2/CN11/RG9	40	OSCO/CLKO/CN22/RC15
9	VSS	41	VSS
10	VDD	42	RTCC/DMLN/**RP2**/CN53/RD8
11	PGEC3/AN5/C1INA/VBUSON/**RP18**/CN7/RB5	43	DPLN/SDA1/**RP4**/PMACK2/CN54/RD9
12	PGED3/AN4/C1INB/USBOEN/**RP28**/CN6/RB4	44	SCL1/**RP3**/PMA15/PMCS2**(1)**/CN55/RD10
13	AN3/C2INA/VPIO/CN5/RB3	45	**RP12**/PMA14/PMCS1**(1)**/CN56/RD11
14	AN2/C2INB/VMIO/**RP13**/CN4/RB2	46	DMH/**RP11**/INT0/CN49/RD0
15	PGEC1/AN1/VREF-/**RP1**/CN3/RB1	47	SOSCI/C3IND/CN1/RC13
16	PGED1/AN0/VREF+/PMA6/**RP0**/CN2/RB0	48	SOSCO/SCLKI/T1CK/C3INC/**RPI37**/CN0/RC14
17	PGEC2/AN6/**RP6**/CN24/RB6	49	VCPCON/**RP24**/VBUSCHG/CN50/RD1
18	PGED2/AN7/**RP7**/RCV/CN25/RB7	50	DPH/**RP23**/PMACK1/CN51/RD2
19	AVDD	51	**RP22**/PMBE0/CN52/RD3
20	AVSS	52	**RP25**/PMWR/CN13/RD4
21	AN8/**RP8**/CN26/RB8	53	**RP20**/PMRD/CN14/RD5
22	AN9/**RP9**/PMA7/CN27/RB9	54	C3INB/CN15/RD6
23	TMS/CVREF/AN10/PMA13/CN28/RB10	55	C3INA/SESSEND/CN16/RD7
24	TDO/AN11/PMA12/CN29/RB11	56	VCAP
25	VSS	57	ENVREG
26	VDD	58	VBUSST/VCMPST1/VBUSVLD/CN68/RF0
27	TCK/AN12/CTEDG2/PMA11/CN30/RB12	59	VCMPST2/SESSVLD/CN69/RF1
28	TDI/AN13/CTEDG1/PMA10/CN31/RB13	60	PMD0/CN58/RE0
29	AN14/CTPLS/**RP14**/PMA1/CN32/RB14	61	PMD1/CN59/RE1
30	AN15/**RP29**/REFO/PMA0/CN12/RB15	62	PMD2/CN60/RE2
31	SDA2/**RP10**/PMA9/CN17/RF4	63	PMD3/CN61/RE3
32	SCL2/**RP17**/PMA8/CN18/RF5	64	PMD4/CN62/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.
Note 1: Pin assignment for PMCSx when CSF<1:0> are not equal to '00'.

Pin Diagram (100-Pin TQFP)



Legend: **RPn** and **RPIn** represent remappable peripheral pins.
Shaded pins indicate pins that are tolerant to up to +5.5V.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 100-PIN DEVICES

Pin	Function	Pin	Function
1	CN82/RG15	41	AN12/PMA11/CTEDG2/CN30/RB12
2	VDD	42	AN13/PMA10/CTEDG1/CN31/RB13
3	PMD5/CN63/RE5	43	AN14/CTPLS/**RP14**/PMA1/CN32/RB14
4	SCL3/PMD6/CN64/RE6	44	AN15/REFO/**RP29**/PMA0/CN12/RB15
5	SDA3/PMD7/CN65/RE7	45	VSS
6	**RPI38**/CN45/RC1	46	VDD
7	**RPI39**/CN46/RC2	47	**RPI43**/CN20/RD14
8	**RPI40**/CN47/RC3	48	**RP5**/CN21/RD15
9	AN16/**RPI41**/PMCS2/PMA22(2)/CN48/RC4	49	**RP10**/PMA9/CN17/RF4
10	AN17/C1IND/**RP21**/PMA5/PMA18(2)/CN8/RG6	50	**RP17**/PMA8/CN18/RF5
11	AN18/C1INC/**RP26**/PMA4/PMA20(2)/CN9/RG7	51	**RP16**/USBID/CN71/RF3
12	AN19/C2IND/**RP19**/PMA3/PMA21(2)/CN10/RG8	52	**RP30**/CN70/RF2
13	$\overline{\text{MCLR}}$	53	**RP15**/CN74/RF8
14	AN20/C2INC/**RP27**/PMA2/CN11/RG9	54	VBUS/CN73/RF7
15	VSS	55	VUSB
16	VDD	56	D-/CN84/RG3
17	TMS/CN33/RA0	57	D+/CN83/RG2
18	**RPI33**/PMCS1/CN66/RE8	58	SCL2/CN35/RA2
19	AN21/**RPI34**/PMA19/CN67/RE9	59	SDA2/PMA20/PMA4(2)/CN36/RA3
20	PGEC3/AN5/C1INA/VBUSON/**RP18**/CN7/RB5	60	TDI/PMA21/PMA3(2)/CN37/RA4
21	PGED3/AN4/C1INB/USBOEN/**RP28**/CN6/RB4	61	TDO/CN38/RA5
22	AN3/C2INA/VPIO/CN5/RB3	62	VDD
23	AN2/C2INB/VMIO/**RP13**/CN4/RB2	63	OSCI/CLKI/CN23/RC12
24	PGEC1/AN1/VREF-(1)/**RP1**/CN3/RB1	64	OSCO/CLKO/CN22/RC15
25	PGED1/AN0/VREF+(1)/**RP0**/CN2/RB0	65	VSS
26	PGEC2/AN6/**RP6**/CN24/RB6	66	SCL1/**RPI36**/PMA22/PMCS2(2)/CN43/RA14
27	PGED2/AN7/**RP7**/RCV/CN25/RB7	67	SDA1/**RPI35**/PMBE1/CN44/RA15
28	VREF-/PMA7/CN41/RA9	68	DMLN/RTCC/**RP2**/CN53/RD8
29	VREF+/PMA6/CN42/RA10	69	DPLN/**RP4**/PMACK2/CN54/RD9
30	AVDD	70	**RP3**/PMA15/PMCS2(3)/CN55/RD10
31	AVSS	71	**RP12**/PMA14/PMCS1(3)/CN56/RD11
32	AN8/**RP8**/CN26/RB8	72	DMH/**RP11**/INT0/CN49/RD0
33	AN9/**RP9**/CN27/RB9	73	SOSCI/C3IND/CN1/RC13
34	AN10/CVREF/PMA13/CN28/RB10	74	SOSCO/SCLKI/T1CK/C3INC/**RPI37**/CN0/RC14
35	AN11/PMA12/CN29/RB11	75	VSS
36	VSS	76	VCPCON/**RP24**/VBUSCHG/CN50/RD1
37	VDD	77	DPH/**RP23**/PMACK1/CN51/RD2
38	TCK/CN34/RA1	78	**RP22**/PMBE0/CN52/RD3
39	**RP31**/CN76/RF13	79	**RPI42**/PMD12/CN57/RD12
40	**RPI32**/PMA18/PMA5(2)/CN75/RF12	80	PMD13/CN19/RD13

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: Alternate pin assignments for VREF+ and VREF- when the $\overline{\text{ALTVREF}}$ Configuration bit is programmed.

2: Alternate pin assignments for EPMP when the $\overline{\text{ALTPMP}}$ Configuration bit is programmed (only in 100-pin devices).

3: Pin assignment for PMCSx when CSF<1:0> is not equal to '00'.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 100-PIN DEVICES (CONTINUED)

Pin	Function	Pin	Function
81	**RP25**/PMWR/CN13/RD4	91	AN23/CN39/RA6
82	**RP20**/PMRD/CN14/RD5	92	AN22/PMA17/CN40/RA7
83	C3INB/PMD14/CN15/RD6	93	PMD0/CN58/RE0
84	C3INA/SESSEND/PMD15/CN16/RD7	94	PMD1/CN59/RE1
85	VCAP	95	PMA16/CN81/RG14
86	ENVREG	96	CN79/RG12
87	VBUSST/VCMPST1/VBUSVLD/PMD11/CN68/RF0	97	CN80/RG13
88	VCMPST2/SESSVLD/PMD10/CN69/RF1	98	PMD2/CN60/RE2
89	PMD9/CN78/RG1	99	PMD3/CN61/RE3
90	PMD8/CN77/RG0	100	PMD4/CN62/RE4

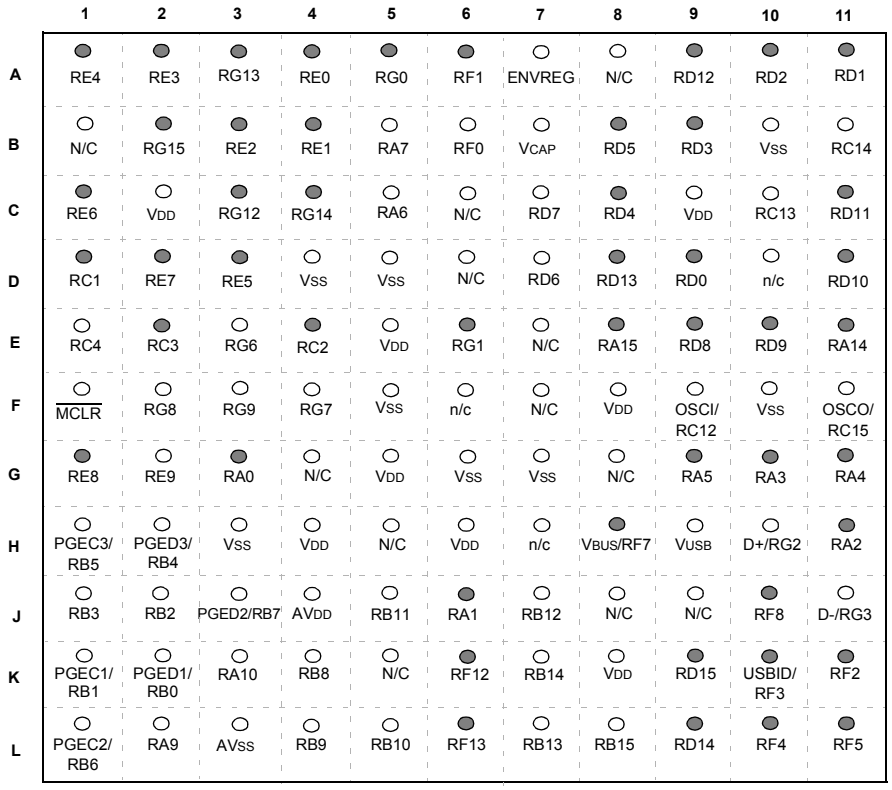
Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: Alternate pin assignments for VREF+ and VREF- when the ALTVREF Configuration bit is programmed.

2: Alternate pin assignments for EPMP when the ALTPMP Configuration bit is programmed (only in 100-pin devices).

3: Pin assignment for PMCSx when CSF<1:0> is not equal to '00'.

Pin Diagram – Top View (121-Pin BGA)(1)



	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	ENVREG	N/C	RD12	RD2	RD1
B	N/C	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	N/C	RD7	RD4	VDD	RC13	RD11
D	RC1	RE7	RE5	VSS	VSS	N/C	RD6	RD13	RD0	n/c	RD10
E	RC4	RC3	RG6	RC2	VDD	RG1	N/C	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	n/c	N/C	VDD	OSCI/ RC12	VSS	OSCO/ RC15
G	RE8	RE9	RA0	N/C	VDD	VSS	VSS	N/C	RA5	RA3	RA4
H	PGEC3/ RB5	PGED3/ RB4	VSS	VDD	N/C	VDD	n/c	VBUS/RF7	VUSB	D+/RG2	RA2
J	RB3	RB2	PGED2/RB7	AVDD	RB11	RA1	RB12	N/C	N/C	RF8	D-/RG3
K	PGEC1/ RB1	PGED1/ RB0	RA10	RB8	N/C	RF12	RB14	VDD	RD15	USBID/ RF3	RF2
L	PGEC2/ RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: See Table 3 for complete functional pinout descriptions.

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.
Shaded pins indicate pins tolerant to up to +5.5V.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 121-PIN (BGA) DEVICES

Pin	Function	Pin	Function
A1	PMD4/CN62/RE4	E5	VDD
A2	PMD3/CN61/RE3	E6	PMD9/CN78/RG1
A3	CN80/RG13	E7	N/C
A4	PMD0/CN58/RE0	E8	SDA1/**RPI35**/PMBE1/CN44/RA15
A5	PMD8/CN77/RG0	E9	DMLN/RTCC/**RP2**/CN53/RD8
A6	VCMPST2/SESSVLD/PMD10/CN69/RF1	E10	DPLN/**RP4**/PMACK2/CN54/RD9
A7	ENVREG	E11	SCL1/**RPI36**/PMA22/PMCS2(2)/CN43/RA14
A8	N/C	F1	$\overline{\text{MCLR}}$
A9	**RPI42**/PMD12/CN57/RD12	F2	AN19/C2IND/**RP19**/PMA3/PMA21(2)/CN10/RG8
A10	DPH/**RP23**/PMACK1/CN51/RD2	F3	AN20/C2INC/**RP27**/PMA2/CN11/RG9
A11	VCPCON/**RP24**/VBUSCHG/CN50/RD1	F4	AN18/C1INC/**RP26**/PMA4/PMA20(2)/CN9/RG7
B1	N/C	F5	VSS
B2	CN82/RG15	F6	N/C
B3	PMD2/CN60/RE2	F7	N/C
B4	PMD1/CN59/RE1	F8	VDD
B5	AN22/PMA17/CN40/RA7	F9	OSCI/CLKI/CN23/RC12
B6	VBUSST/VCMPST1/VBUSVLD/PMD11/CN68/RF0	F10	VSS
B7	VCAP	F11	OSCO/CLKO/CN22/RC15
B8	**RP20**/PMRD/CN14/RD5	G1	**RPI33**/PMCS1/CN66/RE8
B9	**RP22**/PMBE0/CN52/RD3	G2	AN21/**RPI34**/PMA19/CN67/RE9
B10	VSS	G3	TMS/CN33/RA0
B11	SOSCO/SCLKI/T1CK/C3INC/**RPI37**/CN0/RC14	G4	N/C
C1	SCL3/PMD6/CN64/RE6	G5	VDD
C2	VDD	G6	VSS
C3	VSYNC/CN79/RG12	G7	VSS
C4	PMA16/CN81/RG14	G8	N/C
C5	AN23/CN39/RA6	G9	TDO/CN38/RA5
C6	N/C	G10	SDA2/PMA20/PMA4(2)/CN36/RA3
C7	C3INA/SESSEND/PMD15/CN16/RD7	G11	TDI/PMA21/PMA3(2)/CN37/RA4
C8	**RP25**/PMWR/CN13/RD4	H1	PGEC3/AN5/C1INA/VBUSON/**RP18**/CN7/RB5
C9	VDD	H2	PGED3/AN4/C1INB/USBOEN/**RP28**/CN6/RB4
C10	SOSCI/C3IND/CN1/RC13	H3	VSS
C11	**RP12**/PMA14/PMCS1(3)/CN56/RD11	H4	VDD
D1	**RPI38**/CN45/RC1	H5	N/C
D2	SDA3/PMD7/CN65/RE7	H6	VDD
D3	PMD5/CN63/RE5	H7	N/C
D4	VSS	H8	VBUS/CN73/RF7
D5	VSS	H9	VUSB
D6	N/C	H10	D+/CN83/RG2
D7	C3INB/PMD14/CN15/RD6	H11	SCL2/CN35/RA2
D8	PMD13/CN19/RD13	J1	AN3/C2INA/VPIO/CN5/RB3
D9	DMH/**RP11**/INT0/CN49/RD0	J2	AN2/C2INB/VMIO/**RP13**/CN4/RB2
D10	N/C	J3	PGED2/AN7/**RP7**/RCV/CN25/RB7
D11	**RP3**/PMA15/PMCS2(3)/CN55/RD10	J4	AVDD
E1	AN16/**RPI41**/PMCS2/PMA22(2)/CN48/RC4	J5	AN11/PMA12/CN29/RB11
E2	**RPI40**/CN47/RC3	J6	TCK/CN34/RA1
E3	AN17/C1IND/**RP21**/PMA5/PMA18(2)/CN8/RG6	J7	AN12/PMA11/CTEDG2/CN30/RB12
E4	**RPI39**/CN46/RC2	J8	N/C

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Note 1: Alternate pin assignments for VREF+ and VREF- when the ALTVREF Configuration bit is programmed.

2: Alternate pin assignments for EPMP when the ALTPMP Configuration bit is programmed (only in 100-pin devices).

3: Pin assignment for PMCSx when CSF<1:0> is not equal to '00'.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 121-PIN (BGA) DEVICES (CONTINUED)

Pin	Function	Pin	Function
J9	N/C	L1	PGEC2/AN6/**RP6**/CN24/RB6
J10	**RP15**/CN74/RF8	L2	VREF-(1)/PMA7/CN41/RA9
J11	D-/CN84/RG3	L3	AVSS
K1	PGEC1/AN1/VREF-(1)/**RP1**/CN3/RB1	L4	AN9/**RP9**/CN27/RB9
K2	PGED1/AN0/VREF+(1)/**RP0**/CN2/RB0	L5	AN10/CVREF/PMA13/CN28/RB10
K3	VREF+(1)/PMA6/CN42/RA10	L6	**RP31**/CN76/RF13
K4	AN8/**RP8**/CN26/RB8	L7	AN13/PMA10/CTEDG1/CN31/RB13
K5	N/C	L8	AN15/REFO/**RP29**/PMA0/CN12/RB15
K6	**RPI32**/PMA18/PMA5(2)/CN75/RF12	L9	**RPI43**/CN20/RD14
K7	AN14/CTPLS/**RP14**/PMA1/CN32/RB14	L10	**RP10**/PMA9/CN17/RF4
K8	VDD	L11	**RP17**/PMA8/SCL2/CN18/RF5
K9	**RP5**/CN21/RD15	—	—
K10	**RP16**/USBID/CN71/RF3	—	—
K11	**RP30**/CN70/RF2	—	—

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Note 1: Alternate pin assignments for VREF+ and VREF- when the ALTVREF Configuration bit is programmed.

2: Alternate pin assignments for EPMP when the ALTPMP Configuration bit is programmed (only in 100-pin devices).

3: Pin assignment for PMCSx when CSF<1:0> is not equal to '00'.

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ128GB206
- PIC24FJ256GB206
- PIC24FJ128GB210
- PIC24FJ256GB210

The PIC24FJ256GB210 family enhances on the existing line of Microchip's 16-bit microcontrollers, adding a large data RAM, up to 96 Kbytes. The PIC24FJ256GB210 family allows the CPU to fetch data directly from an external memory device using the EPMP module.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 POWER-SAVING TECHNOLOGY

All of the devices in the PIC24FJ256GB210 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **On-the-Fly Clock Switching:** The device clock can be changed under software control to the Timer1 source or the internal, low-power RC oscillator during operation, allowing the user to incorporate power-saving ideas into their software designs.
- **Doze Mode Operation:** When timing-sensitive applications, such as serial communications, require the uninterrupted operation of peripherals, the CPU clock speed can be selectively reduced, allowing incremental power savings without missing a beat.
- **Instruction-Based Power-Saving Modes:** The microcontroller can suspend all operations, or selectively shut down its core while leaving its peripherals active with a single instruction in software.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ256GB210 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes using crystals or ceramic resonators.
- Two External Clock modes offering the option of a divide-by-2 clock output.
- A Fast Internal Oscillator (FRC) with a nominal 8 MHz output, which can also be divided under software control to provide clock speeds as low as 31 kHz.
- A Phase Lock Loop (PLL) frequency multiplier, available to the external oscillator modes and the FRC oscillator, which allows clock speeds of up to 32 MHz.
- A separate Low-Power Internal RC Oscillator (LPRC) with a fixed 31 kHz output, which provides a low-power option for timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger, or even in jumping from 64-pin to 100-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

1.2 USB On-The-Go

The USB On-The-Go (USB OTG) module provides on-chip functionality as a target device, compatible with the USB 2.0 standard, as well as limited stand-alone functionality as a USB embedded host. By implementing USB Host Negotiation Protocol (HNP), the module can also dynamically switch between device and host operation, allowing for a much wider range of versatile USB enabled applications on a microcontroller platform.

In addition to USB host functionality, PIC24FJ256GB210 family devices provide a true single chip USB solution, including an on-chip transceiver and voltage regulator, and a voltage boost generator for sourcing bus power during host operations.

1.3 Other Special Features

- **Peripheral Pin Select:** The Peripheral Pin Select (PPS) feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ256GB210 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are three independent I^2C™ modules that support both Master and Slave modes of operation. Devices also have, through the PPS feature, four independent UARTs with built-in IrDA® encoders/decoders and three SPI modules.
- **Analog Features:** All members of the PIC24FJ256GB210 family include a 10-bit A/D Converter (ADC) module and a triple comparator module. The ADC module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and faster sampling speeds. The comparator module includes three analog comparators that are configurable for a wide range of operations.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ256GB210 family include the CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** There are general purpose I/O ports, which can be configured for parallel data communications. In this mode, the device can be master or slave on the communication bus. 4-bit, 8-bit and 16-bit data transfers, with up to 23 external address lines, are supported in Master modes.
- **Real-Time Clock and Calendar: (RTCC)** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.4 Details on Individual Family Members

Devices in the PIC24FJ256GB210 family are available in 64-pin and 100-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in seven ways:

1. Flash program memory (128 Kbytes for PIC24FJ128GB2XX devices and 256 Kbytes for PIC24FJ256GB2XX devices).
2. Available I/O pins and ports (52 pins on 6 ports for PIC24FJXXXGB2XX devices and 84 pins on 7 ports for PIC24FJXXXGB2XX devices).
3. Available Interrupt-on-Change Notification (ICN) inputs (52 on PIC24FJXXXGB2XX devices and 84 on PIC24FJXXXGB2XX devices).
4. Available remappable pins (29 pins on PIC24FJXXXGB2XX devices and 44 pins on PIC24FJXXXGB2XX devices).
5. Analog channels for ADC (16 channels for PIC24FJXXXGB206 devices and 24 channels for PIC24FJXXXGB2XX devices).

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

A list of the pin features available on the PIC24FJ256GB210 family devices, sorted by function, is shown in Table 1-1. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ256GB210 FAMILY: 64-PIN

Features	PIC24FJ128GB206	PIC24FJ256GB206
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	128K	256K
Program Memory (instructions)	44,032	87,552
Data Memory (bytes)	96K	
Interrupt Sources (soft vectors/NMI traps)	65 (61/4)	
I/O Ports	Ports B, C, D, E, F, G	
Total I/O Pins	52	
Remappable Pins	29 (28 I/O, 1 Input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture Channels	9(1)	
Output Compare/PWM Channels	9(1)	
Input Change Notification Interrupt	52	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	3(1)	
I^2C™	3	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
10-Bit Analog-to-Digital Converter (ADC) Module (input channels)	16	
Analog Comparators	3	
CTMU Interface	Yes	
USB OTG	Yes	
Resets (and Delays)	POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	64-Pin TQFP and QFN	

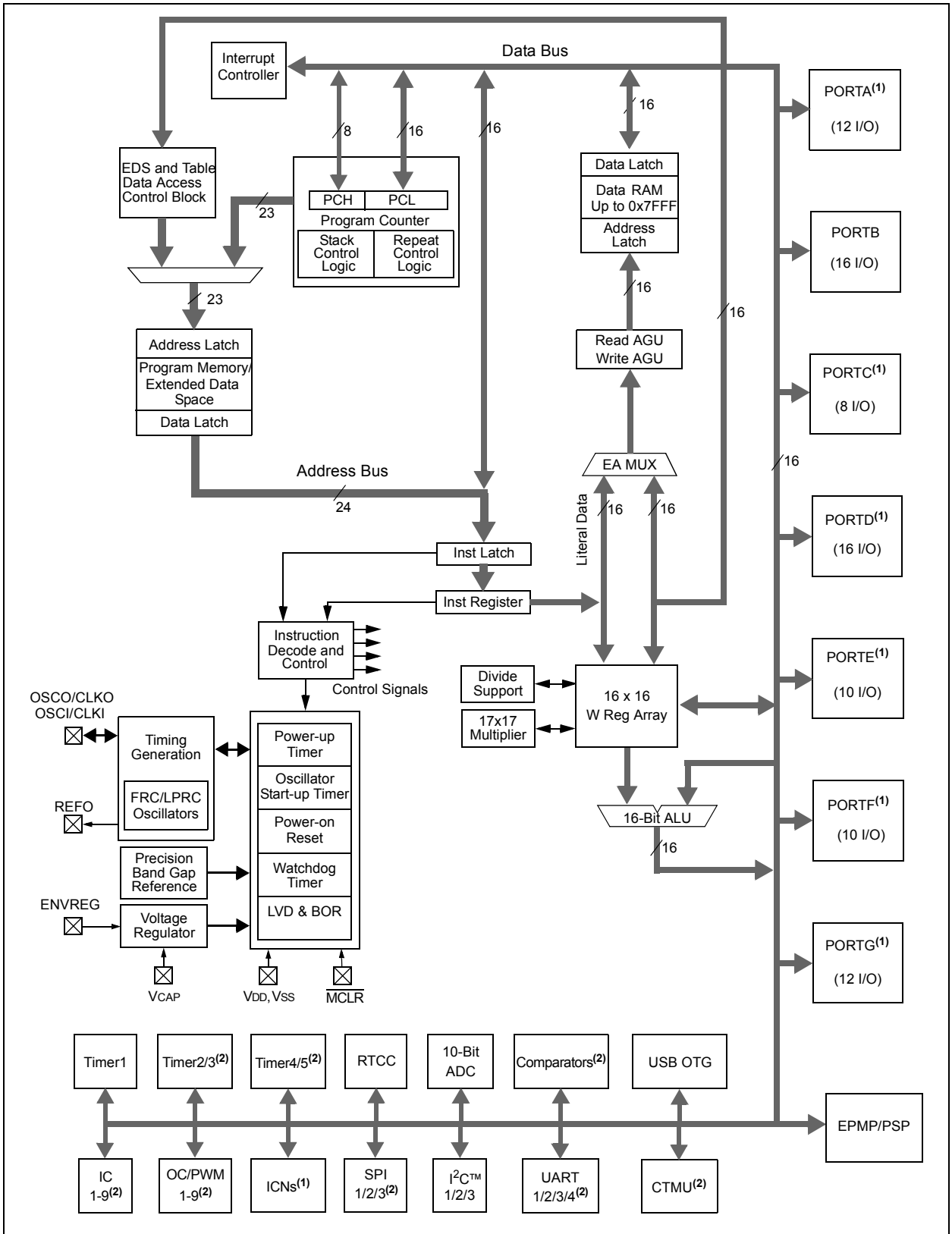
Note 1: Peripherals are accessible through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ256GB210 FAMILY: 100-PIN DEVICES

Features	PIC24FJ128GB210	PIC24FJ256GB210
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	128K	256K
Program Memory (instructions)	44,032	87,552
Data Memory (bytes)	96K	
Interrupt Sources (soft vectors/NMI traps)	65 (61/4)	
I/O Ports	Ports A, B, C, D, E, F, G	
Total I/O Pins	84	
Remappable Pins	44 (32 I/O, 12 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture Channels	9(1)	
Output Compare/PWM Channels	9(1)	
Input Change Notification Interrupt	84	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	3(1)	
I^2C™	3	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
10-Bit Analog-to-Digital Converter (ADC) Module (input channels)	24	
Analog Comparators	3	
CTMU Interface	Yes	
USB OTG	Yes	
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	100-Pin TQFP and 121-Pin BGA	

Note 1: Peripherals are accessible through remappable pins.

FIGURE 1-1: PIC24FJ256GB210 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-1 for specific implementations by pin count.
2: These peripheral I/Os are only accessible through remappable pins.

TABLE 1-3: PIC24FJ256GB210 FAMILY PINOUT DESCRIPTIONS

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
AN0	16	25	K2	I	ANA	A/D Analog Inputs.
AN1	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	21	32	K4	I	ANA	
AN9	22	33	L4	I	ANA	
AN10	23	34	L5	I	ANA	
AN11	24	35	J5	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	—	10	E3	I	ANA	
AN18	—	11	F4	I	ANA	
AN19	—	12	F2	I	ANA	
AN20	—	14	F3	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	B5	I	ANA	
AN23	—	91	C5	I	ANA	
AVDD	19	30	J4	P	—	Positive Supply for Analog modules.
AVSS	20	31	L3	P	—	Ground Reference for Analog modules.
C1INA	11	20	H1	I	ANA	Comparator 1 Input A.
C1INB	12	21	H2	I	ANA	Comparator 1 Input B.
C1INC	5	11	F4	I	ANA	Comparator 1 Input C.
C1IND	4	10	E3	I	ANA	Comparator 1 Input D.
C2INA	13	22	J1	I	ANA	Comparator 2 Input A.
C2INB	14	23	J2	I	ANA	Comparator 2 Input B.
C2INC	8	14	F3	I	ANA	Comparator 2 Input C.
C2IND	6	12	F2	I	ANA	Comparator 2 Input D.
C3INA	55	84	C7	I	ANA	Comparator 3 Input A.
C3INB	54	83	D7	I	ANA	Comparator 3 Input B.
C3INC	48	74	B11	I	ANA	Comparator 3 Input C.
C3IND	47	73	C10	I	ANA	Comparator 3 Input D.
CLKI	39	63	F9	I	ST	Main Clock Input Connection.
CLKO	40	64	F11	O	—	System Clock Output.

Legend: TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I^2C™ = I^2C/SMBus input buffer

Note 1: The alternate EPMP pins are selected when the $\overline{\text{ALTPMP}}$ (CW3<12>) bit is programmed to '0'.

2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.

3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.

4: The alternate VREF pins selected when the $\overline{\text{ALTVREF}}$ (CW1<5>) bit is programmed to '0'.

TABLE 1-3: PIC24FJ256GB210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
CN0	48	74	B11	I	ST	Interrupt-on-Change Inputs.
CN1	47	73	C10	I	ST	
CN2	16	25	K2	I	ST	
CN3	15	24	K1	I	ST	
CN4	14	23	J2	I	ST	
CN5	13	22	J1	I	ST	
CN6	12	21	H2	I	ST	
CN7	11	20	H1	I	ST	
CN8	4	10	E3	I	ST	
CN9	5	11	F4	I	ST	
CN10	6	12	F2	I	ST	
CN11	8	14	F3	I	ST	
CN12	30	44	L8	I	ST	
CN13	52	81	C8	I	ST	
CN14	53	82	B8	I	ST	
CN15	54	83	D7	I	ST	
CN16	55	84	C7	I	ST	
CN17	31	49	L10	I	ST	
CN18	32	50	L11	I	ST	
CN19	—	80	D8	I	ST	
CN20	—	47	L9	I	ST	
CN21	—	48	K9	I	ST	
CN22	40	64	F11	I	ST	
CN23	39	63	F9	I	ST	
CN24	17	26	L1	I	ST	
CN25	18	27	J3	I	ST	
CN26	21	32	K4	I	ST	
CN27	22	33	L4	I	ST	
CN28	23	34	L5	I	ST	
CN29	24	35	J5	I	ST	
CN30	27	41	J7	I	ST	
CN31	28	42	L7	I	ST	
CN32	29	43	K7	I	ST	
CN33	—	17	G3	I	ST	
CN34	—	38	J6	I	ST	
CN35	—	58	H11	I	ST	
CN36	—	59	G10	I	ST	
CN37	—	60	G11	I	ST	
CN38	—	61	G9	I	ST	
CN39	—	91	C5	I	ST	

Legend: TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I^2C™ = I^2C/SMBus input buffer

Note 1: The alternate EPMP pins are selected when the $\overline{\text{ALTPMP}}$ (CW3<12>) bit is programmed to '0'.

2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.

3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.

4: The alternate VREF pins selected when the $\overline{\text{ALTVREF}}$ (CW1<5>) bit is programmed to '0'.

TABLE 1-3: PIC24FJ256GB210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
CN40	—	92	B5	I	ST	Interrupt-on-Change Inputs.
CN41	—	28	L2	I	ST	
CN42	—	29	K3	I	ST	
CN43	—	66	E11	I	ST	
CN44	—	67	E8	I	ST	
CN45	—	6	D1	I	ST	
CN46	—	7	E4	I	ST	
CN47	—	8	E2	I	ST	
CN48	—	9	E1	I	ST	
CN49	46	72	D9	I	ST	
CN50	49	76	A11	I	ST	
CN51	50	77	A10	I	ST	
CN52	51	78	B9	I	ST	
CN53	42	68	E9	I	ST	
CN54	43	69	E10	I	ST	
CN55	44	70	D11	I	ST	
CN56	45	71	C11	I	ST	
CN57	—	79	A9	I	ST	
CN58	60	93	A4	I	ST	
CN59	61	94	B4	I	ST	
CN60	62	98	B3	I	ST	
CN61	63	99	A2	I	ST	
CN62	64	100	A1	I	ST	
CN63	1	3	D3	I	ST	
CN64	2	4	C1	I	ST	
CN65	3	5	D2	I	ST	
CN66	—	18	G1	I	ST	
CN67	—	19	G2	I	ST	
CN68	58	87	B6	I	ST	
CN69	59	88	A6	I	ST	
CN70	—	52	K11	I	ST	
CN71	33	51	K10	I	ST	
CN73	—	54	H8	I	ST	
CN74	—	53	J10	I	ST	
CN75	—	40	K6	I	ST	
CN76	—	39	L6	I	ST	
CN77	—	90	A5	I	ST	
CN78	—	89	E6	I	ST	
CN79	—	96	C3	I	ST	
CN80	—	97	A3	I	ST	

Legend: TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I^2C™ = I^2C/SMBus input buffer

Note 1: The alternate EPMP pins are selected when the $\overline{\text{ALTPMP}}$ (CW3<12>) bit is programmed to '0'.

2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.

3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.

4: The alternate V_{REF} pins selected when the $\overline{\text{ALTVREF}}$ (CW1<5>) bit is programmed to '0'.

TABLE 1-3: PIC24FJ256GB210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
CN81	—	95	C4	I	ST	Interrupt-on-Change Inputs.
CN82	—	1	B2	I	ST	
CN83	37	57	H10	I	ST	
CN84	36	56	J11	I	ST	
CTEDG1	28	42	L7	I	ANA	CTMU External Edge Input 1.
CTEDG2	27	41	J7	I	ANA	CTMU External Edge Input 2.
CTPLS	29	43	K7	O	—	CTMU Pulse Output.
CVREF	23	34	L5	O	—	Comparator Voltage Reference Output.
D+	37	57	H10	I/O	—	USB Differential Plus Line (internal transceiver).
D-	36	56	J11	I/O	—	USB Differential Minus Line (internal transceiver).
DMH	46	72	D9	O	—	D- External Pull-up Control Output.
DMLN	42	68	E9	O	—	D- External Pull-down Control Output.
DPH	50	77	A10	O	—	D+ External Pull-up Control Output.
DPLN	43	69	E10	O	—	D+ External Pull-down Control Output.
ENVREG	57	86	J7	I	ST	Voltage Regulator Enable.
INT0	46	72	D9	I	ST	External Interrupt Input.
$\overline{MCLR}$	7	13	F1	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	39	63	F9	I	ANA	Main Oscillator Input Connection.
OSCO	40	64	F11	O	ANA	Main Oscillator Output Connection.
PGEC1	15	24	K1	I/O	ST	In-Circuit Debugger/Emulator/ICSP™ Programming Clock 1.
PGED1	16	25	K2	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 1.
PGEC2	17	26	L1	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock 2.
PGED2	18	27	J3	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 2.
PGEC3	11	20	H1	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock 3.
PGED3	12	21	H2	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 3.

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

Note 1: The alternate EPMP pins are selected when the $\overline{ALTPMP}$ (CW3<12>) bit is programmed to '0'.

2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.

3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.

4: The alternate VREF pins selected when the $\overline{ALTVREF}$ (CW1<5>) bit is programmed to '0'.

TABLE 1-3: PIC24FJ256GB210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
PMA0	30	44	L8	I/O	ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	43	K7	I/O	ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	14	F3	O	—	Parallel Master Port Address bits<22:2>.
PMA3	6	12, 60(1)	F2, G11(1)	O	—	
PMA4	5	11,59(1)	F4,G10(1)	O	—	
PMA5	4	10,40(1)	E3,K6(1)	O	—	
PMA6	16	29	K3	O	—	
PMA7	22	28	L2	O	—	
PMA8	32	50	L11	O	—	
PMA9	31	49	L10	O	—	
PMA10	28	42	L7	O	—	
PMA11	27	41	J7	O	—	
PMA12	24	35	J5	O	—	
PMA13	23	34	L5	O	—	
PMA14	45	71	C11	O	—	
PMA15	44	70	D11	O	—	
PMA16	—	95	C4	O	—	
PMA17	—	92	B5	O	—	
PMA18	—	40,10(1)	K6,E3(1)	O	—	
PMA19	—	19	G2	O	—	
PMA20	—	59, 11(1)	G10, F4(1)	O	—	
PMA21	—	60,12(1)	G11,F2(1)	O	—	
PMA22	—	66,9(1)	E11,E1(1)	O	—	
PMACK1	50	77	A10	I	ST/TTL	Parallel Master Port Acknowledge Input 1.
PMACK2	43	69	E10	I	ST/TTL	Parallel Master Port Acknowledge Input 2.
PMALL	30	44	L8	O	—	Parallel Master Port Lower Address Latch Strobe.
PMALH	29	43	K7	O	—	Parallel Master Port Higher Address Latch Strobe.
PMALU	—	14	F3	O	—	Parallel Master Port Upper Address Latch Strobe.
PMBE0	51	78	B9	O	—	Parallel Master Port Byte Enable Strobe 0.
PMBE1	—	67	E8	O	—	Parallel Master Port Byte Enable Strobe 1.
PMCS1	45	71(3),18	C11(3),G1	I/O	ST/TTL	Parallel Master Port Chip Select Strobe 1.
PMCS2	44	70(2),9, 66(1)	D11(2),E1, E11(1)	O	—	Parallel Master Port Chip Select Strobe 2.

Legend: TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I^2C™ = I^2C/SMBus input buffer

Note 1: The alternate EPMP pins are selected when the $\overline{\text{ALTPMP}}$ (CW3<12>) bit is programmed to '0'.

2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.

3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.

4: The alternate VREF pins selected when the $\overline{\text{ALTVREF}}$ (CW1<5>) bit is programmed to '0'.

TABLE 1-3: PIC24FJ256GB210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
PMD0	60	93	A4	I/O	ST/TTL	Parallel Master Port Data bits<15:0>.
PMD1	61	94	B4	I/O	ST/TTL	
PMD2	62	98	B3	I/O	ST/TTL	
PMD3	63	99	A2	I/O	ST/TTL	
PMD4	64	100	A1	I/O	ST/TTL	
PMD5	1	3	D3	I/O	ST/TTL	
PMD6	2	4	C1	I/O	ST/TTL	
PMD7	3	5	D2	I/O	ST/TTL	
PMD8	—	90	A5	I/O	ST/TTL	
PMD9	—	89	E6	I/O	ST/TTL	
PMD10	—	88	A6	I/O	ST/TTL	
PMD11	—	87	B6	I/O	ST/TTL	
PMD12	—	79	A9	I/O	ST/TTL	
PMD13	—	80	D8	I/O	ST/TTL	
PMD14	—	83	D7	I/O	ST/TTL	
PMD15	—	84	C7	I/O	ST/TTL	
PMRD	53	82	B8	I/O	ST/TTL	Parallel Master Port Read Strobe.
PMWR	52	81	C8	I/O	ST/TTL	Parallel Master Port Write Strobe.
RA0	—	17	G3	I/O	ST	PORTA Digital I/O.
RA1	—	38	J6	I/O	ST	
RA2	—	58	H11	I/O	ST	
RA3	—	59	G10	I/O	ST	
RA4	—	60	G11	I/O	ST	
RA5	—	61	G9	I/O	ST	
RA6	—	91	C5	I/O	ST	
RA7	—	92	B5	I/O	ST	
RA9	—	28	L2	I/O	ST	
RA10	—	29	K3	I/O	ST	
RA14	—	66	E11	I/O	ST	
RA15	—	67	E8	I/O	ST	

Legend: TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I^2C™ = I^2C/SMBus input buffer

Note 1: The alternate EPMP pins are selected when the $\overline{\text{ALTPMP}}$ (CW3<12>) bit is programmed to '0'.

2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.

3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.

4: The alternate V_{REF} pins selected when the $\overline{\text{ALTVREF}}$ (CW1<5>) bit is programmed to '0'.