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PIC24FJ1024GA610/GB610 FAMILY

16-Bit Microcontrollers with Large, Dual Partition Flash Program Memory and USB On-The-Go (OTG)

High-Performance CPU

- Modified Harvard Architecture
- Largest Program Memory Available for PIC24 (1024 Kbytes) for the Most Complex Applications
- 32 Kbytes SRAM for All Part Variants
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Fast RC Internal Oscillator:
  - 96 MHz PLL option
  - Multiple clock divide options
  - Run-time self-calibration capability for maintaining better than ±0.20% accuracy
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16-Bit x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory

Universal Serial Bus Features

- USB v2.0 On-The-Go (OTG) Compliant
- Dual Role Capable – Can Act as Either Host or Peripheral
- Low-Speed (1.5 Mb/s) and Full-Speed (12 Mb/s) USB Operation in Host mode
- Full-Speed USB Operation in Device mode
- High-Precision PLL for USB
- USB Device mode Operation from FRC Oscillator – No Crystal Oscillator Required
- Supports up to 32 Endpoints (16 bidirectional):
  - USB module can use any RAM location on the device as USB endpoint buffers
- On-Chip USB Transceiver with Interface for Off-Chip USB Transceiver
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- On-Chip Pull-up and Pull-Down Resistors

Analog Features

- 10/12-Bit, up to 24-Channel Analog-to-Digital (A/D) Converter:
  - 12-bit conversion rate of 200 ksps
  - Auto-scan and threshold compare features
  - Conversion available during Sleep
- Three Rail-to-Rail, Enhanced Analog Comparators with Programmable Input/Output Configuration
- Charge Time Measurement Unit (CTMU):
  - Used for capacitive touch sensing, up to 24 channels
  - Time measurement down to 100 ps resolution

Low-Power Features

- Sleep and Idle modes Selectively Shut Down Peripherals and/or Core for Substantial Power Reduction and Fast Wake-up
- Doze mode Allows CPU to Run at a Lower Clock Speed than Peripherals
- Alternate Clock modes Allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction
- Wide Range Digitally Controlled Oscillator (DCO) for Fast Start-up and Low-Power Operation

Special Microcontroller Features

- Large, Dual Partition Flash Program Array:
  - Capable of holding two independent software applications, including bootloader
  - Permits simultaneous programming of one partition while executing application code from the other
  - Allows run-time switching between Active Partitions
- 10,000 Erase/Write Cycle Endurance, Typical
- Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Supply Voltage Range of 2.0V to 3.6V
- Operating Ambient Temperature Range of -40°C to +85°C
- On-Chip Voltage Regulators (1.8V) for Low-Power Operation
- Programmable Reference Clock Output
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via 2 Pins
- JTAG Boundary Scan Support
- Fail-Safe Clock Monitor Operation:
  - Detects clock failure and switches to on-chip, low-power RC Oscillator
- Power-on Reset (POR), Brown-out Reset (BOR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable High/Low-Voltage Detect (HLVD)
- Flexible Watchdog Timer (WDT) with its Own RC Oscillator for Reliable Operation

Peripheral Features

- Peripheral Pin Select (PPS) – Allows Independent I/O Mapping of Many Peripherals
- Up to 5 External Interrupt Sources
- Configurable Interrupt-on-Change on All I/O Pins:
  - Each pin is independently configurable for rising edge or falling edge change detection
- Eight-Channel DMA Supports All Peripheral modules:
  - Minimizes CPU overhead and increases data throughput
- Five 16-Bit Timers/Counters with Prescalers:
  - Can be paired as 32-bit timers/counters
- Six Input Capture modules, Each with a Dedicated 16-Bit Timer
- Six Output Compare/PWM modules, Each with a Dedicated 16-Bit Timer
- Four Single Output CCPs (SCCPs) and Three Multiple Output CCPs (MCCPs):
  - Independent 16/32-bit time base for each module
  - Internal time base and period registers
  - Legacy PIC24F Capture and Compare modes (16 and 32-bit)
  - Special Variable Frequency Pulse and Brushless DC Motor Output modes
- Enhanced Parallel Master/Slave Port (EPMP/EPSP)
- Hardware Real-Time Clock/Calendar (RTCC) with Timestamping
- Three 3-Wire/4-Wire SPI modules:
  - Support 4 Frame modes
  - 8-level FIFO buffer
  - Support I^2S operation
- Three I^2C modules Support Multi-Master/Slave mode and 7-Bit/10-Bit Addressing
- Six UART modules:
  - Support RS-485, RS-232 and LIN/J2602
  - On-chip hardware encoder/decoder for IrDA®
  - Auto-wake-up on Auto-Baud Detect (ABD)
  - 4-level deep FIFO buffer
- Programmable 32-Bit Cyclic Redundancy Check (CRC) Generator
- Four Configurable Logic Cells (CLCs):
  - Two inputs and one output, all mappable to peripherals or I/O pins
  - AND/OR/XOR logic and D/JK flip-flop functions
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Configurable Open-Drain Outputs on Digital I/O Pins
- 5.5V Tolerant Inputs on Multiple I/O Pins

PIC24FJ1024GA610/GB610 FAMILY PRODUCT FAMILIES

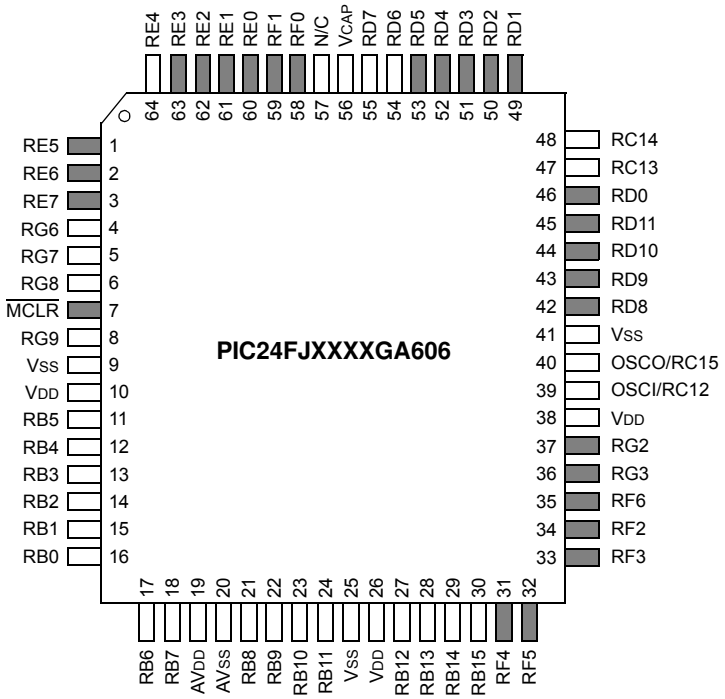
The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. Their pinout diagrams appear on the following pages.

TABLE 1: PIC24FJ1024GA610/GB610 GENERAL PURPOSE FAMILIES

Device	Memory		Pins		Analog			Digital								RTCC	USB OTG
	Program (bytes)	Data (bytes)	Total	I/O	10/12-Bit A/D (ch)	Comparator	CTMU	16/32-Bit Timer	IC/OC/PWM	MCCP/SCCP	I^2C	SPI	UART w/IrDA®	EPMP/EPSP	CLC		
PIC24FJ128GA606	128K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ256GA606	256K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ512GA606	512K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ1024GA606	1024K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ128GA610	128K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ256GA610	256K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ512GA610	512K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ1024GA610	1024K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	N
PIC24FJ128GB606	128K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y
PIC24FJ256GB606	256K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y
PIC24FJ512GB606	512K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y
PIC24FJ1024GB606	1024K	32K	64	53	16	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y
PIC24FJ128GB610	128K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y
PIC24FJ256GB610	256K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y
PIC24FJ512GB610	512K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y
PIC24FJ1024GB610	1024K	32K	100	85	24	3	Y	5/2	6/6	3/4	3	3	6/2	Y	4	Y	Y

Pin Diagrams(2)

64-Pin TQFP
64-Pin QFN(1)



Legend: See Table 2 for a complete description of pin functions. Pinouts are subject to change.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.
2: Gray shading indicates 5.5V tolerant input pins.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA606)

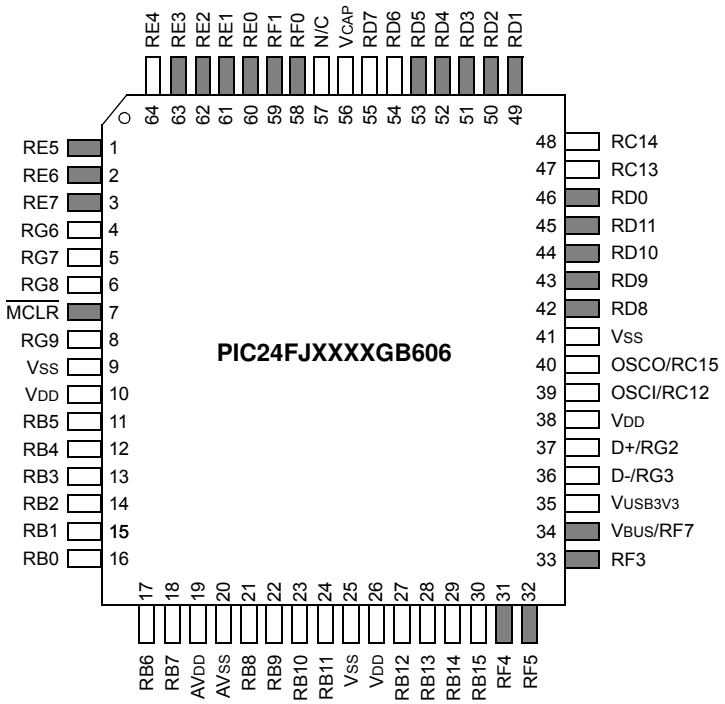
Pin	Function	Pin	Function
1	IC4/CTED4/PMD5/RE5	33	**RP16**/RF3
2	SCL3/IC5/PMD6/RE6	34	**RP30**/RF2
3	SDA3/IC6/PMD7/RE7	35	INT0/RF6
4	C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	36	SDA1/RG3
5	C1INC/**RP26**/OCM1B/PMA4/RG7	37	SCL1/RG2
6	C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/RC12
8	C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	40	OSCO/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
11	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	43	**RP4**/PMACK2/RD9
12	PGED3/AN4/C1INB/**RP28**/OCM3B/RB4	44	**RP3**/PMA15/PMCS2/RD10
13	AN3/C2INA/RB3	45	**RP12**/PMA14/PMCS1/RD11
14	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	46	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/RD0
15	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	47	SOSCI/C3IND/RC13
16	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/PMA6/RB0	48	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
17	PGEC2/AN6/**RP6**/RB6	49	**RP24**/U5TX/ICM4/RD1
18	PGED2/AN7/**RP7**/U6TX/RB7	50	**RP23**/PMACK1/RD2
19	AVDD	51	**RP22**/ICM7/PMBE0/RD3
20	AVSS	52	**RP25**/PMWR/PMENB/RD4
21	AN8/**RP8**/PWRGT/RB8	53	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
22	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/RB9	54	C3INB/U5RX/OC4/RD6
23	TMS/CVREF/AN10/PMA13/RB10	55	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/RD7
24	TDO/AN11/REFI/PMA12/RB11	56	VCAP
25	VSS	57	N/C
26	VDD	58	$\overline{\text{U5CTS}}$/OC6/RF0
27	TCK/AN12/U6RX/CTED2/PMA11/RB12	59	RF1
28	TDI/AN13/CTED1/PMA10/RB13	60	PMD0/RE0
29	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	61	PMD1/RE1
30	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	62	PMD2/RE2
31	**RP10**/SDA2/PMA9/RF4	63	CTED9/PMD3/RE3
32	**RP17**/SCL2/PMA8/RF5	64	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams[2] (Continued)

64-Pin TQFP
64-Pin QFN[1]



Legend: See Table 3 for a complete description of pin functions. Pinouts are subject to change.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.
2: Gray shading indicates 5.5V tolerant input pins.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB606)

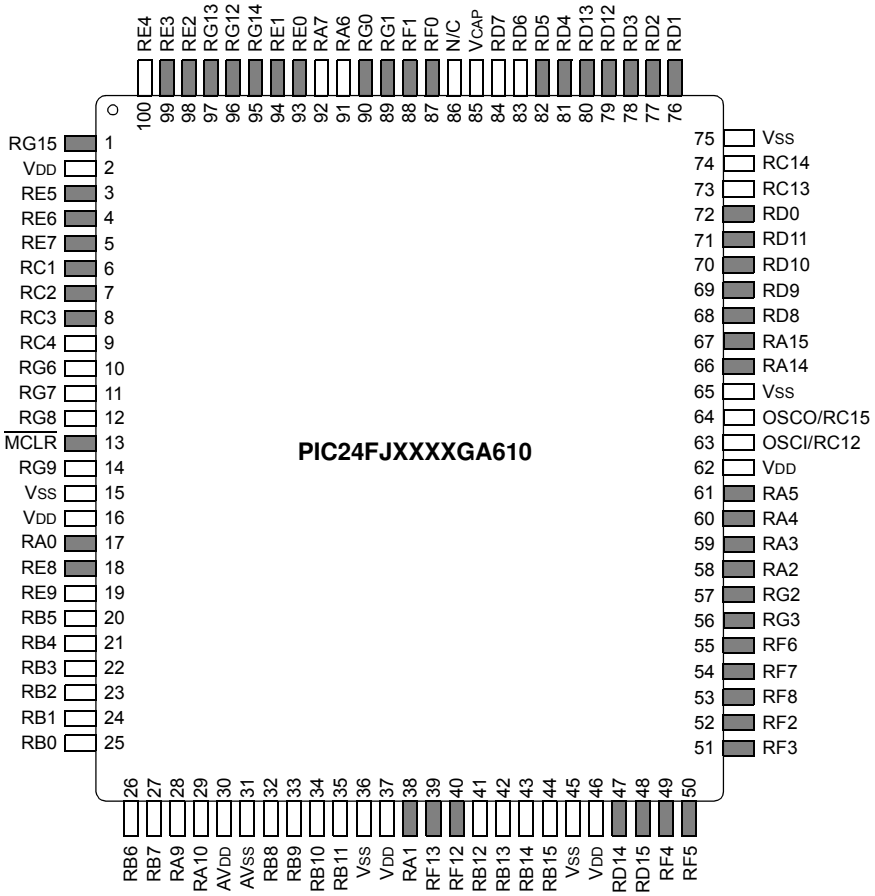
Pin	Function	Pin	Function
1	IC4/CTED4/PMD5/RE5	33	**RP16**/USBID/RF3
2	SCL3/IC5/PMD6/RE6	34	VBUS/RF7
3	SDA3/IC6/PMD7/RE7	35	VUSB3V3
4	C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	36	D-/RG3
5	C1INC/**RP26**/OCM1B/PMA4/RG7	37	D+/RG2
6	C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/RC12
8	C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	40	OSCO/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
11	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	43	**RP4**/SDA1/PMACK2/RD9
12	PGED3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/OCM3B/RB4	44	**RP3**/SCL1/PMA15/PMCS2/RD10
13	AN3/C2INA/RB3	45	**RP12**/PMA14/PMCS1/RD11
14	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	46	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/RD0
15	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	47	SOSCI/C3IND/RC13
16	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/PMA6/RB0	48	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
17	PGEC2/AN6/**RP6**/RB6	49	**RP24**/U5TX/ICM4/RD1
18	PGED2/AN7/**RP7**/U6TX/RB7	50	**RP23**/PMACK1/RD2
19	AVDD	51	**RP22**/ICM7/PMBE0/RD3
20	AVSS	52	**RP25**/PMWR/PMENB/RD4
21	AN8/**RP8**/PWRGT/RB8	53	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
22	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/RB9	54	C3INB/U5RX/OC4/RD6
23	TMS/CVREF/AN10/PMA13/RB10	55	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/RD7
24	TDO/AN11/REFI/PMA12/RB11	56	VCAP
25	VSS	57	N/C
26	VDD	58	$\overline{\text{U5CTS}}$/OC6/RF0
27	TCK/AN12/U6RX/CTED2/PMA11/RB12	59	RF1
28	TDI/AN13/CTED1/PMA10/RB13	60	PMD0/RE0
29	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	61	PMD1/RE1
30	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	62	PMD2/RE2
31	**RP10**/SDA2/PMA9/RF4	63	CTED9/PMD3/RE3
32	**RP17**/SCL2/PMA8/RF5	64	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams[1] (Continued)

100-Pin TQFP



Legend: See Table 4 for a complete description of pin functions. Pinouts are subject to change.
Note 1: Gray shading indicates 5.5V tolerant input pins.

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA610 TQFP)

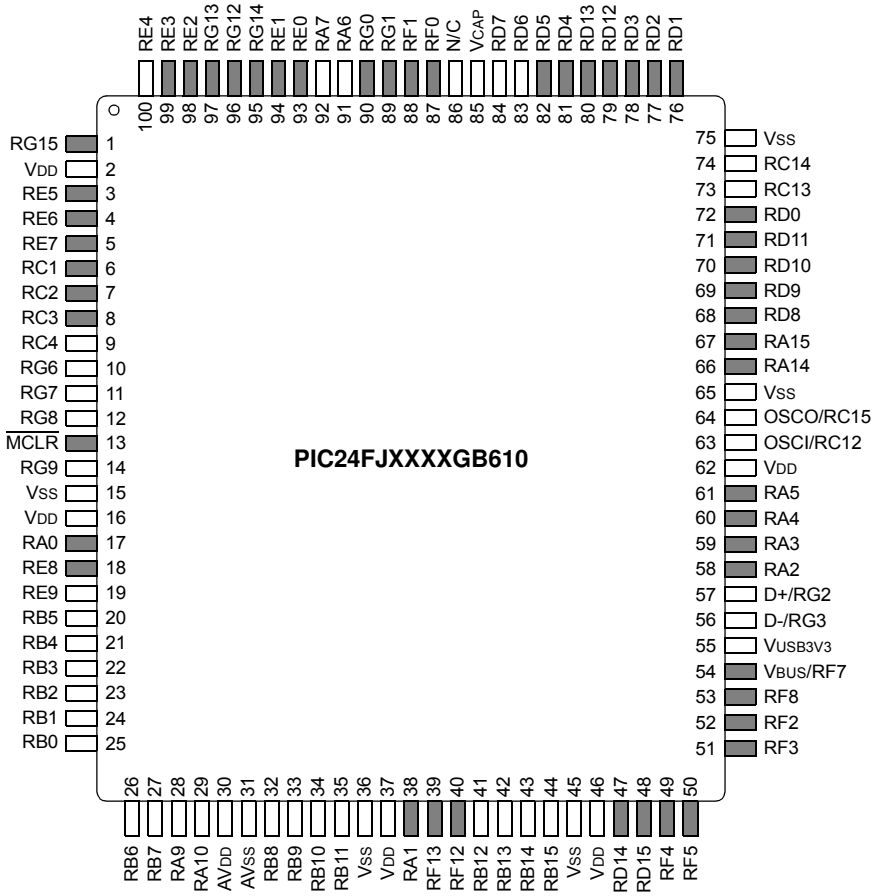
Pin	Function	Pin	Function
1	OCM1C/CTED3/RG15	51	**RP16**/RF3
2	VDD	52	**RP30**/RF2
3	IC4/CTED4/PMD5/RE5	53	**RP15**/RF8
4	SCL3/IC5/PMD6/RE6	54	RF7
5	SDA3/IC6/PMD7/RE7	55	INT0/RF6
6	**RPI38**/OCM1D/RC1	56	SDA1/RG3
7	**RPI39**/OCM2C/RC2	57	SCL1/RG2
8	**RPI40**/OCM2D/RC3	58	PMPCS1/SCL2/RA2
9	AN16/**RPI41**/OCM3C/PMCS2/RC4	59	SDA2/PMA20/RA3
10	AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	60	TDI/PMA21/RA4
11	AN18/C1INC/**RP26**/OCM1B/PMA4/RG7	61	TDO/RA5
12	AN19/C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/RC12
14	AN20/C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	64	OSCO/CLKO/RC15
15	VSS	65	VSS
16	VDD	66	**RPI36**/PMA22/RA14
17	TMS/OCM3D/RA0	67	**RPI35**/PMBE1/RA15
18	**RPI33**/PMCS1/RE8	68	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
19	AN21/**RPI34**/PMA19/RE9	69	**RP4**/PMACK2/RD9
20	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	70	**RP3**/PMA15/PMCS2/RD10
21	PGED3/AN4/C1INB/**RP28**/OCM3B/RB4	71	**RP12**/PMA14/PMCS1/RD11
22	AN3/C2INA/RB3	72	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/RD0
23	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	73	SOSCI/C3IND/RC13
24	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	74	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
25	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	75	VSS
26	PGEC2/AN6/**RP6**/RB6	76	**RP24**/U5TX/ICM4/RD1
27	PGED2/AN7/**RP7**/U6TX/RB7	77	**RP23**/PMACK1/RD2
28	CVREF-/VREF-/PMA7/RA9	78	**RP22**/ICM7/PMBE0/RD3
29	CVREF+/VREF+/PMA6/RA10	79	**RPI42**/OCM3E/PMD12/RD12
30	AVDD	80	OCM3F/PMD13/RD13
31	AVSS	81	**RP25**/PMWR/PMENB/RD4
32	AN8/**RP8**/PWRGT/RB8	82	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
33	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9	83	C3INB/U5RX/OC4/PMD14/RD6
34	CVREF/AN10/PMA13/RB10	84	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/RD7
35	AN11/REFI/PMA12/RB11	85	VCAP
36	VSS	86	N/C
37	VDD	87	$\overline{\text{U5CTS}}$/OC6/PMD11/RF0
38	TCK/RA1	88	PMD10/RF1
39	**RP31**/RF13	89	PMD9/RG1
40	**RPI32**/CTED7/PMA18/RF12	90	PMD8/RG0
41	AN12/U6RX/CTED2/PMA11/RB12	91	AN23/OCM1E/RA6
42	AN13/CTED1/PMA10/RB13	92	AN22/OCM1F/PMA17/RA7
43	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	93	PMD0/RE0
44	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	94	PMD1/RE1
45	VSS	95	CTED11/PMA16/RG14
46	VDD	96	OCM2E/RG12
47	**RPI43**/RD14	97	OCM2F/CTED10/RG13
48	**RP5**/RD15	98	PMD2/RE2
49	**RP10**/PMA9/RF4	99	CTED9/PMD3/RE3
50	**RP17**/PMA8/RF5	100	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams[1] (Continued)

100-Pin TQFP



Legend: See Table 5 for a complete description of pin functions. Pinouts are subject to change.
Note 1: Gray shading indicates 5.5V tolerant input pins.

TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB610 TQFP)

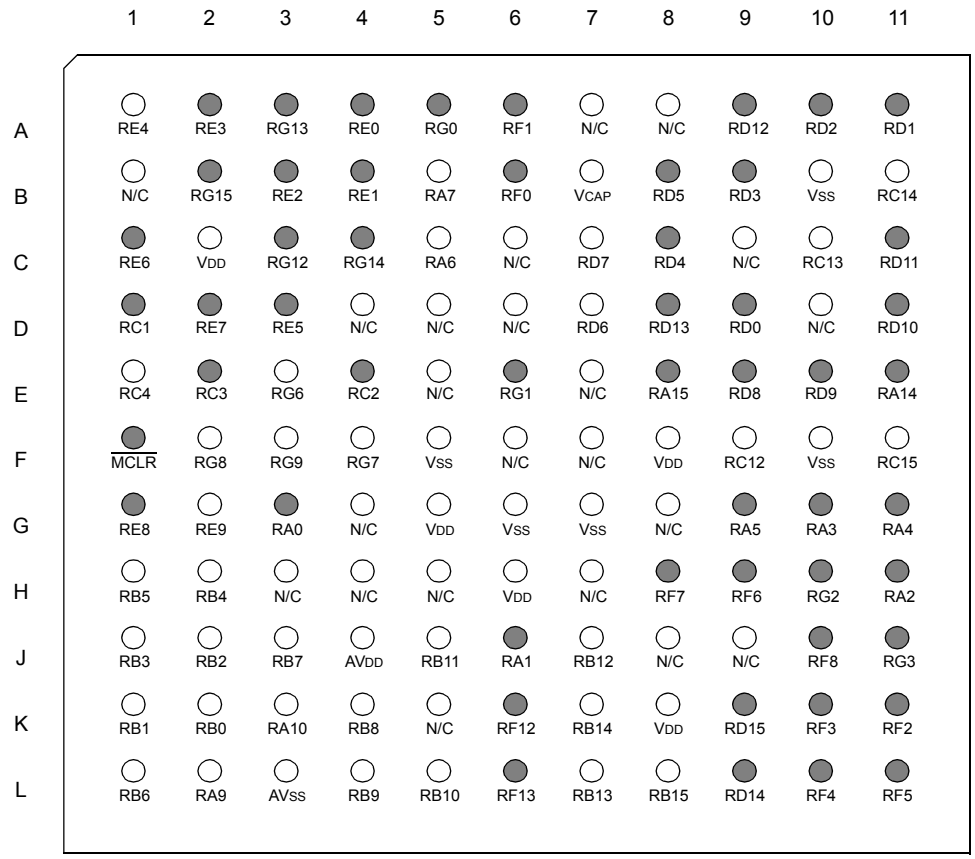
Pin	Function	Pin	Function
1	OCM1C/CTED3/RG15	51	**RP16**/USBID/RF3
2	VDD	52	**RP30**/RF2
3	IC4/CTED4/PMD5/RE5	53	**RP15**/RF8
4	SCL3/IC5/PMD6/RE6	54	VBUS/RF7
5	SDA3/IC6/PMD7/RE7	55	VUSB3V3
6	**RPI38**/OCM1D/RC1	56	D-/RG3
7	**RPI39**/OCM2C/RC2	57	D+/RG2
8	**RPI40**/OCM2D/RC3	58	PMPCS1/SCL2/RA2
9	AN16/**RPI41**/OCM3C/PMCS2/RC4	59	SDA2/PMA20/RA3
10	AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	60	TDI/PMA21/RA4
11	AN18/C1INC/**RP26**/OCM1B/PMA4/RG7	61	TDO/RA5
12	AN19/C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/RC12
14	AN20/C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	64	OSCO/CLKO/RC15
15	VSS	65	VSS
16	VDD	66	**RPI36**/SCL1/PMA22/RA14
17	TMS/OCM3D/RA0	67	**RPI35**/SDA1/PMBE1/RA15
18	**RPI33**/PMCS1/RE8	68	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
19	AN21/**RPI34**/PMA19/RE9	69	**RP4**/PMACK2/RD9
20	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	70	**RP3**/PMA15/PMCS2/RD10
21	PGED3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/OCM3B/RB4	71	**RP12**/PMA14/PMCS1/RD11
22	AN3/C2INA/RB3	72	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/RD0
23	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	73	SOSCI/C3IND/RC13
24	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	74	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
25	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	75	VSS
26	PGEC2/AN6/**RP6**/RB6	76	**RP24**/U5TX/ICM4/RD1
27	PGED2/AN7/**RP7**/U6TX/RB7	77	**RP23**/PMACK1/RD2
28	CVREF-/VREF-/PMA7/RA9	78	**RP22**/ICM7/PMBE0/RD3
29	CVREF+/VREF+/PMA6/RA10	79	**RPI42**/OCM3E/PMD12/RD12
30	AVDD	80	OCM3F/PMD13/RD13
31	AVSS	81	**RP25**/PMWR/PMENB/RD4
32	AN8/**RP8**/PWRGT/RB8	82	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
33	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9	83	C3INB/U5RX/OC4/PMD14/RD6
34	CVREF/AN10/PMA13/RB10	84	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/RD7
35	AN11/REFI/PMA12/RB11	85	VCAP
36	VSS	86	N/C
37	VDD	87	$\overline{\text{U5CTS}}$/OC6/PMD11/RF0
38	TCK/RA1	88	PMD10/RF1
39	**RP31**/RF13	89	PMD9/RG1
40	**RPI32**/CTED7/PMA18/RF12	90	PMD8/RG0
41	AN12/U6RX/CTED2/PMA11/RB12	91	AN23/OCM1E/RA6
42	AN13/CTED1/PMA10/RB13	92	AN22/OCM1F/PMA17/RA7
43	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	93	PMD0/RE0
44	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	94	PMD1/RE1
45	VSS	95	CTED11/PMA16/RG14
46	VDD	96	OCM2E/RG12
47	**RPI43**/RD14	97	OCM2F/CTED10/RG13
48	**RP5**/RD15	98	PMD2/RE2
49	**RP10**/PMA9/RF4	99	CTED9/PMD3/RE3
50	**RP17**/PMA8/RF5	100	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams[1] (Continued)

PIC24FJXXXGA610 121-Pin BGA



Legend: See Table 6 for a complete description of pin functions. Pinouts are subject to change.
Note 1: Gray shading indicates 5.5V tolerant input pins.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA610 BGA)

Pin	Full Pin Name	Pin	Full Pin Name
A1	HLVDIN/CTED8/PMD4/RE4	E1	AN16/**RPI41**/OCM3C/PMCS2/RC4
A2	CTED9/PMD3/RE3	E2	**RPI40**/OCM2D/RC3
A3	OCM2F/CTED10/RG13	E3	AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6
A4	PMD0/RE0	E4	**RPI39**/OCM2C/RC2
A5	PMD8/RG0	E5	N/C
A6	PMD10/RF1	E6	PMD9/RG1
A7	N/C	E7	N/C
A8	N/C	E8	**RPI35**/PMBE1/RA15
A9	**RPI42**/OCM3E/PMD12/RD12	E9	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
A10	**RP23**/PMACK1/RD2	E10	**RP4**/PMACK2/RD9
A11	**RP24**/U5TX/ICM4/RD1	E11	**RPI36**/PMA22/RA14
B1	N/C	F1	$\overline{\text{MCLR}}$
B2	OCM1C/CTED3/RG15	F2	AN19/C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8
B3	PMD2/RE2	F3	AN20/C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9
B4	PMD1/RE1	F4	AN18/C1INC/**RP26**/OCM1B/PMA4/RG7
B5	AN22/OCM1F/PMA17/RA7	F5	VSS
B6	$\overline{\text{U5CTS}}$/OC6/PMD11/RF0	F6	N/C
B7	VCAP	F7	N/C
B8	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5	F8	VDD
B9	**RP22**/ICM7/PMBE0/RD3	F9	OSCI/CLKI/RC12
B10	VSS	F10	VSS
B11	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14	F11	OSCO/CLKO/RC15
C1	SCL3/IC5/PMD6/RE6	G1	**RPI33**/PMCS1/RE8
C2	VDD	G2	AN21/**RPI34**/PMA19/RE9
C3	OCM2E/RG12	G3	TMS/OCM3D/RA0
C4	CTED11/PMA16/RG14	G4	N/C
C5	AN23/OCM1E/RA6	G5	VDD
C6	N/C	G6	VSS
C7	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/RD7	G7	VSS
C8	**RP25**/PMWR/PMENB/RD4	G8	N/C
C9	N/C	G9	TDO/RA5
C10	SOSCI/C3IND/RC13	G10	SDA2/PMA20/RA3
C11	**RP12**/PMA14/PMCS1/RD11	G11	TDI/PMA21/RA4
D1	**RPI38**/OCM1D/RC1	H1	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5
D2	SDA3/IC6/PMD7/RE7	H2	PGED3/AN4/C1INB/**RP28**/OCM3B/RB4
D3	IC4/CTED4/PMD5/RE5	H3	N/C
D4	N/C	H4	N/C
D5	N/C	H5	N/C
D6	N/C	H6	VDD
D7	C3INB/U5RX/OC4/PMD14/RD6	H7	N/C
D8	OCM3F/PMD13/RD13	H8	RF7
D9	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/RD0	H9	INT0/RF6
D10	N/C	H10	SCL1/RG2
D11	**RP3**/PMA15/PMCS2/RD10	H11	PMPCS1/SCL2/RA2

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA610 BGA) (CONTINUED)

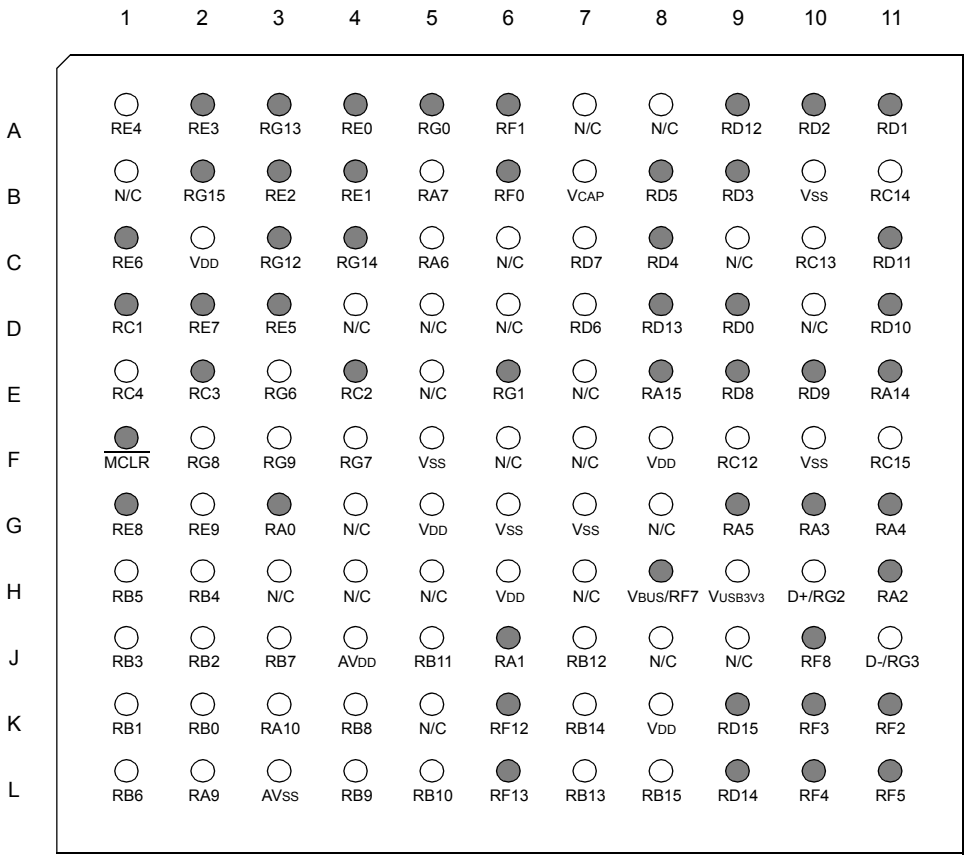
Pin	Full Pin Name	Pin	Full Pin Name
J1	AN3/C2INA/RB3	K7	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14
J2	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	K8	VDD
J3	PGED2/AN7/**RP7**/U6TX/RB7	K9	**RP5**/RD15
J4	AVDD	K10	**RP16**/RF3
J5	AN11/REFI/PMA12/RB11	K11	**RP30**/RF2
J6	TCK/RA1	L1	PGEC2/AN6/**RP6**/RB6
J7	AN12/U6RX/CTED2/PMA11/RB12	L2	CVREF-/VREF-/PMA7/RA9
J8	N/C	L3	AVSS
J9	N/C	L4	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9
J10	**RP15**/RF8	L5	CVREF/AN10/PMA13/RB10
J11	SDA1/RG3	L6	**RP31**/RF13
K1	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	L7	AN13/CTED1/PMA10/RB13
K2	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	L8	AN15/**RP29**/CTED6/PMA0/PMALL/RB15
K3	CVREF+/VREF+/PMA6/RA10	L9	**RPI43**/RD14
K4	AN8/**RP8**/PWRGT/RB8	L10	**RP10**/PMA9/RF4
K5	N/C	L11	**RP17**/PMA8/RF5
K6	**RPI32**/CTED7/PMA18/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams[1] (Continued)

PIC24FJXXXGB610 121-Pin BGA



Legend: See Table 7 for a complete description of pin functions. Pinouts are subject to change.
Note 1: Gray shading indicates 5.5V tolerant input pins.

TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB610 BGA)

Pin	Full Pin Name	Pin	Full Pin Name
A1	HLVDIN/CTED8/PMD4/RE4	E1	AN16/**RPI41**/OCM3C/PMCS2/RC4
A2	CTED9/PMD3/RE3	E2	**RPI40**/OCM2D/RC3
A3	OCM2F/CTED10/RG13	E3	AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6
A4	PMD0/RE0	E4	**RPI39**/OCM2C/RC2
A5	PMD8/RG0	E5	N/C
A6	PMD10/RF1	E6	PMD9/RG1
A7	N/C	E7	N/C
A8	N/C	E8	**RPI35**/SDA1/PMBE1/RA15
A9	**RPI42**/OCM3E/PMD12/RD12	E9	CLC4OUT/**RP2**/U6RTS/U6BCLK/ICM5/RD8
A10	**RP23**/PMACK1/RD2	E10	**RP4**/PMACK2/RD9
A11	**RP24**/U5TX/ICM4/RD1	E11	**RPI36**/SCL1/PMA22/RA14
B1	N/C	F1	MCLR
B2	OCM1C/CTED3/RG15	F2	AN19/C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8
B3	PMD2/RE2	F3	AN20/C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/ RG9
B4	PMD1/RE1	F4	AN18/C1INC/**RP26**/OCM1B/PMA4/RG7
B5	AN22/OCM1F/PMA17/RA7	F5	VSS
B6	U5CTS/OC6/PMD11/RF0	F6	N/C
B7	VCAP	F7	N/C
B8	**RP20**/PMRD/PMWR/RD5	F8	VDD
B9	**RP22**/ICM7/PMBE0/RD3	F9	OSCI/CLKI/RC12
B10	VSS	F10	VSS
B11	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14	F11	OSCO/CLKO/RC15
C1	SCL3/IC5/PMD6/RE6	G1	**RPI33**/PMCS1/RE8
C2	VDD	G2	AN21/**RPI34**/PMA19/RE9
C3	OCM2E/RG12	G3	TMS/OCM3D/RA0
C4	CTED11/PMA16/RG14	G4	N/C
C5	AN23/OCM1E/RA6	G5	VDD
C6	N/C	G6	VSS
C7	C3INA/U5RTS/U5BCLK/OC5/PMD15/RD7	G7	VSS
C8	**RP25**/PMWR/PMENB/RD4	G8	N/C
C9	N/C	G9	TDO/RA5
C10	SOSCI/C3IND/RC13	G10	SDA2/PMA20/RA3
C11	**RP12**/PMA14/PMCS1/RD11	G11	TDI/PMA21/RA4
D1	**RPI38**/OCM1D/RC1	H1	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5
D2	SDA3/IC6/PMD7/RE7	H2	PGED3/AN4/C1INB/**RP28**/USBOEN/OCM3B/RB4
D3	IC4/CTED4/PMD5/RE5	H3	N/C
D4	N/C	H4	N/C
D5	N/C	H5	N/C
D6	N/C	H6	VDD
D7	C3INB/U5RX/OC4/PMD14/RD6	H7	N/C
D8	OCM3F/PMD13/RD13	H8	VBUS/RF7
D9	CLC3OUT/**RP11**/U6CTS/ICM6/INT0/RD0	H9	VUSB3V3
D10	N/C	H10	D+/RG2
D11	**RP3**/PMA15/PMCS2/RD10	H11	PMPCS1/SCL2/RA2

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.l

TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB610 BGA) (CONTINUED)

Pin	Full Pin Name	Pin	Full Pin Name
J1	AN3/C2INA/RB3	K7	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14
J2	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	K8	VDD
J3	PGED2/AN7/**RP7**/U6TX/RB7	K9	**RP5**/RD15
J4	AVDD	K10	**RP16**/USBID/RF3
J5	AN11/REFI/PMA12/RB11	K11	**RP30**/RF2
J6	TCK/RA1	L1	PGEC2/AN6/**RP6**/RB6
J7	AN12/U6RX/CTED2/PMA11/RB12	L2	CVREF-/VREF-/PMA7/RA9
J8	N/C	L3	AVSS
J9	N/C	L4	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9
J10	**RP15**/RF8	L5	CVREF/AN10/PMA13/RB10
J11	D-/RG3	L6	**RP31**/RF13
K1	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	L7	AN13/CTED1/PMA10/RB13
K2	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	L8	AN15/**RP29**/CTED6/PMA0/PMALL/RB15
K3	CVREF+/VREF+/PMA6/RA10	L9	**RPI43**/RD14
K4	AN8/**RP8**/PWRGT/RB8	L10	**RP10**/PMA9/RF4
K5	N/C	L11	**RP17**/PMA8/RF5
K6	**RPI32**/CTED7/PMA18/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.l

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the PIC24FJ1024GA610/GB610 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"CPU with Extended Data Space (EDS)"** (DS39732)
- **"Data Memory with Extended Data Space (EDS)"** (DS39733)
- **"Direct Memory Access Controller (DMA)"** (DS39742)
- **"PIC24F Flash Program Memory"** (DS30009715)
- **"Reset"** (DS39712)
- **"Interrupts"** (DS70000600)
- **"Power-Saving Features"** (DS39698)
- **"I/O Ports with Peripheral Pin Select (PPS)"** (DS39711)
- **"Timers"** (DS39704)
- **"Input Capture with Dedicated Timer"** (DS70000352)
- **"Output Compare with Dedicated Timer"** (DS70005159)
- **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035A)
- **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136)
- **"Inter-Integrated Circuit (I^2C)"** (DS70000195)
- **"UART"** (DS39708)
- **"USB On-The-Go (OTG)"** (DS39721)
- **"Enhanced Parallel Master Port (EPMP)"** (DS39730)
- **"RTCC with Timestamp"** (DS70005193)
- **"RTCC with External Power Control"** (DS39745)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729)
- **"12-Bit A/D Converter with Threshold Detect"** (DS39739)
- **"Scalable Comparator Module"** (DS39734)
- **"Dual Comparator Module"** (DS39710)
- **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (DS30009743)
- **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725)
- **"Watchdog Timer (WDT)"** (DS39697)
- **"CodeGuard™ Intermediate Security"** (DS70005182)
- **"High-Level Device Integration"** (DS39719)
- **"Programming and Diagnostics"** (DS39716)
- **"Dual Partition Flash Program Memory"** (DS70005156)

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ1024GB610
- PIC24FJ512GB610
- PIC24FJ256GB610
- PIC24FJ128GB610
- PIC24FJ1024GB606
- PIC24FJ512GB606
- PIC24FJ256GB606
- PIC24FJ128GB606
- PIC24FJ1024GA610
- PIC24FJ512GA610
- PIC24FJ256GA610
- PIC24FJ128GA610
- PIC24FJ1024GA606
- PIC24FJ512GA606
- PIC24FJ256GA606
- PIC24FJ128GA606

The PIC24FJ1024GA610/GB610 family introduces many new analog features to the extreme low-power Microchip devices. This is a 16-bit microcontroller family with a broad peripheral feature set and enhanced computational performance. This family also offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but do not require the numerical processing power of a Digital Signal Processor (DSP).

Table 1-3 lists the functions of the various pins shown in the pinout diagrams.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 POWER-SAVING TECHNOLOGY

The PIC24FJ1024GA610/GB610 family of devices includes Retention Sleep, a low-power mode with essential circuits being powered from a separate low-voltage regulator.

This new low-power mode also supports the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from this new feature, PIC24FJ1024GA610/GB610 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of the Idle and the Sleep modes

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ1024GA610/GB610 family offer six different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- Two External Clock (EC) modes
- A Phase-Locked Loop (PLL) frequency multiplier, which allows clock speeds of up to 32 MHz
- A Digitally Controlled Oscillator (DCO) with multiple frequencies and fast wake-up time
- A Fast Internal Oscillator (FRC), a nominal 8 MHz output, with multiple frequency divider options
- A separate Low-Power Internal RC Oscillator (LPRC), 31 kHz nominal, for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger device, or even in jumping from 64-pin to 100-pin devices.

The PIC24F family is pin-compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

1.2 DMA Controller

PIC24FJ1024GA610/GB610 family devices have a Direct Memory Access (DMA) Controller. This module acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Eight independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.3 Other Special Features

- **Peripheral Pin Select:** The Peripheral Pin Select (PPS) feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Configurable Logic Cell:** The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins.
- **Timing Modules:** The PIC24FJ1024GA610/GB610 family provides five independent, general purpose, 16-bit timers (four of which can be combined into two 32-bit timers). The devices also include 3 multiple output and 4 single output advanced Capture/Compare/PWM/Timer peripherals, and 6 independent legacy Input Capture and 6 independent legacy Output Compare modules.
- **Communications:** The PIC24FJ1024GA610/GB610 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are 3 independent I^2C modules that support both Master and Slave modes of operation. Devices also have, through the PPS feature, 6 independent UARTs with built-in IrDA® encoders/decoders and 3 SPI modules.
- **Analog Features:** All members of the PIC24FJ1024GA610/GB610 family include the new 12-bit A/D Converter (A/D) module and a triple comparator module. The A/D module incorporates a range of new features that allow the converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions. The comparator module includes three analog comparators that are configurable for a wide range of operations.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ1024GA610/GB610 family include the CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits and address widths of up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.4 Details on Individual Family Members

Devices in the PIC24FJ1024GA610/GB610 family are available in 64-pin, 100-pin and 121-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in six ways:

1. Flash program memory (128 Kbytes for PIC24FJ128GX6XX devices, 256 Kbytes for PIC24FJ256GX6XX devices, 512 Kbytes for PIC24FJ512GX6XX devices and 1024 Kbytes for PIC24FJ1024GX6XX devices).
2. Available I/O pins and ports (53 pins on 6 ports for 64-pin devices and 85 pins on 7 ports for 100-pin and 121-pin devices).
3. Available Interrupt-on-Change Notification (IOC) inputs (53 on 64-pin devices and 85 on 100-pin and 121-pin devices).
4. Available remappable pins (29 pins on 64-pin devices, 44 pins on 100-pin and 121-pin devices).
5. Available USB peripheral (available on PIC24FJXXXGB6XX devices; not available on PIC24FJXXXGA6XX devices).
6. Analog input channels (16 channels for 64-pin devices and 24 channels for 100-pin and 121-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

A list of the pin features available on the PIC24FJ1024GA610/GB610 family devices, sorted by function, is shown in Table 1-3. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ1024GA606/GB606: 64-PIN DEVICES

Features	PIC24FJ128GX606	PIC24FJ256GX606	PIC24FJ512GX606	PIC24FJ1024GX606
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	128K	256K	512K	1024K
Program Memory (instructions)	44,032	88,064	176,128	352,256
Data Memory (bytes)	32K			
Interrupt Sources (soft vectors/ NMI traps)	103 (97/6)			
I/O Ports	Ports B, C, D, E, F, G			
Total I/O Pins	53			
Remappable Pins	29 (28 I/O, 1 input only)			
Timers: Total Number (16-bit)	5(1)			
32-Bit (from paired 16-bit timers)	2			
Input Capture Channels	6(1)			
Output Compare/PWM Channels	6(1)			
Input Change Notification Interrupt	53			
Serial Communications: UART	6(1)			
SPI (3-wire/4-wire)	3(1)			
I^2C	3			
Configurable Logic Cell (CLC)	4(1)			
Parallel Communications (EPMP/PSP)	Yes			
Capture/Compare/PWM/Timer Modules	3 Multiple Outputs and 4 Single Outputs			
JTAG Boundary Scan	Yes			
12/10-Bit Analog-to-Digital Converter (A/D) Module (input channels)	16			
Analog Comparators	3			
CTMU Interface	Yes			
Universal Serial Bus Controller	Yes (PIC24FJ1024GB606 devices only)			
Resets (and Delays)	Core POR, VDD POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	64-Pin TQFP and QFN			

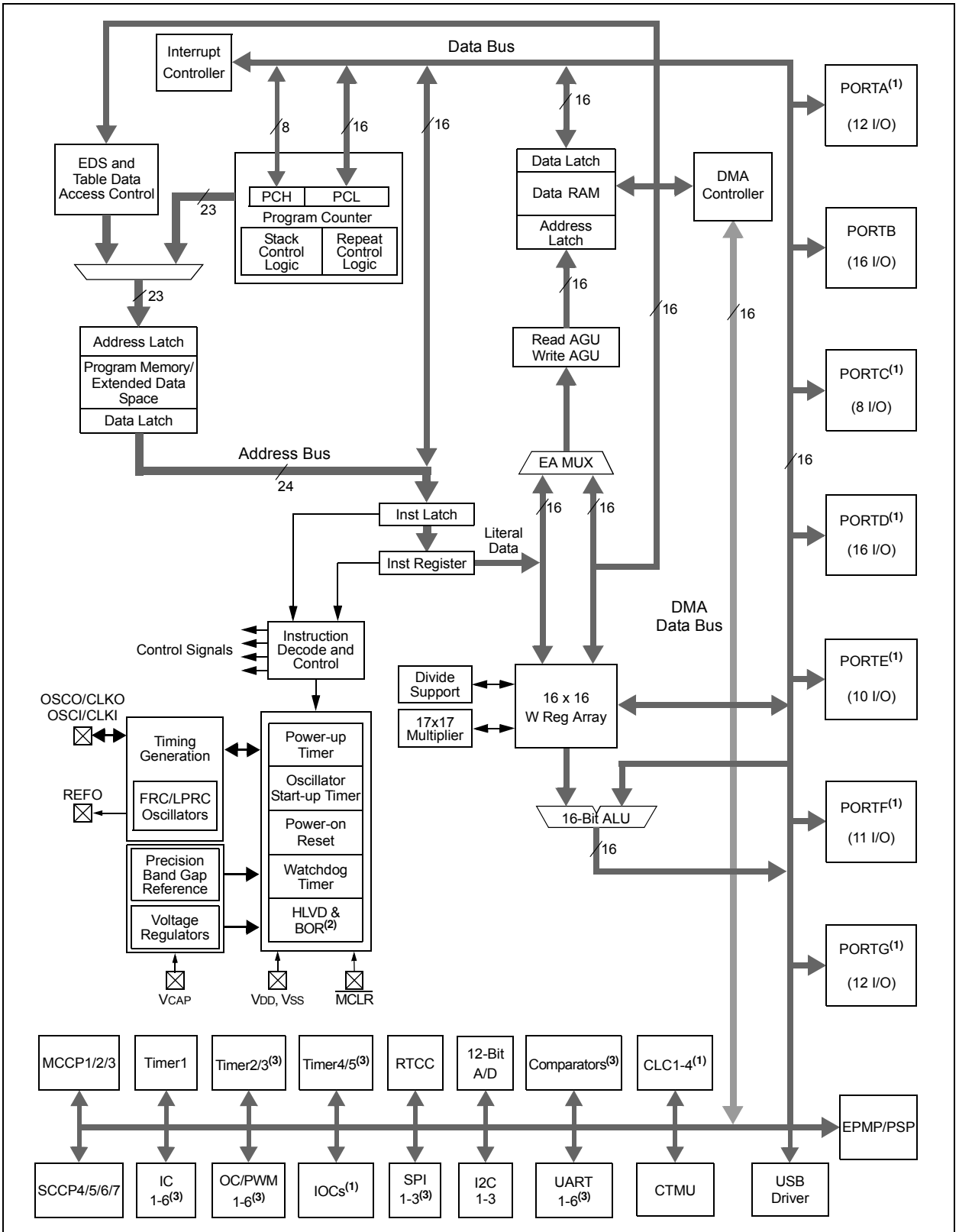
Note 1: Some peripherals are accessible through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ1024GX610: 100-PIN AND 121-PIN DEVICES

Features	PIC24FJ128GX610	PIC24FJ256GX610	PIC24FJ512GX610	PIC24FJ1024GX610
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	128K	256K	512K	1024K
Program Memory (instructions)	44,032	88,064	176,128	352,256
Data Memory (bytes)	32K			
Interrupt Sources (soft vectors/NMI traps)	103 (97/6)			
I/O Ports	Ports A, B, C, D, E, F, G			
Total I/O Pins	85			
Remappable Pins	44 (32 I/O, 12 input only)			
Timers: Total Number (16-bit)	5(1)			
32-Bit (from paired 16-bit timers)	2			
Capture/Compare/PWM/Timer Modules	3 Multiple Outputs and 4 Single Outputs			
Input Capture Channels	6(1)			
Output Compare/PWM Channels	6(1)			
Input Change Notification Interrupt	85			
Serial Communications: UART	6(1)			
SPI (3-wire/4-wire)	3(1)			
I^2C	3			
Configurable Logic Cell (CLC	4			
Parallel Communications (EPMP/PSP)	Yes			
JTAG Boundary Scan	Yes			
12/10-Bit Analog-to-Digital Converter (A/D) Module (input channels)	24			
Analog Comparators	3			
CTMU Interface	Yes			
Universal Serial Bus Controller	Yes (PIC14FJ1024GB610 devices only)			
Resets (and delays)	Core POR, VDD POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	100-Pin TQFP and 121-Pin BGA			

Note 1: Some peripherals are accessible through remappable pins.

FIGURE 1-1: PIC24FJ1024GA610/GB610 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-3 for specific implementations by pin count.
2: BOR functionality is provided when the on-board voltage regulator is enabled.
3: Some peripheral I/Os are only accessible through remappable pins.