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PIC24FJ128GB204 FAMILY

28/44-Pin, General Purpose, 16-Bit Flash Microcontrollers with Cryptographic Engine, ISO 7816, USB On-The-Go and XLP Technology

Cryptographic Engine

- AES Engine with 128,192 or 256-Bit Key
- Supports ECB, CBC, OFB, CTR and CFB128 modes
- DES/Triple DES (TDES) Engine: Supports 2-Key and 3-Key EDE or DED TDES
- Supports up to Three Unique Keys for TDES
- Programmatically Secure
- True Random Number Generator
- Pseudorandom Number Generator
- Non-Readable, On-Chip, OTP Key Storages

Universal Serial Bus Features

- USB v2.0 On-The-Go (OTG) Compliant
- Dual Role Capable; can Act as Either Host or Peripheral
- Low-Speed (1.5 Mb/s) and Full-Speed (12 Mb/s) USB Operation in Host mode
- Full-Speed USB Operation in Device mode
- High-Precision PLL for USB
- USB Device mode Operation from FRC Oscillator:
  - No crystal oscillator required
- Supports up to 32 Endpoints (16 bidirectional):
  - USB module can use any RAM locations on the device as USB endpoint buffers
- On-Chip USB Transceiver
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- On-Chip Pull-up and Pull-Down Resistors

Extreme Low-Power Features

- Multiple Power Management Options for Extreme Power Reduction:
  - VBAT allows the device to transition to a backup battery for the lowest power consumption with RTCC
  - Deep Sleep allows near total power-down, with the ability to wake-up on internal or external triggers
  - Sleep and Idle modes selectively shut down peripherals and/or core for substantial power reduction and fast wake-up
  - Doze mode allows CPU to run at a lower clock speed than peripherals
- Alternate Clock modes allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction
- Extreme Low-Power Current Consumption for Deep Sleep:
  - WDT: 270 nA @ 3.3V typical
  - RTCC: 400 nA @ 32 kHz, 3.3V typical
  - Deep Sleep current: 40 nA, 3.3V typical

Device	Memory		Pins	Analog Peripherals			Digital Peripherals							USB OTG	Deep Sleep w/VBAT	AES/DES Cryptographic
	Program Flash (bytes)	Data RAM (bytes)		10/12-Bit A/D (ch)	Comparators	CTMU (ch)	Input Capture	Output Compare/PWM	I2C™	SPI	UART w/IrDA® 7816	EPMP/PSP	16-Bit Timers			
PIC24FJ128GB204	128K	8K	44	12	3	12	6	6	2	3	4	Y	5	Y	Y	Y
PIC24FJ128GB202	128K	8K	28	9	3	9	6	6	2	3	4	N	5	Y	Y	Y
PIC24FJ64GB204	64K	8K	44	12	3	12	6	6	2	3	4	Y	5	Y	Y	Y
PIC24FJ64GB202	64K	8K	28	9	3	9	6	6	2	3	4	N	5	Y	Y	Y

Analog Features

- 10/12-Bit, 12-Channel Analog-to-Digital (A/D) Converter:
  - Conversion rate of 500 ksps (10-bit), 200 ksps (12-bit)
  - Conversion available during Sleep and Idle
- Three Rail-to-Rail, Enhanced Analog Comparators with Programmable Input/Output Configuration
- Three On-Chip Programmable Voltage References
- Charge Time Measurement Unit (CTMU):
  - Used for capacitive touch sensing, up to 12 channels
  - Time measurement down to 100 ps resolution
  - Operation in Sleep mode

Peripheral Features

- Up to Five External Interrupt Sources
- Peripheral Pin Select (PPS); Allows Independent I/O Mapping of many Peripherals
- Five 16-Bit Timers/Counters with Prescaler:
  - Can be paired as 32-bit timers/counters
- Six-Channel DMA supports All Peripheral modules:
  - Minimizes CPU overhead and increases data throughput
- Six Input Capture modules, each with a Dedicated 16-Bit Timer
- Six Output Compare/PWM modules, each with a Dedicated 16-Bit Timer
- Enhanced Parallel Master/Slave Port (EPMP/EPSP)
- Hardware Real-Time Clock/Calendar (RTCC):
  - Runs in Sleep, Deep Sleep and VBAT modes
- Three 3-Wire/4-Wire SPI modules:
  - Support four Frame modes
  - Variable FIFO buffer
  - I^2S mode
  - Variable width from 2-bit to 32-bit
- Two I^2C™ modules Support Multi-Master/ Slave mode and 7-Bit/10-Bit Addressing
- Four UART modules:
  - Support RS-485, RS-232 and LIN/J2602
  - On-chip hardware encoder/decoder for IrDA®
  - Smart Card ISO 7816 support on UART1 and UART2 only:
    - T = 0 protocol with automatic error handling
    - T = 1 protocol
    - Dedicated Guard Time Counter (GTC)
    - Dedicated Waiting Time Counter (WTC)
  - Auto-wake-up on Auto-Baud Detect (ABD)
  - 4-level deep FIFO buffer
- Programmable 32-Bit Cyclic Redundancy Check (CRC) Generator
- Digital Signal Modulator provides On-Chip FSK and PSK Modulation for a Digital Signal Stream
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Configurable Open-Drain Outputs on Digital I/O Pins
- 5.5V Tolerant Inputs on Most Pins

High-Performance CPU

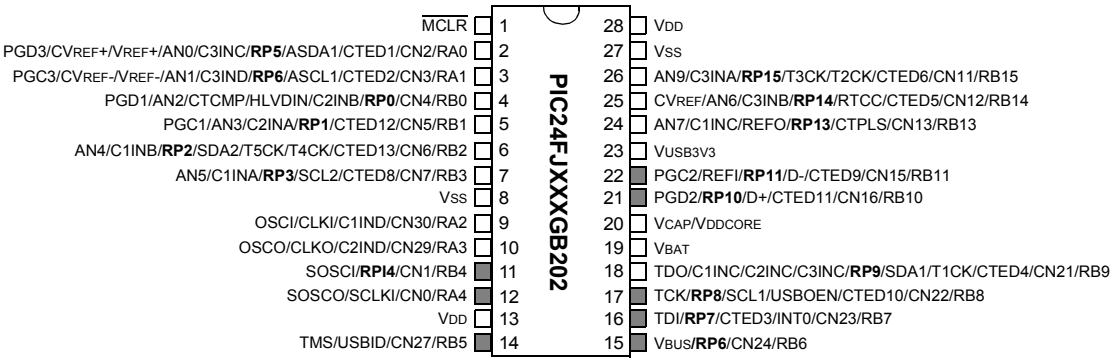
- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Internal Oscillator:
  - 96 MHz PLL option
  - Multiple clock divide options
  - Run-time self-calibration capability for maintaining better than ±0.20% accuracy
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture (ISA)
- Two Address Generation Units (AGUs) for Separate Read and Write Addressing of Data Memory

Special Microcontroller Features

- Supply Voltage Range of 2.0V to 3.6V
- Two On-Chip Voltage Regulators (1.8V and 1.2V) for Regular and Extreme Low-Power Operation
- 20,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- Flash Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Programmable Reference Clock Output
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via 2 Pins
- JTAG Programming and Boundary Scan Support
- Fail-Safe Clock Monitor (FSCM) Operation:
  - Detects clock failure and switches to on-chip, Low-Power RC Oscillator
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Separate Brown-out Reset (BOR) and Deep Sleep Brown-out Reset (DSBOR) Circuits
- Programmable High/Low-Voltage Detect (HLVD)
- Flexible Watchdog Timer (WDT) with its Own RC Oscillator for Reliable Operation
- Standard and Ultra Low-Power Watchdog Timers (ULPW) for Reliable Operation in Standard and Deep Sleep modes

Pin Diagrams

28-Pin SPDIP, SOIC, SSOP(1)

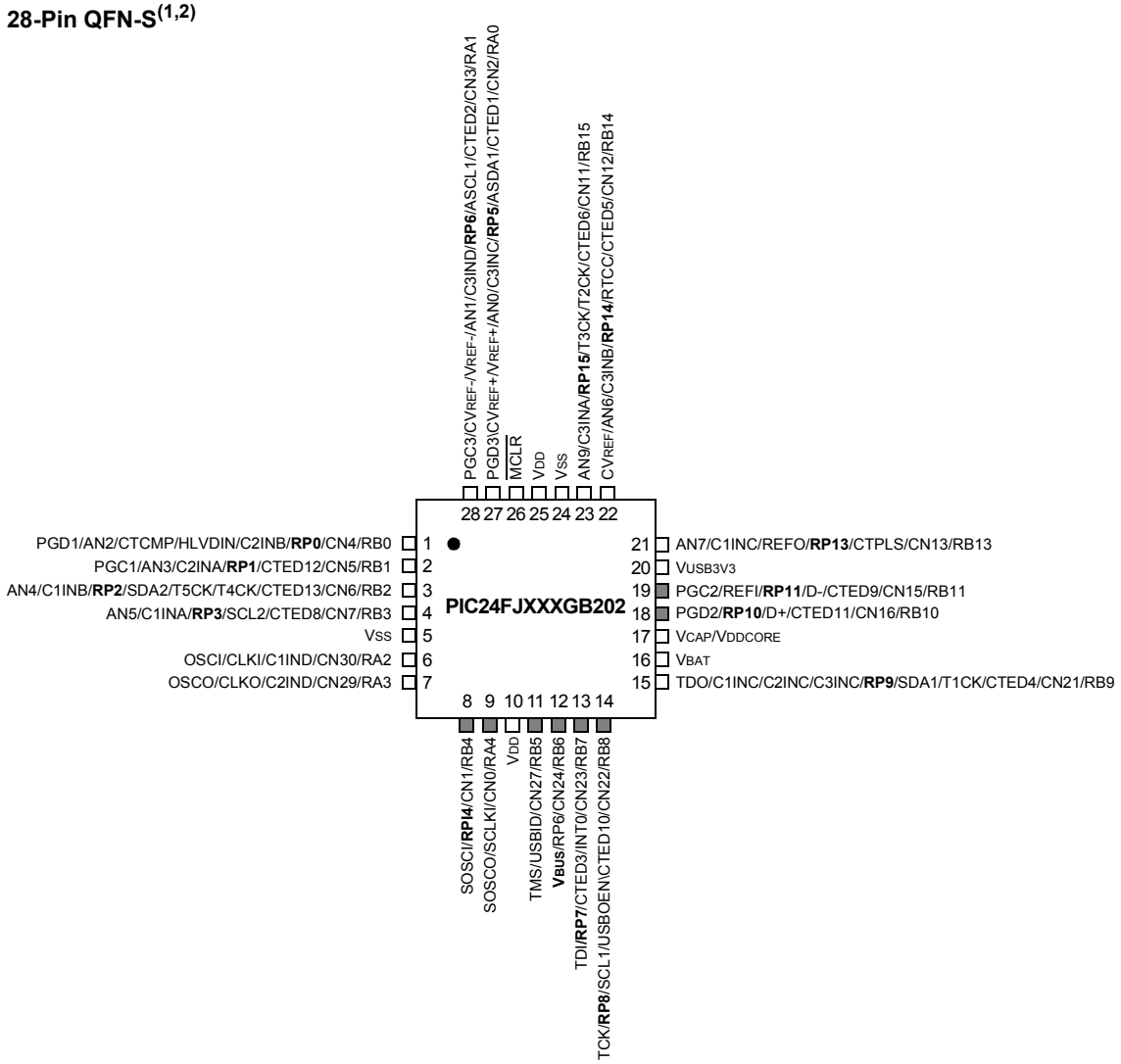


Legend: **RPn** represents remappable peripheral pins.

Note 1: Gray shading indicates 5.5V tolerant input pins.

Pin Diagrams (Continued)

28-Pin QFN-S(1,2)



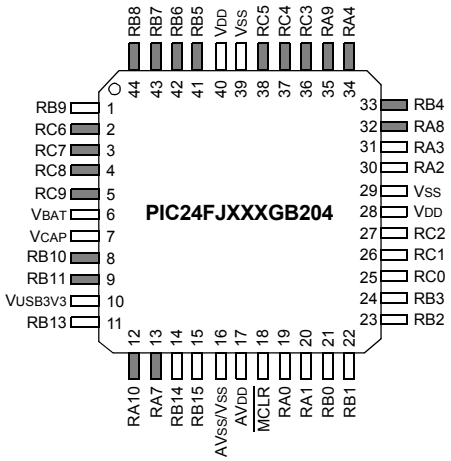
Legend: **RPn** represents remappable peripheral pins.

Note 1: Gray shading indicates 5.5V tolerant input pins.

2: The back pad on QFN devices should be connected to VSS.

Pin Diagrams (Continued)

44-Pin TQFP,
44-Pin QFN(1,2,3)



Note 1: Gray shading indicates 5.5V tolerant input pins.
2: The back pad on QFN devices should be connected to VSS.
3: See Table 1 for complete pinout descriptions.

TABLE 1: PIC24FJXXXGB204 PIN FUNCTION DESCRIPTIONS

Pin	Function	Pin	Function
1	C1INC/C2INC/C3INC/**RP9**/SDA1/T1CK/CTED4/PMD3/CN21/RB9	23	AN4/C1INB/**RP2**/SDA2/T5CK/T4CK/CTED13/CN6/PMD2/RB2
2	**RP22**/PMA1/PMALH/CN18/RC6	24	AN5/C1INA/**RP3**/SCL2/CTED8/CN7/PMWR/RB3
3	**RP23**/PMA0/PMALL/CN17/RC7	25	AN10/**RP16**/PMBE1/CN8/RC0
4	**RP24**/PMA5/CN20/RC8	26	AN11/**RP17**/CN9/RC1
5	**RP25**/CTED7/PMA6/CN19/RC9	27	AN12/**RP18**/PMACK1/CN10/RC2
6	VBAT	28	VDD
7	VCAP	29	VSS
8	**RP10**/CTED11/CN16/PGD2/D+/RB10	30	OSCI/C1IND/CLKI/PMCS1/CN30/RA2
9	REFI/**RP11**/CTED9/CN15/PGC2/D-/RB11	31	OSCO/C2IND/CLKO/CN29/RA3
10	VUSB3V3	32	TDO/PMA8/CN34/RA8
11	AN7/C1INC/REFO/**RP13**/CTPLS/PMRD/CN13/RB13	33	SOSCI/CN1/**RPI4**/RB4
12	TMS/PMA2/PMALU/CN36/RA10	34	SOSCO/SCLKI/CN0/RA4
13	TCK/PMA7/CN33/RA7	35	TDI/PMA9/CN35/RA9
14	CVREF/AN6/C3INB/**RP14**/RTCC/CTED5/CN12/RB14	36	**RP19**/PMBE0/CN28/RC3
15	AN9/C3INA/**RP15**/T3CK/T2CK/CTED6/PMA14/CS1/CN11/PMCS/PMCS1/RB15	37	**RP20**/PMA4/CN25/RC4
16	AVSS/VSS	38	**RP21**/PMA3/CN26/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	CVREF+/VREF+/AN0/C3INC/**RP5**/ASDA1(1)/CTED1/CN2/PMD7/PGD3/RA0	41	CN27/USBID/RB5
20	CVREF-/VREF-/AN1/C3IND/**RP6**/ASCL1(1)/CTED2/CN3/PGC3/RA1	42	PMD6/CN24/VBUS/RB6
21	AN2/CTCMP/C2INB/**RP0**/CN4/PGD1/HLVDIN/PMD0/RB0	43	**RP7**/CTED3/INT0/CN23/PMD5/RB7
22	AN3/C2INA/**RP1**/CTED12/CN5/PMD1/PGC1/RB1	44	**RP8**/SCL1/CTED10/PMD4/CN22/USBOEN/RB8

Legend: **RPn** represents remappable peripheral pins.
Note 1: Alternative multiplexing for SDA1 and SCL1 when the I2C1SEL Configuration bit is set.

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GB202
- PIC24FJ128GB202
- PIC24FJ64GB204
- PIC24FJ128GB204

The PIC24FJ128GB204 family expands the capabilities of the PIC24F family by adding a complete selection of Cryptographic Engines, ISO 7816 support and I^2S support to its existing features. This combination, along with its ultra low-power features, Direct Memory Access (DMA) for peripherals and USB On-The-Go, make this family the new standard for mixed-signal PIC® microcontrollers in one economical and power-saving package.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 XLP POWER-SAVING TECHNOLOGY

The PIC24FJ128GB204 family of devices introduces a greatly expanded range of power-saving operating modes for the ultimate in power conservation. The new modes include:

- Retention Sleep with essential circuits being powered from a separate low-voltage regulator
- Deep Sleep without RTCC for the lowest possible power consumption under software control
- V_{BAT} mode (with or without RTCC) to continue limited operation from a backup battery when V_{DD} is removed

Many of these new low-power modes also support the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from these new features, PIC24FJ128GB204 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of Idle and the many Sleep modes

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ128GB204 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- Two External Clock (EC) modes
- A Phase-Locked Loop (PLL) frequency multiplier, which allows clock speeds of up to 32 MHz
- A Fast Internal Oscillator (FRC) – Nominal 8 MHz output with multiple frequency divider options and automatic frequency self-calibration during run time
- A separate Low-Power Internal RC Oscillator (LPRC) – 31 kHz nominal for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

1.2 DMA Controller

PIC24FJ128GB204 family devices also add a Direct Memory Access (DMA) Controller to the existing PIC24F architecture. The DMA acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Six independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.3 USB On-The-Go (OTG)

USB On-The-Go provides on-chip functionality as a target device compatible with the USB 2.0 standard, as well as limited stand-alone functionality as a USB embedded host. By implementing USB Host Negotiation Protocol (HNP), the module can also dynamically switch between device and host operation, allowing for a much wider range of versatile USB-enabled applications on a microcontroller platform.

PIC24FJ128GB204 family devices also incorporate an integrated USB transceiver and precision oscillator, minimizing the required complexity of implementing a complete USB device, embedded host, dual role or On-The-Go application.

1.4 Cryptographic Engine

The Cryptographic Engine provides a new set of data security options. Using its own free-standing state machines, the engine can independently perform NIST standard encryption and decryption of data, independently of the CPU.

Support for True Random Number Generation (TRNG) and Pseudorandom Number Generation (PRNG); NIST SP800-90 compliant.

1.5 Other Special Features

- **Peripheral Pin Select (PPS):** The Peripheral Pin Select feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ128GB204 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are two independent I^2C™ modules that support both Master and Slave modes of operation. Devices also have, through the PPS feature, four independent UARTs with built-in IrDA® encoders/decoders, ISO 7816 Smart Card support (UART1 and UART2 only) and three SPI modules with I^2S and variable data width support.
- **Analog Features:** All members of the PIC24FJ128GB204 family include a 12-bit A/D Converter module and a triple comparator module. The A/D module incorporates a range of new features that allows the converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions. The comparator module includes three analog comparators that are configurable for a wide range of operations.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ128GB204 family include the CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits, and address widths of up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use by the core application.
- **Data Signal Modulator (DSM):** The Data Signal Modulator (DSM) allows the user to mix a digital data stream (the “modulator signal”) with a carrier signal to produce a modulated output.

1.6 Details on Individual Family Members

Devices in the PIC24FJ128GB204 family are available in 28-pin and 44-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in six ways:

1. Flash program memory (64 Kbytes for PIC24FJ64GB2XX devices and 128 Kbytes for PIC24FJ128GB2XX devices).
2. Available I/O pins and ports (21 pins on two ports for 28-pin devices, 35 pins on three ports for 44-pin devices).
3. Available Input Change Notification (ICN) inputs (20 on 28-pin devices and 34 on 44-pin devices).
4. Available remappable pins (14 pins on 28-pin devices and 24 pins on 44-pin devices).
5. Analog input channels for the A/D Converter (12 channels for 44-pin devices and 9 channels for 28-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

A list of the pin features available on the PIC24FJ128GB204 family devices, sorted by function, is shown in Table 1-3. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GB204 FAMILY: 44-PIN DEVICES

Features	PIC24FJ64GB204	PIC24FJ128GB204
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	72 (68/4)	
I/O Ports	Ports A, B, C	
Total I/O Pins	34	
Remappable Pins	24 (23 I/Os, 1 Input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture w/Timer Channels	6(1)	
Output Compare/PWM Channels	6(1)	
Input Change Notification Interrupts	34	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	3(1)	
I^2C™	2	
Digital Signal Modulator (DSM)	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12-Bit SAR Analog-to-Digital (A/D) Converter (input channels)	12	
Analog Comparators	3	
CTMU Interface	12 Channels	
Resets (and Delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	44-Pin TQFP and QFN	
Cryptographic Engine	Supports AES with 128, 192 and 256-Bit Key, DES and TDES, True Random and Pseudorandom Number Generator, On-Chip OTP Storage	
USB	USB Full-Speed and Low-Speed Compatible, On-The-Go (OTG) USB	
RTCC	Yes	

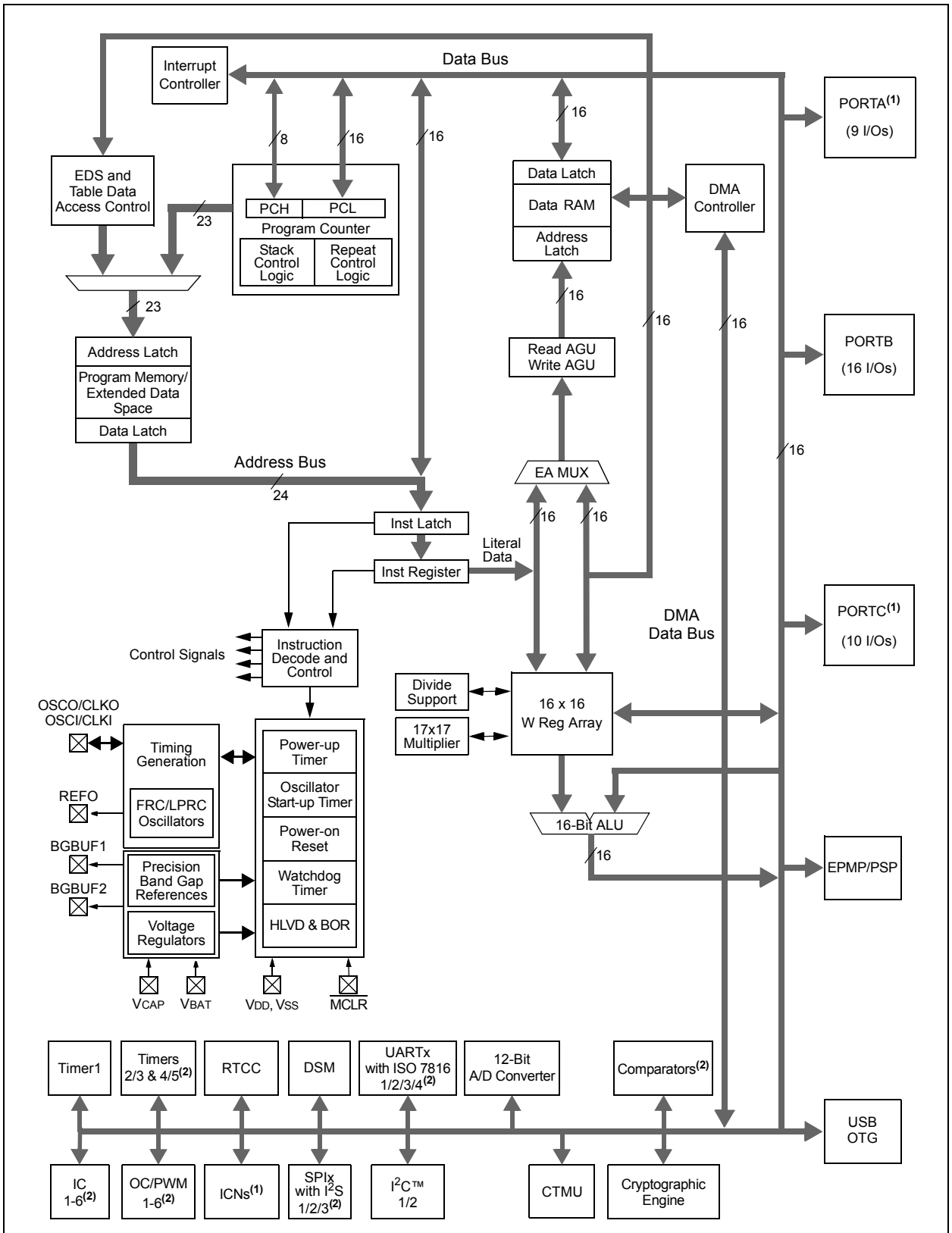
Note 1: Peripherals are accessible through remappable pins.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ128GB204 FAMILY: 28-PIN DEVICES

Features	PIC24FJ64GB202	PIC24FJ128GB202
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	72 (68/4)	
I/O Ports	Ports A, B	
Total I/O Pins	20	
Remappable Pins	15 (14 I/Os, 1 Input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture w/Timer Channels	6(1)	
Output Compare/PWM Channels	6(1)	
Input Change Notification Interrupts	20	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	3(1)	
I^2C™	2	
Digital Signal Modulator (DSM)	Yes	
JTAG Boundary Scan	Yes	
12-Bit SAR Analog-to-Digital (A/D) Converter (input channels)	9	
Analog Comparators	3	
CTMU Interface	9 Channels	
Resets (and Delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	28-Pin SPDIP, SSOP, SOIC and QFN-S	
Cryptographic Engine	Supports AES with 128, 192 and 256-Bit Key, DES and TDES, True Random and Pseudorandom Number Generator, On-Chip OTP Storage	
USB	USB Full-Speed and Low-Speed Compatible, On-The-Go (OTG) USB	
RTCC	Yes	

Note 1: Peripherals are accessible through remappable pins.

FIGURE 1-1: PIC24FJ128GB204 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-3 for specific implementations by pin count.

2: These peripheral I/Os are only accessible through remappable pins.

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
AN0	2	27	19	I	ANA	12-Bit SAR A/D Converter Inputs.
AN1	3	28	20	I	ANA	
AN2	4	1	21	I	ANA	
AN3	5	2	22	I	ANA	
AN4	6	3	23	I	ANA	
AN5	7	4	24	I	ANA	
AN6	25	22	14	I	ANA	
AN7	24	21	11	I	ANA	
AN9	26	23	15	I	ANA	
AN10	—	—	25	I	ANA	
AN11	—	—	26	I	ANA	
AN12	—	—	27	I	ANA	
ASCL1	3	28	20	—	—	
ASDA1	2	27	19	—	—	
AVDD	—	—	17	P	ANA	Positive Supply for Analog modules.
AVSS	—	24	16	P	ANA	Ground Reference for Analog modules.
C1INA	7	4	24	I	ANA	Comparator 1 Input A.
C1INB	6	3	23	I	ANA	Comparator 1 Input B.
C1INC	24	15	1	I	ANA	Comparator 1 Input C.
C1IND	9	6	30	I	ANA	Comparator 1 Input D.
C2INA	5	2	22	I	ANA	Comparator 2 Input A.
C2INB	4	1	21	I	ANA	Comparator 2 Input B.
C2INC	18	15	1	I	ANA	Comparator 2 Input C.
C2IND	10	7	31	I	ANA	Comparator 2 Input D.
C3INA	26	23	15	I	ANA	Comparator 3 Input A.
C3INB	25	22	14	I	ANA	Comparator 3 Input B.
C3INC	2	15	1	I	ANA	Comparator 3 Input C.
C3IND	3	28	20	I	ANA	Comparator 3 Input D.
CLKI	9	6	30	I	ANA	Main Clock Input Connection.
CLKO	10	7	31	O	—	System Clock Output.

Legend: ST = Schmitt Trigger input; TTL = TTL compatible input; I = Input
ANA = Analog input; O = Output; P = Power
I^2C = ST with I^2C™ or SMBus levels

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
CN0	12	9	34	—	—	Interrupt-on-Change Inputs.
CN1	11	8	33	—	—	
CN2	2	27	19	—	—	
CN3	3	28	20	—	—	
CN4	4	1	21	—	—	
CN5	5	2	22	—	—	
CN6	6	3	23	—	—	
CN7	7	4	24	—	—	
CN8	—	—	25	—	—	
CN9	—	—	26	—	—	
CN10	—	—	27	—	—	
CN11	26	23	15	—	—	
CN12	25	22	14	—	—	
CN13	24	21	11	—	—	
CN15	22	19	9	—	—	
CN16	21	18	8	—	—	
CN17	—	—	3	—	—	
CN18	—	—	2	—	—	
CN19	—	—	5	—	—	
CN20	—	—	4	—	—	
CN21	18	15	1	—	—	
CN22	17	14	44	—	—	
CN23	16	13	43	—	—	
CN24	15	12	42	—	—	
CN25	—	—	37	—	—	
CN26	—	—	38	—	—	
CN27	14	11	41	—	—	
CN28	—	—	36	—	—	
CN29	10	7	31	—	—	
CN30	9	6	30	—	—	
CN33	—	—	13	—	—	
CN34	—	—	32	—	—	
CN35	—	—	35	—	—	
CN36	—	—	12	—	—	
CTCMP	4	1	21	I	ANA	CTMU Comparator 2 Input (Pulse mode).

Legend: ST = Schmitt Trigger input
TTL = TTL compatible input
I = Input
ANA = Analog input
O = Output
P = Power
I^2C = ST with I^2C™ or SMBus levels

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
CTED1	2	27	19	I	ANA	CTMU External Edge Inputs.
CTED2	3	28	20	I	ANA	
CTED3	16	13	43	I	ANA	
CTED4	18	15	1	I	ANA	
CTED5	25	22	14	I	ANA	
CTED6	26	23	15	I	ANA	
CTED7	—	—	5	I	ANA	
CTED8	7	4	24	I	ANA	
CTED9	22	19	9	I	ANA	
CTED10	17	14	44	I	ANA	
CTED11	21	18	8	I	ANA	
CTED12	5	2	22	I	ANA	
CTED13	6	3	23	I	ANA	
CTPLS	24	21	11	O	—	CTMU Pulse Output.
CV_{REF}	25	22	14	O	ANA	Comparator Voltage Reference Output.
$CV_{REF}+$	2	27	19	I	ANA	Comparator Voltage Reference (high) Input.
$CV_{REF}-$	3	28	20	I	ANA	Comparator Voltage Reference (low) Input.
D+	21	18	8	I/O	—	USB Differential Plus Line (internal transceiver).
D-	22	19	9	I/O	—	USB Differential Minus Line (internal transceiver).
INT0	16	13	43	I	ST	External Interrupt Input 0.
HLVDIN	4	1	21	I	ANA	High/Low-Voltage Detect Input.
$\overline{MCLR}$	1	26	18	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	9	6	30	I	ANA	Main Oscillator Input Connection.
OSCO	10	7	31	O	—	Main Oscillator Output Connection.
PGC1	5	2	22	I/O	ST	In-Circuit Debugger/Emulator/ICSP™ Programming Clock.
PGC2	22	19	9	I/O	ST	
PGC3	3	28	20	I/O	ST	
PGD1	4	1	21	I/O	ST	
PGD2	21	18	8	I/O	ST	
PGD3	2	27	19	I/O	ST	

Legend: ST = Schmitt Trigger input TTL = TTL compatible input I = Input
ANA = Analog input O = Output P = Power
I^2C = ST with I^2C™ or SMBus levels

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
PMA0/PMALL	—	—	3	O	—	Parallel Master Port Address.
PMA1/PMALH	—	—	2	O	—	
PMA14/PMCS/ PMCS1	—	—	15	O	—	
PMA2/PMALU	—	—	12	O	—	
PMA3	—	—	38	O	—	
PMA4	—	—	37	O	—	
PMA5	—	—	4	O	—	
PMA6	—	—	5	O	—	
PMA7	—	—	13	O	—	
PMA8	—	—	32	O	—	
PMA9	—	—	35	O	—	
PMACK1	—	—	27	I	ST/TTL	Parallel Master Port Acknowledge Input 1.
PMBE0	—	—	36	O	—	Parallel Master Port Byte Enable 0 Strobe.
PMBE1	—	—	25	O	—	Parallel Master Port Byte Enable 1 Strobe.
PMCS1	—	—	30	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe.
PMD0	—	—	21	I/O	ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	—	—	22	I/O	ST/TTL	
PMD2	—	—	23	I/O	ST/TTL	
PMD3	—	—	1	I/O	ST/TTL	
PMD4	—	—	44	I/O	ST/TTL	
PMD5	—	—	43	I/O	ST/TTL	
PMD6	—	—	20	I/O	ST/TTL	
PMD7	—	—	19	I/O	ST/TTL	
PMRD	—	—	11	O	—	Parallel Master Port Read Strobe.
PMWR	—	—	24	O	—	Parallel Master Port Write Strobe.
RA0	2	27	19	I/O	ST	PORTA Digital I/Os.
RA1	3	28	20	I/O	ST	
RA2	9	6	30	I/O	ST	
RA3	10	7	31	I/O	ST	
RA4	12	9	34	I	ST	
RA7	—	—	13	I/O	ST	
RA8	—	—	32	I/O	ST	
RA9	—	—	35	I/O	ST	
RA10	—	—	12	I/O	ST	

Legend: ST = Schmitt Trigger input; TTL = TTL compatible input; I = Input
ANA = Analog input; O = Output; P = Power
I^2C = ST with I^2C™ or SMBus levels

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
RB0	4	1	21	I/O	ST	PORTB Digital I/Os.
RB1	5	2	22	I/O	ST	
RB2	6	3	23	I/O	ST	
RB3	7	4	24	I/O	ST	
RB4	11	8	33	I	ST	
RB5	14	11	41	I/O	ST	
RB6	15	12	42	I/O	ST	
RB7	16	13	43	I/O	ST	
RB8	17	14	44	I/O	ST	
RB9	18	15	1	I/O	ST	
RB10	21	18	8	I/O	ST	
RB11	22	19	9	I/O	ST	
RB13	24	21	11	I/O	ST	
RB14	25	22	14	I/O	ST	
RB15	26	23	15	I/O	ST	
RC0	—	—	25	I/O	ST	PORTC Digital I/Os.
RC1	—	—	26	I/O	ST	
RC2	—	—	27	I/O	ST	
RC3	—	—	36	I/O	ST	
RC4	—	—	37	I/O	ST	
RC5	—	—	38	I/O	ST	
RC6	—	—	2	I/O	ST	
RC7	—	—	3	I/O	ST	
RC8	—	—	4	I/O	ST	
RC9	—	—	5	I/O	ST	
REFI	22	19	9	—	—	Reference Clock Input.
REFO	24	21	11	—	—	Reference Clock Output.

Legend: ST = Schmitt Trigger input
ANA = Analog input
I^2C = ST with I^2C™ or SMBus levels
TTL = TTL compatible input
O = Output
I = Input
P = Power

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
RP0	4	1	21	I/O	ST	Remappable Peripheral (input or output).
RP1	5	2	22	I/O	ST	
RP2	6	3	23	I/O	ST	
RP3	7	4	24	I/O	ST	
RP5	2	27	19	I/O	ST	
RP6	3,15	28	20	I/O	ST	
RP7	16	13	43	I/O	ST	
RP8	17	14	44	I/O	ST	
RP9	18	15	1	I/O	ST	
RP10	21	18	8	I/O	ST	
RP11	22	19	9	I/O	ST	
RP13	24	21	11	I/O	ST	
RP14	25	22	14	I/O	ST	
RP15	26	23	15	I/O	ST	
RP16	—	—	25	I/O	ST	
RP17	—	—	26	I/O	ST	
RP18	—	—	27	I/O	ST	
RP19	—	—	36	I/O	ST	
RP20	—	—	37	I/O	ST	
RP21	—	—	38	I/O	ST	
RP22	—	—	2	I/O	ST	
RP23	—	—	3	I/O	ST	
RP24	—	—	4	I/O	ST	
RP25	—	—	5	I/O	ST	
RPI4	11	8	33	I	ST	Remappable Peripheral (input).
RTCC	25	22	14	O	—	Real-Time Clock Alarm/Seconds Pulse Output.
SCL1	17	14	44	I/O	I^2C	I2C1 Synchronous Serial Clock Input/Output.
SCL2	7	4	24	I/O	I^2C	I2C2 Synchronous Serial Clock Input/Output.
SCLKI	12	9	34	I	—	Secondary Oscillator Digital Clock Input.
SDA1	18	15	1	I/O	I^2C	I2C1 Data Input/Output.
SDA2	6	3	23	I/O	I^2C	I2C2 Data Input/Output.
SOSCI	11	8	33	I	ANA	Secondary Oscillator/Timer1 Clock Input.
SOSCO	12	9	34	O	ANA	Secondary Oscillator/Timer1 Clock Output.

Legend: ST = Schmitt Trigger input
ANA = Analog input
I^2C = ST with I^2C™ or SMBus levels
TTL = TTL compatible input
O = Output
I = Input
P = Power

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
T1CK	18	15	1	I	ST	Timer1 Clock.
T2CK	26	23	15	I	ST	Timer2 Clock.
T3CK	26	23	15	I	ST	Timer3 Clock.
T4CK	6	3	23	I	ST	Timer4 Clock.
T5CK	6	3	23	I	ST	Timer5 Clock.
TCK	17	14	13	I	ST	JTAG Test Clock/Programming Clock Input.
TDI	16	13	35	I	ST	JTAG Test Data/Programming Data Input.
TDO	18	15	32	O	—	JTAG Test Data Output.
TMS	14	11	12	I	—	JTAG Test Mode Select Input.
USBID	14	11	41	I	ST	USB OTG ID (OTG mode only).
USBOEN	17	14	44	O	—	USB Output Enable Control (for external transceiver).
VBAT	19	16	6	P	—	Backup Battery (B+) Input (1.2V nominal).
VBUS	15	12	42	P	—	USB Voltage, Host mode (5V).
VCAP	20	17	7	P	—	External Filter Capacitor Connection.
VDD	13,28	25	28,40	P	—	Positive Supply for Peripheral Digital Logic and I/O Pins.
VDDCORE	20	17	7	—	—	Microcontroller Core Supply Voltage.
VREF+	2	27	19	I	ANA	A/D Reference Voltage Input (+).
VREF-	3	28	20	I	ANA	A/D Reference Voltage Input (-).
VSS	8,27	5,24	29,39	P	—	Ground Reference for Logic and I/O Pins.
VUSB3V3	23	20	10	P	—	USB Transceiver Power Input Voltage (3.3V nominal).

Legend: ST = Schmitt Trigger input; TTL = TTL compatible input; I = Input
ANA = Analog input; O = Output; P = Power
I^2C = ST with I^2C™ or SMBus levels

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24FJ128GB204 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Power Supply Pins"**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used
  (see **Section 2.2 "Power Supply Pins"**)
- MCLR pin
  (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- ENVREG/DISVREG and VCAP/VDDCORE pins
  (see **Section 2.4 "Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)"**)

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

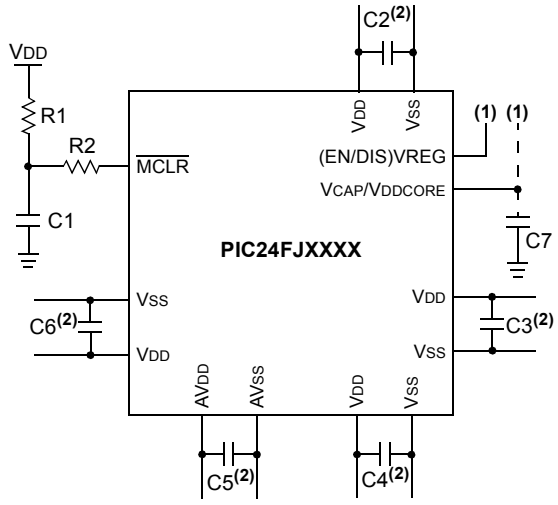
Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for analog modules is implemented

Note:	The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 µF, 20V ceramic

C7: 10 µF, 6.3V or greater, tantalum or ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

Note 1: See **Section 2.4 "Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)"** for the explanation of the ENVREG/DISVREG pin connections.

2: The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including microcontrollers to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF.

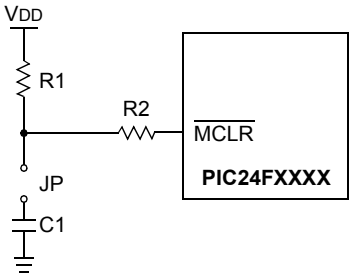
2.3 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



Note 1: R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{\text{MCLR}}$ pin VIH and VIL specifications are met.

2: R2 ≤ 470Ω will limit any current flowing into $\overline{\text{MCLR}}$ from the external capacitor, C, in the event of $\overline{\text{MCLR}}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{\text{MCLR}}$ pin VIH and VIL specifications are met.

2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)

Note: This section applies only to PIC24FJ devices with an on-chip voltage regulator.

The on-chip voltage regulator enable/disable pin (ENVREG or DISVREG, depending on the device family) must always be connected directly to either a supply voltage or to ground. The particular connection is determined by whether or not the regulator is to be used:

- For ENVREG, tie to VDD to enable the regulator, or to ground to disable the regulator
- For DISVREG, tie to ground to enable the regulator or to VDD to disable the regulator

Refer to **Section 30.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

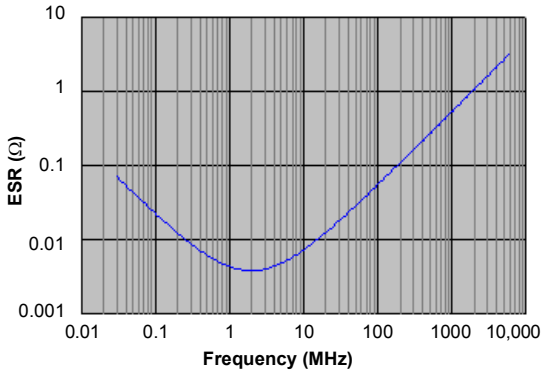
When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP/VDDCORE. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 33.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 33.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to +125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to +85ºC