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PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04

16-bit Microcontrollers (up to 128 KB Flash and 8K SRAM) with Advanced Analog

Operating Conditions

- 3.0V to 3.6V, -40°C to +150°C, DC to 20 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 40 MIPS

Clock Management

- 2% internal oscillator
- Programmable PLL and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Low-power management modes
- Fast wake-up and start-up

High-Efficiency Math Engine

- Single-cycle MUL plus hardware divide

Advanced Analog Features

- 10/12-bit ADC with 1.1Msps/500 ksps conversion rate:
 - Up to 13 ADC input channels and four S&H
 - Flexible/Independent trigger sources
- 150 ns Comparators:
 - Up to two Analog Comparator modules
 - 4-bit DAC with two ranges for Analog Comparators

Input/Output

- Software remappable pin functions
- 5V-tolerant pins
- Selectable open drain and internal pull-ups
- Up to 5 mA overvoltage clamp current/pin
- Multiple external interrupts

Packages

Type	SPDIP	SOIC	QFN-S	QFN	TQFP
Pin Count	28	28	28	44	44
I/O Pins	21	21	21	35	35
Contact Lead/Pitch	.100"	1.27	0.65	0.65	0.80
Dimensions	1.365x.285x.135"	17.9x7.50x2.05	6x6x0.9	8x8x0.9	10x10x1

Note: All dimensions are in millimeters (mm) unless specified.

System Peripherals

- Cyclic Redundancy Check (CRC) module
- Up to five 16-bit and up to two 32-bit Timers/Counters
- Up to four Input Capture (IC) modules
- Up to four Output Compare (OC) modules
- Real-Time Clock and Calendar (RTCC) module

Communication Interfaces

- Parallel Master Port (PMP)
- Two UART modules (10 Mbps)
 - Supports LIN 2.0 protocols
 - RS-232, RS-485, and IrDA[®] support
- Two 4-wire SPI modules (15 Mbps)
- Enhanced CAN (ECAN) module (1 Mbaud) with 2.0B support
- I²C module (100K, 400K and 1Mbaud) with SMBus support

Direct Memory Access (DMA)

- 8-channel hardware DMA with no CPU stalls or overhead
- UART, SPI, ADC, ECAN, IC, OC, INT0

Qualification and Class B Support

- AEC-Q100 REVG (Grade 0 -40°C to +150°C)
- Class B Safety Library, IEC 60730, VDE certified

Debugger Development Support

- In-circuit and in-application programming
- Two program breakpoints
- Trace and run-time watch

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed below. The following pages show their pinout diagrams.

TABLE 1: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 CONTROLLER FAMILIES

Device	Pins	Program Flash Memory (Kbyte)	RAM (Kbyte) ⁽¹⁾	Remappable Peripheral								RTCC	I ² C™	CRC Generator	10-bit/12-bit ADC (Channels)	Analog Comparator (2 Channels/Voltage Regulator)	8-bit Parallel Master Port (Address Lines)	I/O Pins	Packages
				Remappable Pins	16-bit Timer ⁽²⁾	Input Capture	Output Compare Standard PWM	UART	SPI	ECAN™	External Interrupts ⁽³⁾								
PIC24HJ128GP504	44	128	8	26	5	4	4	2	2	1	3	1	1	1	13	1/1	11	35	QFN TQFP
PIC24HJ128GP502	28	128	8	16	5	4	4	2	2	1	3	1	1	1	10	1/0	2	21	SPDIP SOIC QFN-S
PIC24HJ128GP204	44	128	8	26	5	4	4	2	2	0	3	1	1	1	13	1/1	11	35	QFN TQFP
PIC24HJ128GP202	28	128	8	16	5	4	4	2	2	0	3	1	1	1	10	1/0	2	21	SPDIP SOIC QFN-S
PIC24HJ64GP504	44	64	8	26	5	4	4	2	2	1	3	1	1	1	13	1/1	11	35	QFN TQFP
PIC24HJ64GP502	28	64	8	16	5	4	4	2	2	1	3	1	1	1	10	1/0	2	21	SPDIP SOIC QFN-S
PIC24HJ64GP204	44	64	8	26	5	4	4	2	2	0	3	1	1	1	13	1/1	11	35	QFN TQFP
PIC24HJ64GP202	28	64	8	16	5	4	4	2	2	0	3	1	1	1	10	1/0	2	21	SPDIP SOIC QFN-S
PIC24HJ32GP304	44	32	4	26	5	4	4	2	2	0	3	1	1	1	13	1/1	11	35	QFN TQFP
PIC24HJ32GP302	28	32	4	16	5	4	4	2	2	0	3	1	1	1	10	1/0	2	21	SPDIP SOIC QFN-S

Note 1: RAM size is inclusive of 2 Kbytes of DMA RAM for all devices except PIC24HJ32GP302/304, which include 1 Kbyte of DMA RAM.

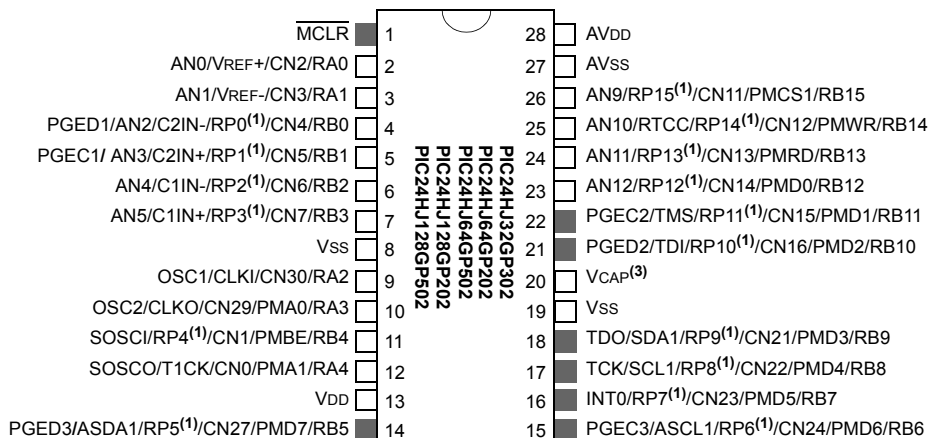
2: Only four out of five timers are remappable.

3: Only two out of three interrupts are remappable.

Pin Diagrams

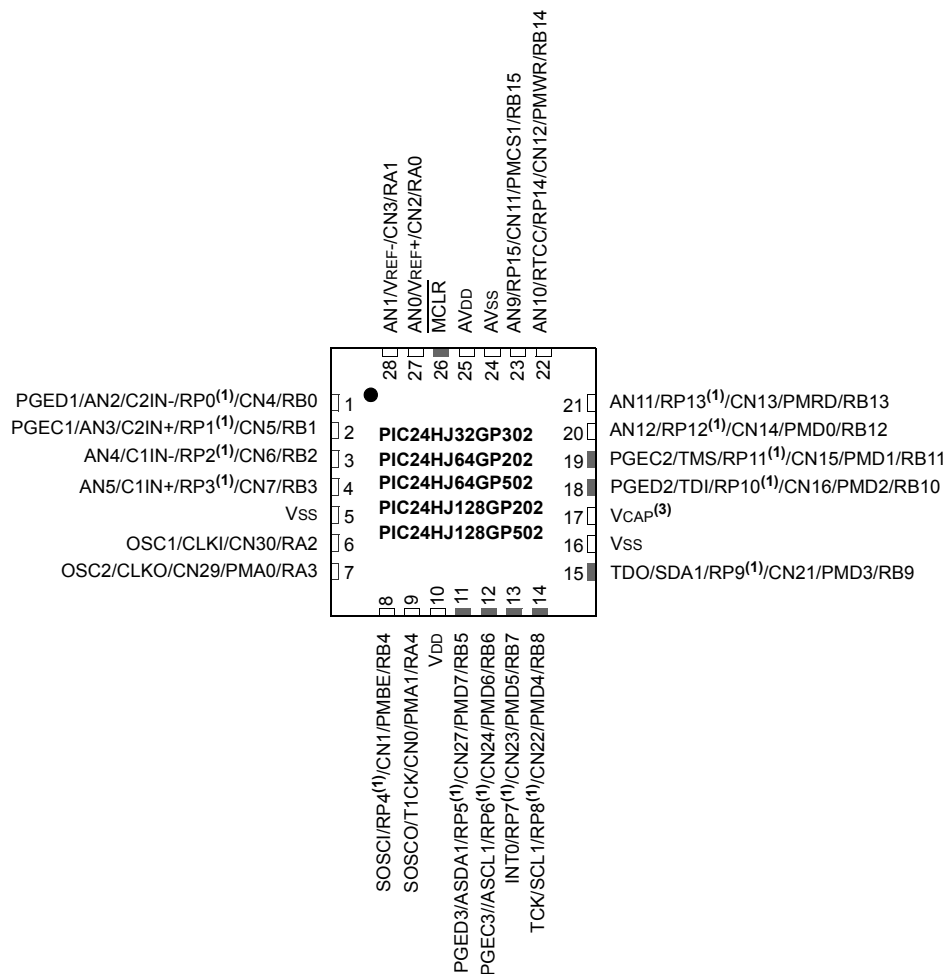
28-Pin SPDIP, SOIC

■ Pins are up to 5V tolerant



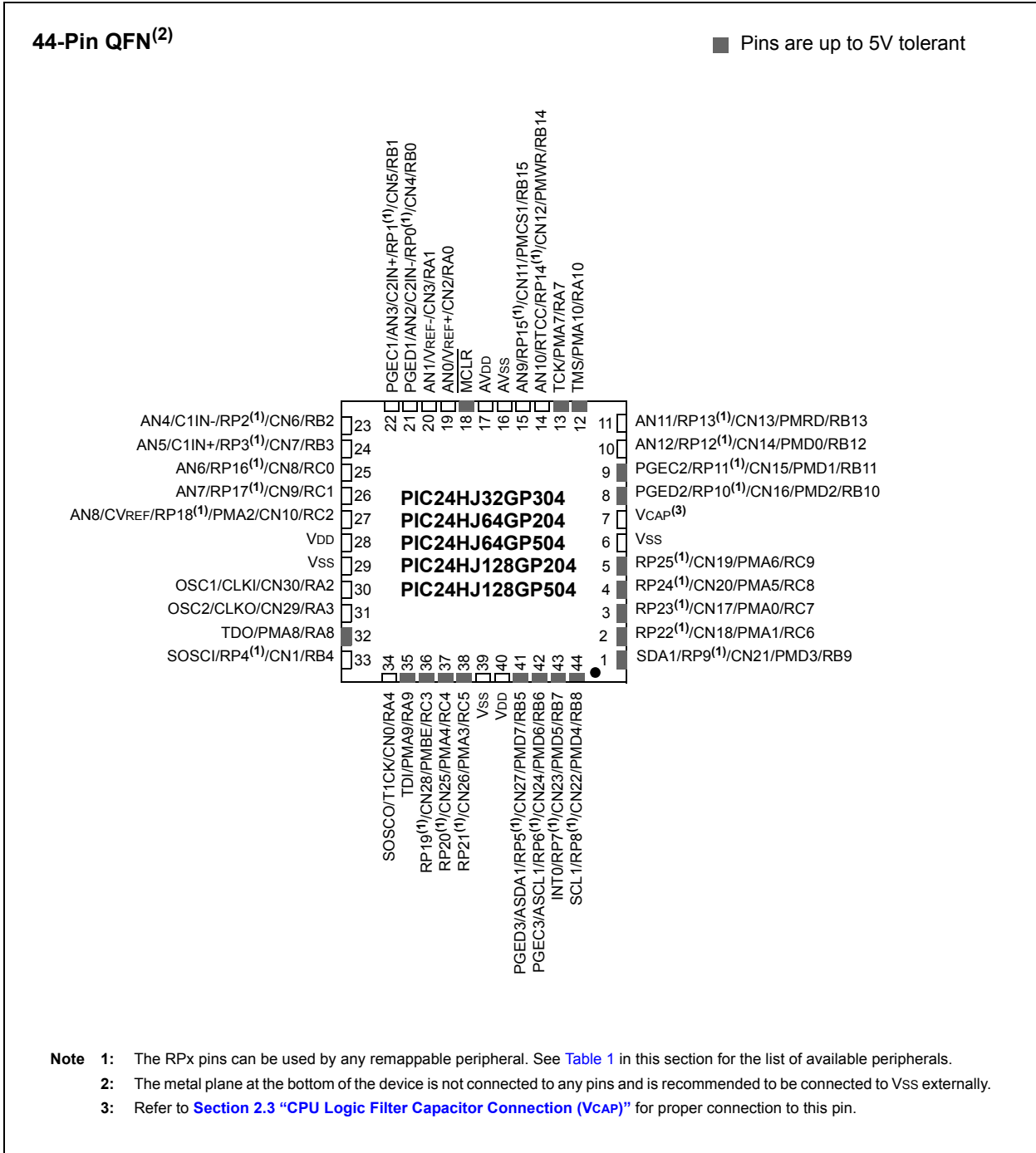
28-Pin QFN-S⁽²⁾

■ Pins are up to 5V tolerant



- Note**
- 1: The RP_x pins can be used by any remappable peripheral. See [Table 1](#) in this section for the list of available peripherals.
 - 2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 3: Refer to [Section 2.3 “CPU Logic Filter Capacitor Connection \(V_{CAP}\)”](#) for proper connection to this pin.

Pin Diagrams (Continued)

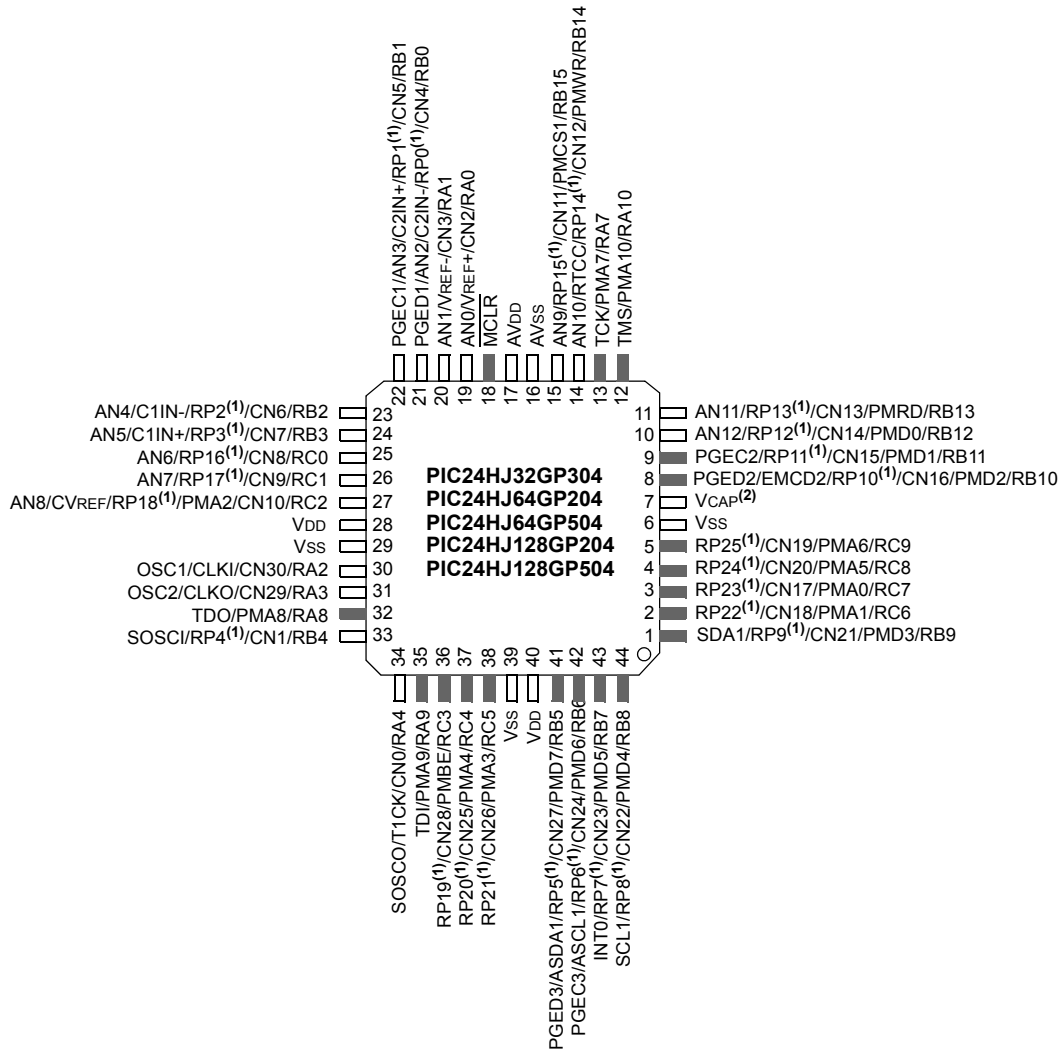


- Note** 1: The RPx pins can be used by any remappable peripheral. See [Table 1](#) in this section for the list of available peripherals.
 2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 3: Refer to [Section 2.3 "CPU Logic Filter Capacitor Connection \(VCAP\)"](#) for proper connection to this pin.

Pin Diagrams (Continued)

44-Pin TQFP

■ Pins are up to 5V tolerant



- Note** 1: The RPx pins can be used by any remappable peripheral. See Table 1 in this section for the list of available peripherals.
 2: Refer to Section 2.3 “CPU Logic Filter Capacitor Connection (Vcap)” for proper connection to this pin.

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To determine if an errata sheet exists for a particular device, please check with one of the following:

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When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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Referenced Sources

This device data sheet is based on the following individual chapters of the “*dsPIC33F/PIC24H Family Reference Manual*”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the [PIC24HJ64GP204](#) product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. “Introduction”** (DS70197)
- **Section 2. “CPU”** (DS70204)
- **Section 3. “Data Memory”** (DS70202)
- **Section 4. “Program Memory”** (DS70202)
- **Section 5. “Flash Programming”** (DS70191)
- **Section 8. “Reset”** (DS70192)
- **Section 9. “Watchdog Timer and Power-saving Modes”** (DS70196)
- **Section 11. “Timers”** (DS70205)
- **Section 12. “Input Capture”** (DS70198)
- **Section 13. “Output Compare”** (DS70209)
- **Section 16. “Analog-to-Digital Converter (ADC)”** (DS70183)
- **Section 17. “UART”** (DS70188)
- **Section 18. “Serial Peripheral Interface (SPI)”** (DS70206)
- **Section 19. “Inter-Integrated Circuit™ (I²C™)”** (DS70195)
- **Section 23. “CodeGuard™ Security”** (DS70199)
- **Section 24. “Programming and Diagnostics”** (DS70209)
- **Section 25. “Device Configuration”** (DS70194)
- **Section 30. “I/O Ports with Peripheral Pin Select (PPS)”** (DS70190)
- **Section 32. “Interrupts (Part III)”** (DS70214)
- **Section 33. “Audio Digital-to-Analog Converter (DAC)”** (DS70211)
- **Section 34. “Comparator”** (DS70212)
- **Section 35. “Parallel Master Port (PMP)”** (DS70299)
- **Section 36. “Programmable Cyclic Redundancy Check (CRC)”** (DS70298)
- **Section 37. “Real-Time Clock and Calendar (RTCC)”** (DS70301)
- **Section 38. “Direct Memory Access”** (DS70215)
- **Section 39. “Oscillator (Part III)”** (DS70216)

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “*dsPIC33F/PIC24H Family Reference Manual*”. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This document contains device specific information for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices.

[Figure 1-1](#) shows a general block diagram of the core and peripheral modules in the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices.

[Table 1-1](#) lists the functions of the various pins shown in the pinout diagrams.

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

FIGURE 1-1: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 BLOCK DIAGRAM

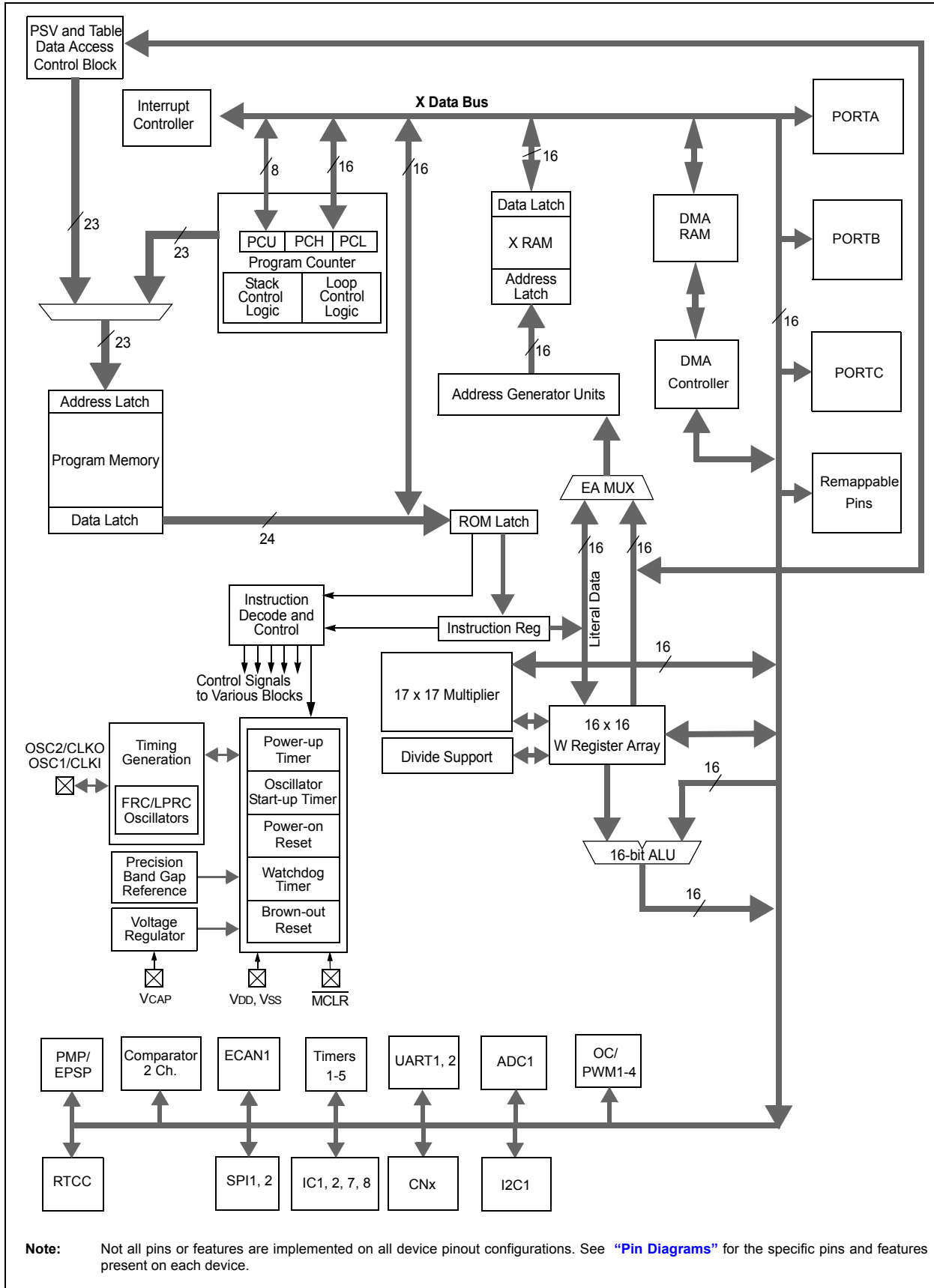


TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN12	I	Analog		Analog input channels.
CLKI	I	ST/CMOS	No	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CLKO	O	—	No	Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/CMOS	No	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	No	32.768 kHz low-power oscillator crystal output.
CN0-CN30	I	ST	No	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1-IC2	I	ST	Yes	Capture inputs 1/2
IC7-IC8	I	ST	Yes	Capture inputs 7/8.
OCFA	I	ST	Yes	Compare Fault A input (for Compare Channels 1, 2, 3 and 4).
OC1-OC4	O	—	Yes	Compare outputs 1 through 4.
INT0	I	ST	No	External interrupt 0.
INT1	I	ST	Yes	External interrupt 1.
INT2	I	ST	Yes	External interrupt 2.
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port.
RA7-RA10	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC9	I/O	ST	No	PORTC is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	Yes	Timer3 external clock input.
T4CK	I	ST	Yes	Timer4 external clock input.
T5CK	I	ST	Yes	Timer5 external clock input.
$\overline{U1CTS}$	I	ST	Yes	UART1 clear to send.
U1RTS	O	—	Yes	UART1 ready to send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
$\overline{U2CTS}$	I	ST	Yes	UART2 clear to send.
U2RTS	O	—	Yes	UART2 ready to send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
SS1	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 PPS = Peripheral Pin Select TTL = TTL input buffer

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
C1RX	I	ST	Yes	ECAN1 bus receive pin.
C1TX	O	—	Yes	ECAN1 bus transmit pin.
RTCC	O	—	No	Real-Time Clock Alarm Output.
CVREF	O	ANA	No	Comparator Voltage Reference Output.
C1IN-	I	ANA	No	Comparator 1 Negative Input.
C1IN+	I	ANA	No	Comparator 1 Positive Input.
C1OUT	O	—	Yes	Comparator 1 Output.
C2IN-	I	ANA	No	Comparator 2 Negative Input.
C2IN+	I	ANA	No	Comparator 2 Positive Input.
C2OUT	O	—	Yes	Comparator 2 Output.
PMA0	I/O	TTL/ST	No	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	I/O	TTL/ST	No	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2 -PMPA10	O	—	No	Parallel Master Port Address (Demultiplexed Master Modes).
PMBE	O	—	No	Parallel Master Port Byte Enable Strobe.
PMCS1	O	—	No	Parallel Master Port Chip Select 1 Strobe.
PMD0-PMPD7	I/O	TTL/ST	No	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMRD	O	—	No	Parallel Master Port Read Strobe.
PMWR	O	—	No	Parallel Master Port Write Strobe.
PGED1	I/O	ST	No	Data I/O pin for programming/debugging communication channel 1.
PGEC1	I	ST	No	Clock input pin for programming/debugging communication channel 1.
PGED2	I/O	ST	No	Data I/O pin for programming/debugging communication channel 2.
PGEC2	I	ST	No	Clock input pin for programming/debugging communication channel 2.
PGED3	I/O	ST	No	Data I/O pin for programming/debugging communication channel 3.
PGEC3	I	ST	No	Clock input pin for programming/debugging communication channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.
VREF+	I	Analog	No	Analog voltage reference (high) input.
VREF-	I	Analog	No	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 PPS = Peripheral Pin Select TTL = TTL input buffer

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

Note 1: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “*dsPIC33F/PIC24H Family Reference Manual*”. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 family of 16-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 “Decoupling Capacitors”**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 “Decoupling Capacitors”**)
- VCAP (see **Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)”**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 “Master Clear (MCLR) Pin”**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 “ICSP Pins”**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 “External Oscillator Pins”**)

Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

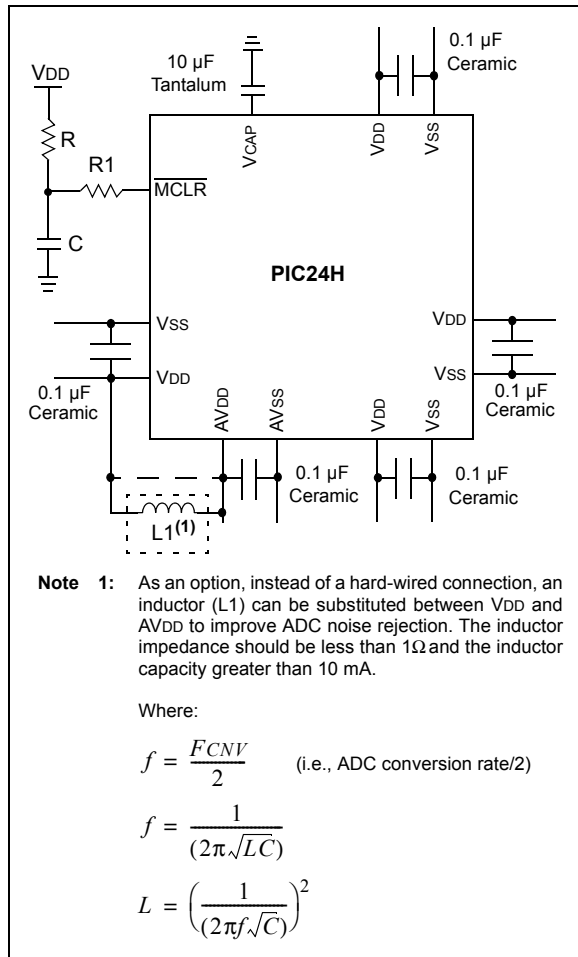
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 μF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including MCUs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 5 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, preferably surface mount connected within one-eighths inch of the VCAP pin connected to ground. The type can be ceramic or tantalum. Refer to [Section 28.0 “Electrical Characteristics”](#) for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to [Section 25.2 “On-Chip Voltage Regulator”](#) for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

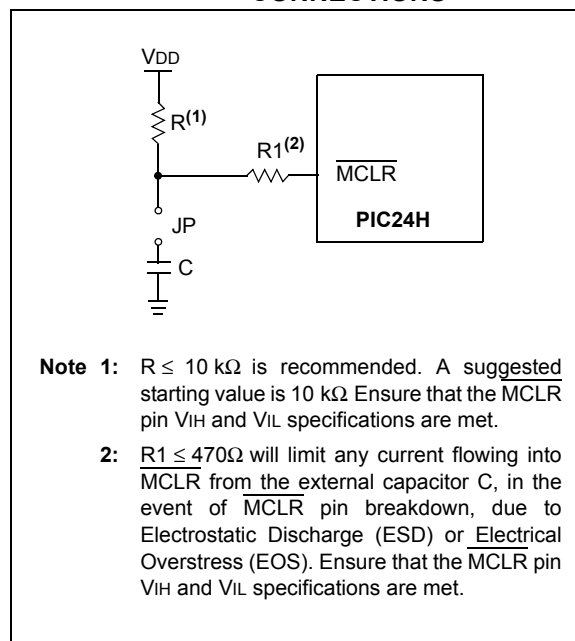
- Device Reset
- Device programming and debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in [Figure 2-2](#), it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in [Figure 2-2](#) within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- “Using MPLAB® ICD 3” (poster) DS51765
- “MPLAB® ICD 3 Design Advisory” DS51764
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” DS51616
- “Using MPLAB® REAL ICE™” (poster) DS51749

2.6 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to [Section 9.0 “Oscillator Configuration”](#) for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in [Figure 2-3](#). Recommendations for crystals and ceramic resonators are provided in [Table 2-1](#) and [Table 2-2](#), respectively.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

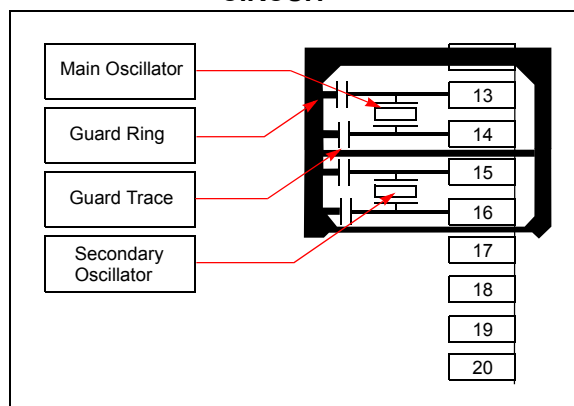


TABLE 2-1: CRYSTAL RECOMMENDATIONS

Part Number	Vendor	Freq.	Load Cap.	Package Case	Frequency Tolerance	Mounting Type	Operating Temperature
ECS-40-20-4DN	ECS Inc.	4 MHz	20 pF	HC49/US	±30 ppm	TH	-40°C to +85°C
ECS-80-18-4DN	ECS Inc.	8 MHz	18 pF	HC49/US	±30 ppm	TH	-40°C to +85°C
ECS-100-18-4-DN	ECS Inc.	10 MHz	18 pF	HC49/US	±30 ppm	TH	-40°C to +85°C
ECS-200-20-4DN	ECS Inc.	20 MHz	20 pF	HC49/US	±30 ppm	TH	-40°C to +85°C
ECS-40-20-5G3XDS-TR	ECS Inc.	4 MHz	20 pF	HC49/US	±30 ppm	SM	-40°C to +125°C
ECS-80-20-5G3XDS-TR	ECS Inc.	8 MHz	20 pF	HC49/US	±30 ppm	SM	-40°C to +125°C
ECS-100-20-5G3XDS-TR	ECS Inc.	10 MHz	20 pF	HC49/US	±30 ppm	SM	-40°C to +125°C
ECS-200-20-5G3XDS-TR	ECS Inc.	20 MHz	20 pF	HC49/US	±30 ppm	SM	-40°C to 125°C
NX3225SA 20MHZ AT-W	NDK	20 MHz	8 pF	3.2 mm x 2.5 mm	±50 ppm	SM	-40°C to 125°C

Legend: TH = Through Hole SM = Surface Mount

TABLE 2-2: RESONATOR RECOMMENDATIONS

Part Number	Vendor	Freq.	Load Cap.	Package Case	Frequency Tolerance	Mounting Type	Operating Temperature
FCR4.0M5T	TDK Corp.	4 MHz	N/A	Radial	±0.5%	TH	-40°C to +85°C
FCR8.0M5	TDK Corp.	8 MHz	N/A	Radial	±0.5%	TH	-40°C to +85°C
HWZT-10.00MD	TDK Corp.	10 MHz	N/A	Radial	±0.5%	TH	-40°C to +85°C
HWZT-20.00MD	TDK Corp.	20 MHz	N/A	Radial	±0.5%	TH	-40°C to +85°C

Legend: TH = Through Hole

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to ≤8 MHz for start-up with the PLL enabled to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration word.

2.8 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 3 or REAL ICE is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as “digital” pins, by setting all bits in the AD1PCFGL register.

The bits in this register that correspond to the A/D pins that are initialized by MPLAB ICD 3 or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must clear the corresponding bits in the AD1PCFGL register during initialization of the ADC module.

When MPLAB ICD 3 or REAL ICE is used as a programmer, the user application firmware must correctly configure the AD1PCFGL register. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic ‘0’, which may affect user application functionality.

2.9 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic-low state.

Alternatively, connect a 1k to 10k resistor between Vss and the unused pins.

3.0 CPU

Note 1: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. “CPU”** (DS70204) of the *“dsPIC33F/PIC24H Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

3.1 Overview

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and addressing modes. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (*MOV.D*) instruction and the table instructions. Overhead-free, single-cycle program loop constructs are supported using the *REPEAT* instruction, which is interruptible at any point.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices have sixteen, 16-bit working registers in the programmer’s model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing $A + B = C$ operations to be executed in a single cycle.

A block diagram of the CPU is shown in [Figure 3-1](#), and the programmer’s model for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 is shown in [Figure 3-2](#).

3.2 Data Addressing Overview

The data space can be linearly addressed as 32K words or 64 Kbytes using an Address Generation Unit (AGU). The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space.

The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers, but may be used as general purpose RAM.

3.3 Special MCU Features

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 features a 17-bit by 17-bit, single-cycle multiplier. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication makes mixed-sign multiplication possible.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices support 16/16 and 32/16 integer divide operations. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A multi-bit data shifter is used to perform up to a 16-bit, left or right shift in a single cycle.

FIGURE 3-1: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 CPU CORE BLOCK DIAGRAM

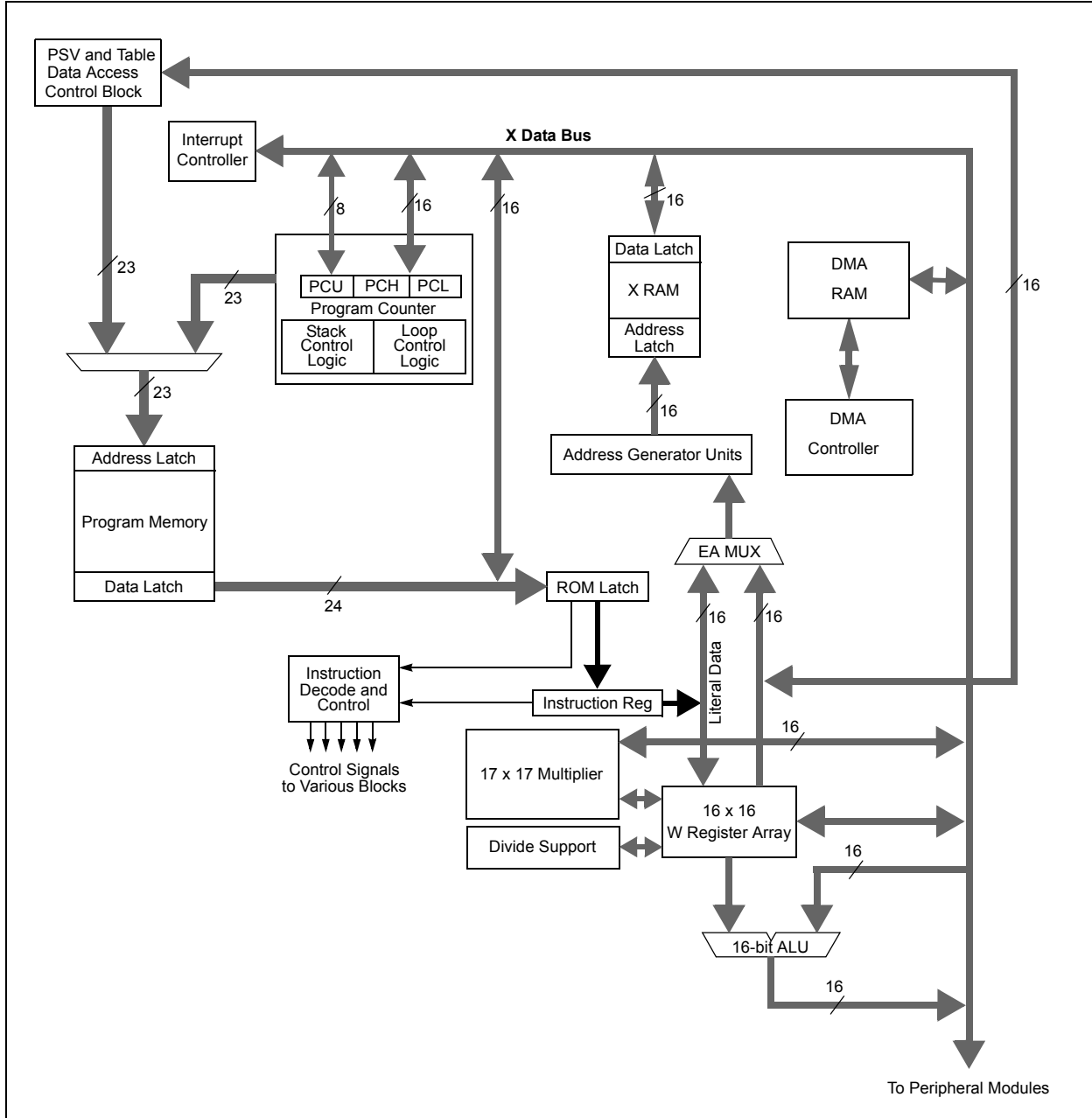
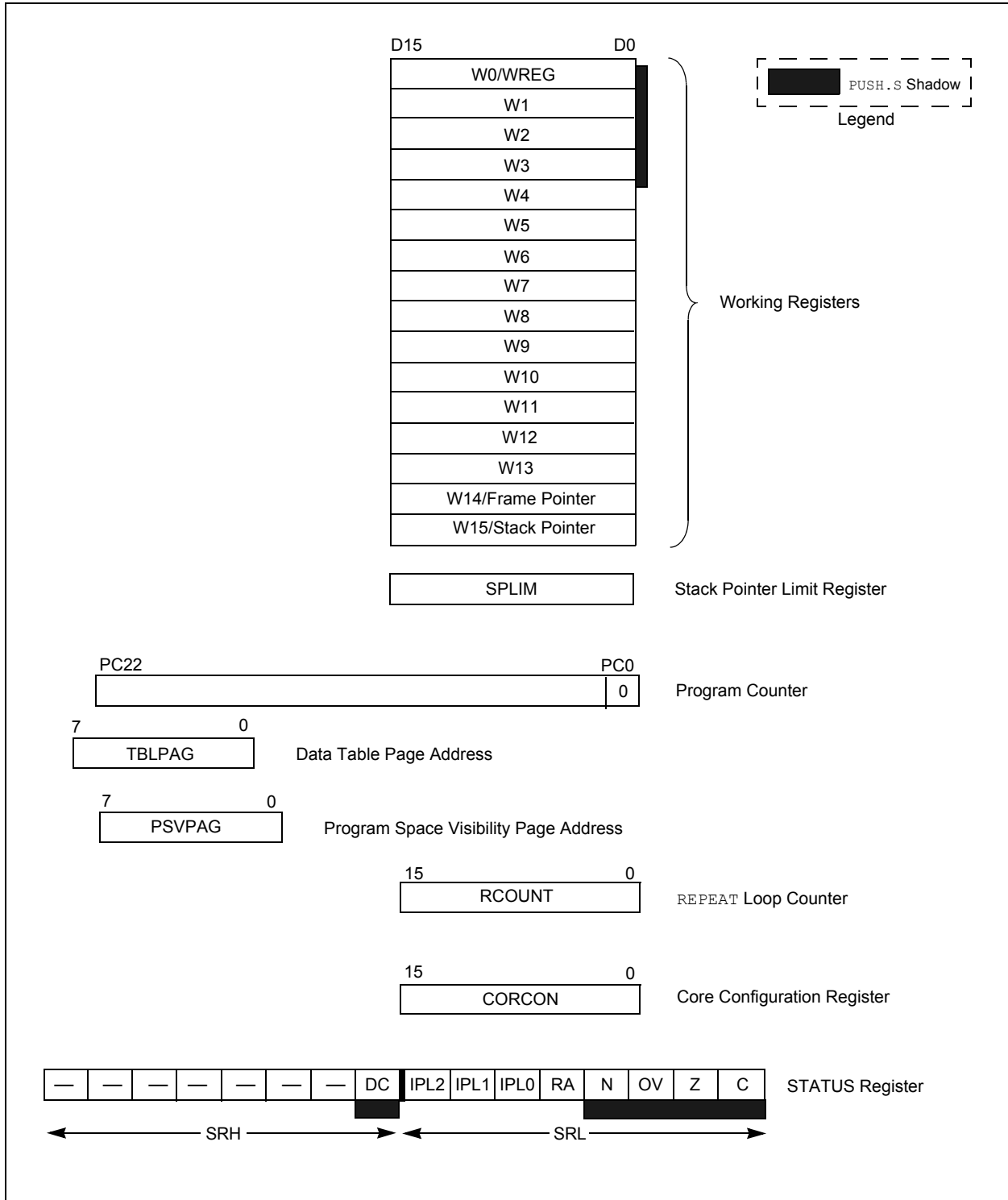


FIGURE 3-2: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 PROGRAMMER'S MODEL



3.4 CPU Resources

Many useful resources related to the CPU are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

<p>Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555</p>
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3.4.1 KEY RESOURCES

- **Section 2. “CPU”** (DS70204)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

3.5 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8
R/W-0 ⁽¹⁾	R/W-0 ⁽²⁾	R/W-0 ⁽²⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0> ⁽²⁾			RA	N	OV	Z	C
bit 7							bit 0

Legend:		
C = Clear only bit	R = Readable bit	U = Unimplemented bit, read as '0'
S = Set only bit	W = Writable bit	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-9 **Unimplemented:** Read as '0'
- bit 8 **DC:** MCU ALU Half Carry/Borrow bit
 - 1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
 - 0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
- bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits⁽²⁾
 - 111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
 - 110 = CPU Interrupt Priority Level is 6 (14)
 - 101 = CPU Interrupt Priority Level is 5 (13)
 - 100 = CPU Interrupt Priority Level is 4 (12)
 - 011 = CPU Interrupt Priority Level is 3 (11)
 - 010 = CPU Interrupt Priority Level is 2 (10)
 - 001 = CPU Interrupt Priority Level is 1 (9)
 - 000 = CPU Interrupt Priority Level is 0 (8)
- bit 4 **RA:** REPEAT Loop Active bit
 - 1 = REPEAT loop in progress
 - 0 = REPEAT loop not in progress
- bit 3 **N:** MCU ALU Negative bit
 - 1 = Result was negative
 - 0 = Result was non-negative (zero or positive)
- bit 2 **OV:** MCU ALU Overflow bit
 - This bit is used for signed arithmetic (two's complement). It indicates an overflow of a magnitude that causes the sign bit to change state.
 - 1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
 - 0 = No overflow occurred
- bit 1 **Z:** MCU ALU Zero bit
 - 1 = An operation that affects the Z bit has set it at some time in the past
 - 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
- bit 0 **C:** MCU ALU Carry/Borrow bit
 - 1 = A carry-out from the Most Significant bit of the result occurred
 - 0 = No carry-out from the Most Significant bit of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read only when the NSTDIS bit (INTCON1<15>) = 1.

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3 ⁽¹⁾	PSV	—	—
bit 7							bit 0

Legend:	C = Clear only bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
0' = Bit is cleared	'x' = Bit is unknown	U = Unimplemented bit, read as '0'	

- bit 15-4 **Unimplemented:** Read as '0'
- bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽¹⁾
 - 1 = CPU interrupt priority level is greater than 7
 - 0 = CPU interrupt priority level is 7 or less
- bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
 - 1 = Program space visible in data space
 - 0 = Program space not visible in data space
- bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

3.6 Arithmetic Logic Unit (ALU)

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

For information on the SR bits affected by each instruction, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

3.6.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.6.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.6.3 MULTI-BIT DATA SHIFTER

The multi-bit data shifter is capable of performing up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either a working register or a memory location.

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

NOTES:

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. “Program Memory”** (DS70203) of the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

4.1 Program Address Space

The program address memory space of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.6 “Interfacing Program and Data Memory Spaces”**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The memory map for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices is shown in **Figure 4-1**.

FIGURE 4-1: PROGRAM MEMORY MAP FOR PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 DEVICES

