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PIC32MK GENERAL PURPOSE AND MOTOR CONTROL (GP/MC) FAMILY

32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps

Operating Conditions: 2.2V to 3.6V

- -40ºC to +85ºC, DC to 120 MHz
- -40ºC to +125ºC, DC to 80 MHz

Core: 120 MHz (up to 198 DMIPS)

- MIPS32® microAptiv™ MCU core with Floating Point Unit
- microMIPS™ mode for up to 40% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating and fractional math
- Code-efficient (C and Assembly) architecture
- Two 32-bit core register files to reduce interrupt latency

Clock Management

- 8 MHz ±5% (FRC) internal oscillator 0ºC to +70ºC
- Programmable PLLs and oscillator clock sources:
  - HS and EC clock modes
- Secondary USB PLL
- 32 kHz Internal Low-power RC oscillator (LPRC)
- Independent external low-power 32 kHz crystal oscillator
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timers (WDT) and Deadman Timer (DMT)
- Fast wake-up and start-up
- Four Fractional clock out (REFCLKO) modules

Power Management

- Low-power management modes (Deep Sleep, Sleep, and Idle)
- Integrated:
  - Power-on Reset (POR) and Brown-out Reset (BOR)
- On-board capacitorless regulator

Motor Control PWM

- Eight PWM pairs
- Six additional Single-Ended PWM modules
- Dead Time for rising and falling edges
- Dead-Time Compensation
- 8.33 ns PWM Resolution
- Clock Chopping for High-Frequency Operation
- PWM Support for:
  - DC/DC, AC/DC, inverters, PFC, lighting
  - BLDC, PMSM, ACIM, SRM motors
- Choice of six Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

Motor Encoder Interface

- Six Quadrature Encoder Interface (QEI) modules:
  - Four inputs: Phase A, Phase B, Home, and Index

Audio/Graphics/Touch Interfaces

- External Graphics interfaces through PMP
- Up to six I^2S audio data communication interfaces
- Up to six SPI audio control interfaces
- Programmable audio master clock:
  - Generation of fractional clock frequencies
  - Can be synchronized with USB clock
  - Can be tuned in run-time

Unique Features

- Permanent non-volatile 4-word unique device serial number

Direct Memory Access (DMA)

- Up to eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)
- Up to 64 KB transfers

Security Features

- Advanced Memory Protection:
  - Peripheral and memory region access control

Advanced Analog Features

- 12-bit ADC module:
  - 25.45 Msps 12-bit mode or 33.79 Msps 8-bit mode
  - 7 individual ADC modules
  - 3.75 Msps per S&H with dedicated DMA
  - Up to 42 analog inputs
- Flexible and independent ADC trigger sources
- Four Op amps and five Comparators
- Up to three 12-bit CDACs
- Internal temperature sensor ±2ºC accuracy
- Capacitive Touch Divider (CVD)

Communication Interfaces

- Up to four CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Up to six UART modules (up to 25 Mbps):
  - Supports LIN 1.2 and IrDA® protocols
- Six SPI/I^2S modules (SPI 50 Mbps)
- Parallel Master Port (PMP)
- Up to two FS USB 2.0-compliant On-The-Go (OTG) controllers
- Peripheral Pin Select (PPS) to enable remappable pin functions

Timers/Output Compare/Input Capture/RTCC

- Up to 14 16-bit or one 16-bit and eight 32-bit timers/counters for GP and MC devices and six additional QEI 32-bit timers for MC devices
- 16 Output Compare (OC) modules
- 16 Input Capture (IC) modules
- PPS to enable function remap
- Real-Time Clock and Calendar (RTCC) module

Input/Output

- 5V-tolerant pins with up to 22 mA source/sink
- Selectable internal open drain, pull-ups, and pull-downs
- External interrupts on all I/O pins
- Five programmable edge/level-triggered interrupt pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1 -40ºC to +125ºC) (planned)
- Class B Safety Library, IEC 60730 (planned)
- Back-up internal oscillator
- Clock monitor with back-up internal oscillator
- Global register locking

Debugger Development Support

- In-circuit and in-application programming
- 2-wire or 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Software and Tools Support

- C/C++ compiler with native DSP/fractional support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™ and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPENRTOS®, Micriμm® μC/OS™, and SEGGER embOS®

Packages

Type	QFN	TQFP	
Pin Count	64	64	100
I/O Pins (up to)	48 (GP devices) 49 (MC devices)	48 (GP devices) 49 (MC devices)	77 (GP devices) 78 (MC devices)
Contact/Lead Pitch	0.50 mm	0.50 mm	0.40 mm
Dimensions	9x9x0.9 mm	10x10x1 mm	12x12x1 mm

TABLE 1: PIC32MK GENERAL PURPOSE (GP) FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	EE Memory (KB)	Floating Point Unit (FPU)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals						DMA Channels (Programmable/Dedicated)	ADC (Channels)	Op amp/Comparator	USB 2.0 FS OTG	PMP	RTCC	REFCLK	CDAC	CTMU	I/O Pins	JTAG/ICSP	Trace
								Remappable Pins	Timers/Capture/Compare(1)	UART	SPI/I²S	External Interrupts(2)	CAN 2.0B												
PIC32MK0512GPD064	512	128	4	Y	64	TQFP, QFN	16	Y	9/16/16	6	6	5	—	8/13	26	4/5	1	Y	1	4	3	1	48	Y	Y
PIC32MK1024GPD064	1024	256																							
PIC32MK0512GPD100	512	128	4	Y	100	TQFP	16	Y	9/16/16	6	6	5	—	8/13	42	4/5	2	Y	1	4	3	1	77	Y	Y
PIC32MK1024GPD100	1024	256																							
PIC32MK0512GPE064	512	128	4	Y	64	TQFP, QFN	16	Y	9/16/16	6	6	5	4	8/13	26	4/5	1	Y	1	4	3	1	48	Y	Y
PIC32MK1024GPE064	1024	256																							
PIC32MK0512GPE100	512	128	4	Y	100	TQFP	16	Y	9/16/16	6	6	5	4	8/13	42	4/5	2	Y	1	4	3	1	77	Y	Y
PIC32MK1024GPE100	1024	256																							

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.
Legend: An '—' indicates this feature is not available for the listed device.

TABLE 2: PIC32MK MOTOR CONTROL (MC) FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	EE Memory (KB)	Floating Point Unit (FPU)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals						DMA Channels (Programmable/Dedicated)	ADC (Channels)	Op amp/Comparator	USB 2.0 FS OTG	PMP	QEI	MCPWM	RTCC	REFCLK	CDAC	CTMU	I/O Pins	JTAG/ICSP	Trace
								Remappable Pins	Timers/Capture/Compare(1)	UART	SPI/I²S	External Interrupts(2)	CAN 2.0B														
PIC32MK0512MCF064	512	128	4	Y	64	TQFP, QFN	16	Y	9/16/16	6	6	5	4	8/13	26	4/5	1	Y	6	12	1	4	3	1	49	Y	Y
PIC32MK1024MCF064	1024	256																									
PIC32MK0512MCF100	512	128	4	Y	100	TQFP	16	Y	9/16/16	6	6	5	4	8/13	42	4/5	2	Y	6	12	1	4	3	1	78	Y	Y
PIC32MK1024MCF100	1024	256																									

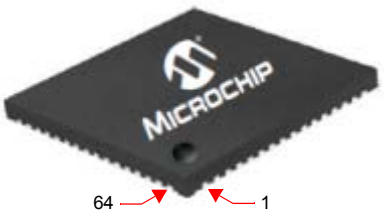
Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.

Device Pin Tables

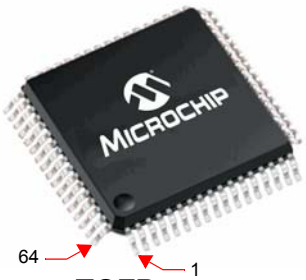
TABLE 3: PIN NAMES FOR 64-PIN GENERAL PURPOSE (GPD/GPE) DEVICES

64-PIN QFN(4) AND TQFP (TOP VIEW)

PIC32MK0512GPD064
PIC32MK0512GPE064
PIC32MK1024GPD064
PIC32MK1024GPE064



QFN(4)



TQFP

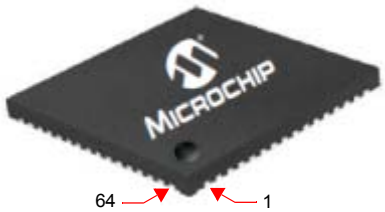
Pin #	Full Pin Name	Pin #	Full Pin Name
1	TCK/RPA7/PMD5/RA7	33	OA5IN+/CDAC1/AN24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
2	RPB14/VBUSON1/PMD6/RB14	34	VBUS
3	RPB15/PMD7/RB15	35	VUSB3V3
4	AN19/RPG6/PMA5/RG6	36	D1-
5	AN18/RPG7/PMA4/RG7(6)	37	D1+
6	AN17/RPG8/PMA3/RG8(7)	38	VDD
7	$\overline{\text{MCLR}}$	39	OSC1/CLKI/AN49/RPC12/RC12
8	AN16/RPG9/PMA2/RG9	40	OSC2/CLKO/RPC15/RC15
9	VSS	41	VSS
10	VDD	42	VBAT(8)
11	AN10/RPA12/RA12	43	PGED2/RPB5/USBID1/RB5(7)
12	AN9/RPA11/RA11	44	PGEC2/RPB6/SCK2/PMA15/RB6(6)
13	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	45	CDAC2/AN48/RPC10/PMA14/RC10
14	OA2IN+/AN1/C2IN1+/RPA1/RA1	46	OA5OUT/AN25/C5IN4-/RPB7/SCK1/INT0/RB7
15	PGED3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	47	SOSCI/RPC13(5)/RC13(5)
16	PGEC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/RPB1/CTED1/PMA6/RB1	48	SOSCO/RPB8(5)/RB8(5)
17	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	49	TMS/OA5IN-/AN27/C5IN1-/RPB9/RB9
18	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	50	TRCLK/RPC6/RC6
19	AVDD	51	TRD0/RPC7/RC7
20	AVSS	52	TRD1/RPC8/PMWR/RC8
21	OA3OUT/AN6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	53	TRD2/RPD5/PMRD/RD5
22	OA3IN-/AN7/C3IN1-/C4IN1-/RPC1/PMA7/RC1	54	TRD3/RPD6/RD6
23	OA3IN+/AN8/C3IN1+/C3IN3-/RPC2/PMA13/RC2	55	RPC9/RC9
24	AN11/C1IN2-/PMA12/RC11	56	VSS
25	VSS	57	VDD
26	VDD	58	RPF0/RF0
27	AN12/C2IN2-/C5IN2-/PMA11/RE12(7)	59	RPF1/RF1
28	AN13/C3IN2-/PMA10/RE13(6)	60	RPB10/PMD0/RB10
29	AN14/RPE14/PMA1/RE14	61	RPB11/PMD1/RB11
30	AN15/RPE15/PMA0/RE15	62	RPB12/PMD2/RB12
31	TDI/CDAC3/AN26/RPA8/PMA9/RA8(7)	63	RPB13/CTPLS/PMD3/RB13
32	RPB4/PMA8/RB4(6)	64	TDO/PMD4/RA10

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
5: Functions are restricted to input functions only and inputs will be slower than the standard inputs.
6: The I2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I2C master/slave clock, that is SCL.
7: The I2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I2C data I/O, that is, SDA.
8: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

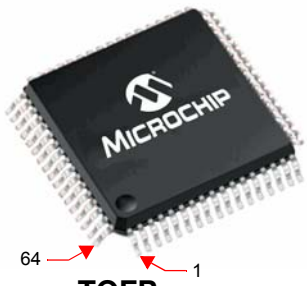
TABLE 4: PIN NAMES FOR 64-PIN MOTOR CONTROL (MCF) DEVICES

64-PIN QFN(4) AND TQFP (TOP VIEW)

PIC32MK0512MCF064
PIC32MK1024MCF064



QFN(4)



TQFP

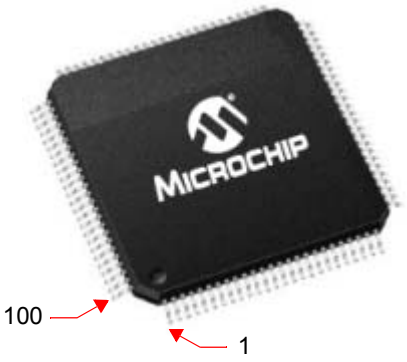
Pin #	Full Pin Name	Pin #	Full Pin Name
1	TCK/RPA7/PWM10H/PWM4L/PMPD5/RA7	33	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/T1G/RA4
2	RPB14/PWM1H/VBUSON1/PMPD6/RB14	34	VBUS
3	RPB15/PWM7H/PWM1L/PMPD7/RB15	35	VUSB3V3
4	AN19/CVD19/RPG6/PMPA5/RG6	36	D-
5	AN18/CVD18/RPG7/PMPA4/RG7(6)	37	D+
6	AN17/CVD17/RPG8/PMPA3/RG8(7)	38	VDD
7	MCLR	39	OSCI/CLKI/AN49/CVD49/RPC12/RC12
8	AN16/CVD16/RPG9/PMPA2/RG9	40	OSCO/CLKO/RPC15/RC15
9	VSS	41	VSS
10	VDD	42	RD8
11	AN10/CVD10/RPA12/RA12	43	PGED2/RPB5/USBID1/RB5(7)
12	AN9/CVD9/RPA11/USBOEN1/RA11	44	PGEC2/RPB6/SCK2/PMPA15/RB6(6)
13	OA2OUT/ANO/C2IN4-/C4IN3-/RPA0/RA0	45	DAC2/AN48/CVD48/RPC10/PMPA14/PSPCS/RC10
14	OA2IN+/AN1/C2IN1+/RPA1/RA1	46	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7
15	PGED3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	47	SOSCI/RPC13(5)/RC13(5)
16	PGEC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/RPB1/CTED1/PMPA6/RB1	48	SOSCO/RPB8(5)/RB8(5)
17	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	49	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9
18	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	50	TRCLK/RPC6/PWM6H/RC6
19	AVDD	51	TRD0/RPC7/PWM12H/PWM6L/RC7
20	AVSS	52	TRD1/RPC8/PWM5H/PMPWR/PSPWR/RC8
21	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	53	TRD2/RPD5/PWM12H/PMPRD/PSPRD/RD5
22	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/PMPA7/RC1	54	TRD3/RPD6/PWM12L/RD6
23	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMPA13/RC2	55	RPC9/PWM11H/PWM5L/RC9
24	AN11/CVD11/C1IN2-/FLT4/PMPA12/RC11	56	VSS
25	VSS	57	VDD
26	VDD	58	RPF0/PWM11H/RF0
27	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMPA11/RE12(7)	59	RPF1/PWM11L/RF1
28	AN13/CVD13/C3IN2-/FLT6/PMPA10/RE13(6)	60	RPB10/PWM3H/PMPD0/RB10
29	AN14/CVD14/RPE14/FLT7/PMPA1/PSPA1/RE14	61	RPB11/PWM9H/PWM3L/PMPD1/RB11
30	AN15/CVD15/RPE15/FLT8/PMPA0/PSPA0/RE15	62	RPB12/PWM2H/PMPD2/RB12
31	TDI/DAC3/AN26/CVD26/RPA8/PMPA9/RA8(7)	63	RPB13/PWM8H/PWM2L/CTPLS/PMPD3/RB13
32	FLT15/RPB4/PMPA8/RB4(6)	64	TDO/PWM4H/PMPD4/RA10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
5: Functions are restricted to input functions only and inputs will be slower than standard inputs.
6: The I^2C Library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
7: The I^2C Library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).

TABLE 5: PIN NAMES FOR 100-PIN GENERAL PURPOSE (GPD/GPE) DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MK0512GPD100
PIC32MK0512GPE100
PIC32MK1024GPD100
PIC32MK1024GPE100



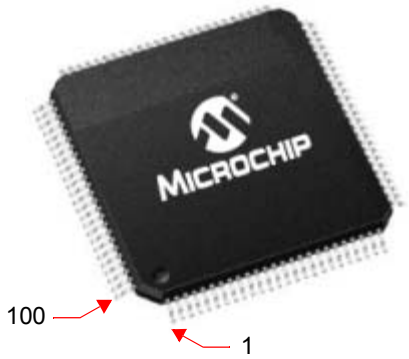
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/PMA23/RG15	36	VSS
2	VDD	37	VDD
3	TCK/RPA7/PMD5/RA7	38	AN35/RG11
4	RPB14/VBUSON1/PMD6/RB14	39	AN36/RF13
5	RPB15/PMD7/RB15	40	AN37/RF12
6	RD1	41(6)	AN12/C2IN2-/C5IN2-/PMA11/RE12
7	RD2	42(5)	AN13/C3IN2-/PMA10/RE13
8	RPD3/RD3	43	AN14/RPE14/PMA1/RE14
9	RPD4/RD4	44	AN15/RPE15/PMA0/RE15
10	AN19/RPG6/VBUSON2/PMA5/RG6	45	VSS
11	AN18/RPG7/1/PMA4/RG7(5)	46	VDD
12	AN17/RPG8//PMA3/RG8(6)	47	AN38/RD14
13	$\overline{\text{MCLR}}$	48	AN39/RD15
14	AN16/RPG9/PMA2/RG9	49	TDI/CDAC3/AN26/RPA8/PMA9/RA8(6)
15	VSS	50	RPB4/PMA8/RB4(5)
16	VDD	51	OA5IN+/CDAC1/AN24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
17	AN22/RG10	52	AN40/RPE0/RE0
18	AN21/RE8	53	AN41/RPE1/RE1
19	AN20/RE9	54	VBUS1
20	AN10/RPA12/RA12	55	VUSB3V3
21	AN9/RPA11/RA11	56	D1-
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	57	D1+
23	OA2IN+/AN1/C2IN1+/RPA1/RA1	58	VBUS2
24	PGED3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	59	D2-
25	PGEC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	60	D2+
26	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	61	AN45/RF5
27	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	62	VDD
28	VREF-/AN33/PMA7/RF9	63	OSC1/CLKI/AN49/RPC12/RC12
29	VREF+/AN34/PMA6/RF10	64	OSC2/CLKO/RPC15/RC15
30	AVDD	65	VSS
31	AVSS	66	AN46/RPA14/RA14
32	OA3OUT/AN6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	67	AN47/RPA15/RA15
33	OA3IN-/AN7/C3IN1-/C4IN1-/RPC1/RC1	68	VBAT(7)
34	OA3IN+/AN8/C3IN1+/C3IN3-/RPC2/PMA13/RC2	69	PGED2/RPB5/USBID1/RB5(6)
35	AN11/C1IN2-/PMA12/RC11	70	PGEC2/RPB6/SCK2/PMA15/RB6(5)

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).
7: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

TABLE 5: PIN NAMES FOR 100-PIN GENERAL PURPOSE (GPD/GPE) DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MK0512GPD100
PIC32MK0512GPE100
PIC32MK1024GPD100
PIC32MK1024GPE100



Pin #	Full Pin Name
71	CDAC2/AN48/RPC10/PMA14/RC10
72	OA5OUT/AN25/C5IN4-/RPB7/SCK1/INT0/RB7
73	SOSCI/RPC13/(4)RC13(4)
74	SOSCO/RPB8(4)/RB8(4)
75	VSS
76	TMS/OA5IN-/AN27/C5IN1-/RPB9/RB9
77	RPC6/USBID2/PMA16/RC6
78	RPC7/PMA17/RC7
79	PMD12/RD12
80	PMD13/RD13
81	RPC8/PMWR/RC8
82	RPD5/PMRD/RD5
83	RPD6/PMD14/RD6
84	RPC9/PMD15/RC9
85	VSS

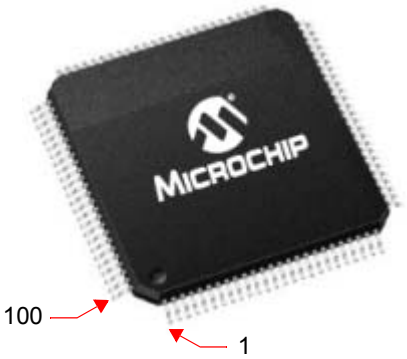
Pin #	Full Pin Name
86	VDD
87	RPF0/PMD11/RF0
88	RPF1/PMD10/RF1
89	RPG1/PMD9/RG1
90	RPG0/PMD8/RG0
91	TRCLK/PMA18/RF6
92	TRD3/PMA19/RF7
93	RPB10/PMD0/RB10
94	RPB11/PMD1/RB11
95	TRD2/PMA20/RG14
96	TRD1/RPG12/PMA21/RG12
97	TRD0/PMA22/RG13
98	RPB12/PMD2/RB12
99	RPB13/CTPLS/PMD3/RB13
100	TDO/PMD4/RA10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).
7: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

TABLE 6: PIN NAMES FOR 100-PIN MOTOR CONTROL (MCF) DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MK0512MCF100
PIC32MK1024MCF100



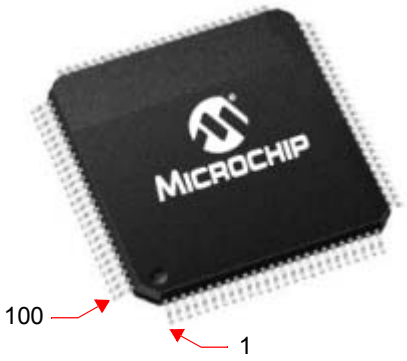
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/CVD23/PMPA23/RG15	36	VSS
2	VDD	37	VDD
3	TCK/RPA7/PWM10H/PWM4L/PMPD5/RA7	38	AN35/CVD35/RG11
4	RPB14/PWM1H/VBUSON1/PMPD6/RB14	39	AN36/CVD36/RF13
5	RPB15/PWM7H/PWM1L/PMPD7/RB15	40	AN37/CVD37/RF12
6	PWM11H/PWM5L/RD1	41	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMPA11/RE12(6)
7	PWM5H/RD2	42	AN13/CVD13/C3IN2-/FLT6/PMPA10/RE13(5)
8	RPD3/PWM12H/PWM6L/RD3	43	AN14/CVD14/RPE14/FLT7/PMPA1/PSPA1/RE14
9	RPD4/PWM6H/RD4	44	AN15/CVD15/RPE15/FLT8/PMPA0/PSPA0/RE15
10	AN19/CVD19/RPG6/VBUSON2/PMPA5/RG6	45	VSS
11	AN18/CVD18/RPG7/PMPA4/RG7(5)	46	VDD
12	AN17/CVD17/RPG8/PMPA3/RG8(6)	47	AN38/CVD38/RD14
13	$\overline{\text{MCLR}}$	48	AN39/CVD39/RD15
14	AN16/CVD16/RPG9/PMPA2/RG9	49	TDI/DAC3/AN26/CVD26/RPA8/PMPA9/RA8(6)
15	VSS	50	FLT15/RPB4/PMPA8/RB4(5)
16	VDD	51	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/T1G/RA4
17	AN22/CVD22/RG10	52	AN40/CVD40/RPE0/RE0
18	AN21/CVD21/RE8	53	AN41/CVD41/RPE1/RE1
19	AN20/CVD20/RE9	54	VBUS
20	AN10/CVD10/RPA12/USBOEN2/RA12	55	VUSB3V3
21	AN9/CVD9/RPA11/USBOEN1/RA11	56	D1-
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	57	D1+
23	OA2IN+/AN1/C2IN1+/RPA1/RA1	58	VBUS2
24	PGED3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	59	D2-
25	PGEC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	60	D2+
26	PGEC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	61	AN45/CVD45/RF5
27	PGED1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	62	VDD
28	VREF-/AN33/CVD33/PMPA7/RF9	63	OSCI/CLKI/AN49/CVD49/RPC12/RC12
29	VREF+/AN34/CVD34/PMPA6/RF10	64	OSCO/CLKO/RPC15/RC15
30	AVDD	65	VSS
31	AVss	66	AN46/CVD46/RPA14/RA14
32	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	67	AN47/CVD47/RPA15/RA15
33	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1	68	RD8
34	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMPA13/RC2	69	PGED2/RPB5/USBID1/RB5(6)
35	AN11/CVD11/C1IN2-/FLT4/PMPA12/RC11	70	PGEC2/RPB6/SCK2/PMPA15/RB6(5)

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).

TABLE 6: PIN NAMES FOR 100-PIN MOTOR CONTROL (MCF) DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MK0512MCF100
PIC32MK1024MCF100



Pin #	Full Pin Name	Pin #	Full Pin Name
71	DAC2/AN48/CVD48/RPC10/PMPA14/PSPCS/RC10	86	VDD
72	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7	87	RPF0/PWM11H/PMPD11/RF0
73	SOSCI/RPC13(4)/RC13(4)	88	RPF1/PWM11L/PMPD10/RF1
74	SOSCO/RPB8(4)/RB8(4)	89	RPG1/PMPD9/RG1
75	VSS	90	RPG0/PMPD8/RG0
76	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9	91	TRCLK/PMPA18/RF6
77	RPC6/USBID2/PMPA16/RC6	92	TRD3/PMPA19/RF7
78	RPC7/PMPA17/RC7	93	RPB10/PWM3H/PMPD0/RB10
79	PMPD12/RD12	94	RPB11/PWM9H/PWM3L/PMPD1/RB11
80	PMPD13/RD13	95	TRD2/PMPA20/RG14
81	RPC8/PMPWR/PSPWR/RC8	96	TRD1/RPG12/PMPA21/RG12
82	RPD5/PWM12H/PMPRD/PSPRD/RD5	97	TRD0/PMPA22/RG13
83	RPD6/PWM12L/PMPD14/RD6	98	RPB12/PWM2H/PMPD2/RB12
84	RPC9/PMPD15/RC9	99	RPB13/PWM8H/PWM2L/CTPLS/PMPD3/RB13
85	VSS	100	TDO/PWM4H/PMPD4/RA10

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 web site: http://www.microchip.com/pic32.

- **Section 1. "Introduction"** (DS60001127)
- **Section 4. "Prefetch Cache Module"** (DS60001119)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)
- **Section 39. "Op amp/Comparator"** (DS60001178)
- **Section 42. "Oscillators with Enhanced PLL"** (DS60001250)
- **Section 43. "Quadrature Encoder Interface (QEI)"** (DS60001346)
- **Section 44. "Motor Control PWM (MCPWM)** (DS60001393)
- **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193)
- **Section 58. "Data EEPROM"** (DS60001341)

NOTES:

1.0 DEVICE OVERVIEW

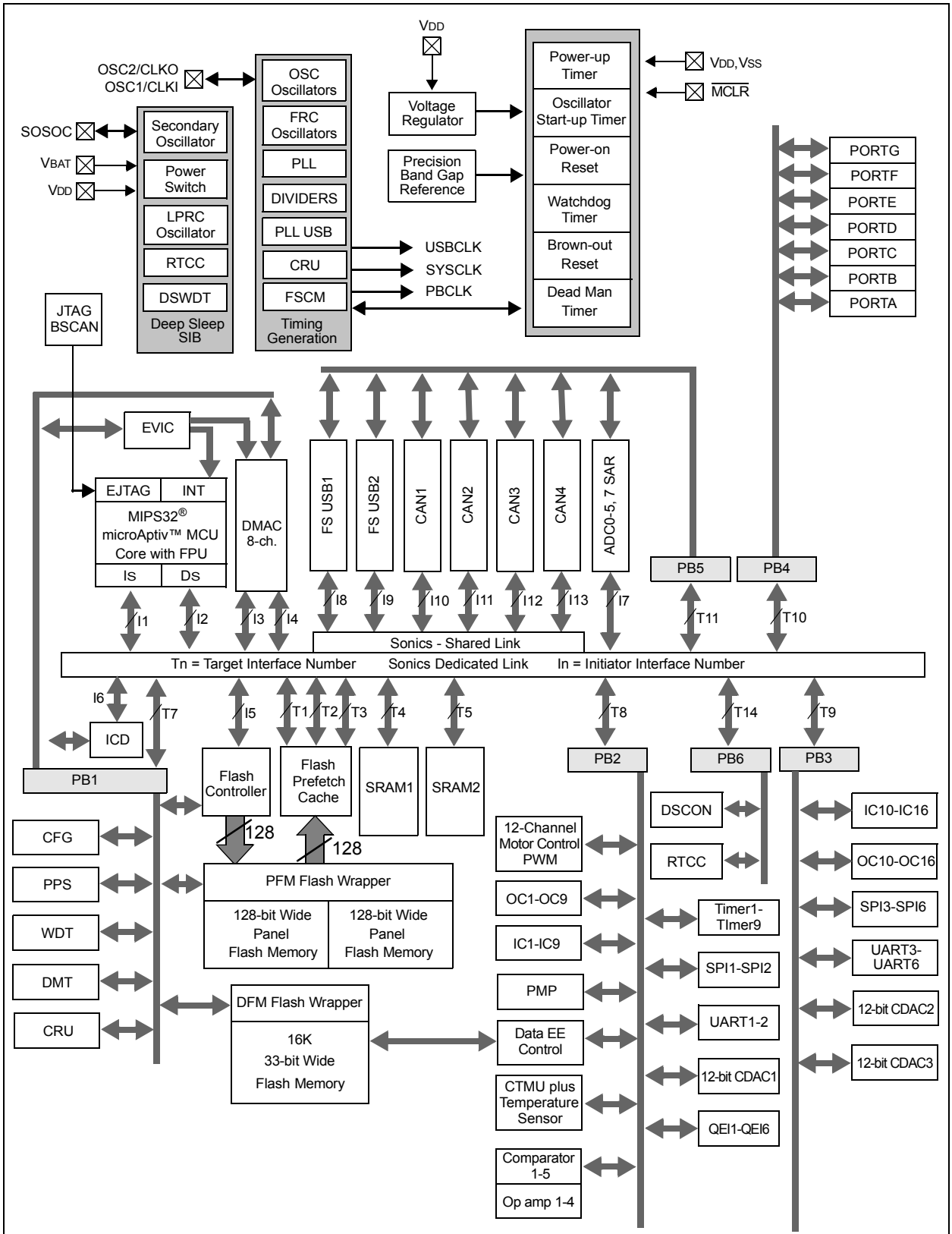
Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This data sheet contains device-specific information for PIC32MK GP/MC devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MK GP/MC family of devices.

Table 1-20 through Table 1-21 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 3 and Table 5).

FIGURE 1-1: PIC32MK GP/MC FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to the family feature tables (Table 1 and Table 2) for the list of available features by device.

TABLE 1-1: ADC1 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
AN0	22	13	I	Analog	Analog Input Channels
AN1	23	14	I	Analog	
AN2	24	15	I	Analog	
AN3	25	16	I	Analog	
AN4	26	17	I	Analog	
AN5	27	18	I	Analog	
AN6	32	21	I	Analog	
AN7	33	22	I	Analog	
AN8	34	23	I	Analog	
AN9	21	12	I	Analog	
AN10	20	11	I	Analog	
AN11	35	24	I	Analog	
AN12	41	27	I	Analog	
AN13	42	28	I	Analog	
AN14	43	29	I	Analog	
AN15	44	30	I	Analog	
AN16	14	8	I	Analog	
AN17	12	6	I	Analog	
AN18	11	5	I	Analog	
AN19	10	4	I	Analog	
AN20	19	—	I	Analog	
AN21	18	—	I	Analog	
AN22	17	—	I	Analog	
AN23	1	—	I	Analog	
AN24	51	33	I	Analog	
AN25	72	46	I	Analog	
AN26	49	31	I	Analog	
AN27	76	49	I	Analog	
AN33	28	—	I	Analog	
AN34	29	—	I	Analog	
AN35	38	—	I	Analog	
AN36	39	—	I	Analog	
AN37	40	—	I	Analog	
AN38	47	—	I	Analog	
AN39	48	—	I	Analog	
AN40	52	—	I	Analog	
AN41	53	—	I	Analog	
AN45	61	—	I	Analog	
AN46	66	—	I	Analog	
AN47	67	—	I	Analog	
AN48	71	45	I	Analog	
AN49	63	39	I	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CLKI	63	39	I	ST	External clock source input. Always associated with OSC1 pin function.
CLKO	64	40	O	CMOS	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	63	39	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	64	40	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	73	47	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	74	48	O	CMOS	32.768 low-power oscillator crystal output.
REFCLKI	PPS	PPS	I	—	One of several alternate REFCLKOx user-selectable input clock sources.
REFCLKO1	PPS	PPS	O	—	Reference Clock Generator Outputs 1-4
REFCLKO2	PPS	PPS	O	—	
REFCLKO3	PPS	PPS	O	—	
REFCLKO4	PPS	PPS	O	—	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-3: IC1 THROUGH IC16 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Input Capture					
IC1	PPS	PPS	I	ST	Input Capture Inputs 1-6
IC2	PPS	PPS	I	ST	
IC3	PPS	PPS	I	ST	
IC4	PPS	PPS	I	ST	
IC5	PPS	PPS	I	ST	
IC6	PPS	PPS	I	ST	
IC7	PPS	PPS	I	ST	
IC8	PPS	PPS	I	ST	
IC9	PPS	PPS	I	ST	
IC10	PPS	PPS	I	ST	
IC11	PPS	PPS	I	ST	
IC12	PPS	PPS	I	ST	
IC13	PPS	PPS	I	ST	
IC14	PPS	PPS	I	ST	
IC15	PPS	PPS	I	ST	
IC16	PPS	PPS	I	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-4: OC1 THROUGH OC16 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Output Compare					
OC1	PPS	PPS	O	—	Output Compare Outputs 1-16
OC2	PPS	PPS	O	—	
OC3	PPS	PPS	O	—	
OC4	PPS	PPS	O	—	
OC5	PPS	PPS	O	—	
OC6	PPS	PPS	O	—	
OC7	PPS	PPS	O	—	
OC8	PPS	PPS	O	—	
OC9	PPS	PPS	O	—	
OC10	PPS	PPS	O	—	
OC11	PPS	PPS	O	—	
OC12	PPS	PPS	O	—	
OC13	PPS	PPS	O	—	
OC14	PPS	PPS	O	—	
OC15	PPS	PPS	O	—	
OC16	PPS	PPS	O	—	
OCFA	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
External Interrupts					
INT0	72	46	I	ST	External Interrupt 0
INT1	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-6: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTA					
RA0	22	13	I/O	ST	PORTA is a bidirectional I/O port
RA1	23	14	I/O	ST	
RA4	51	33	I/O	ST	
RA7	3	1	I/O	ST	
RA8	49	31	I/O	ST	
RA10	100	64	I/O	ST	
RA11	21	12	I/O	ST	
RA12	20	11	I/O	ST	
RA14	66	—	I/O	ST	
RA15	67	—	I/O	ST	
PORTB					
RB0	24	15	I/O	ST	PORTB is a bidirectional I/O port
RB1	25	16	I/O	ST	
RB2	26	17	I/O	ST	
RB3	27	18	I/O	ST	
RB4	50	32	I/O	ST	
RB5	69	43	I/O	ST	
RB6	70	44	I/O	ST	
RB7	72	46	I/O	ST	
RB8	74	48	I	ST	
RB9	76	49	I/O	ST	
RB10	93	60	I/O	ST	
RB11	94	61	I/O	ST	
RB12	98	62	I/O	ST	
RB13	99	63	I/O	ST	
RB14	4	2	I/O	ST	
RB15	5	3	I/O	ST	
PORTC					
RC0	32	21	I/O	ST	PORTC is a bidirectional I/O port
RC1	33	22	I/O	ST	
RC2	34	23	I/O	ST	
RC6	77	50	I/O	ST	
RC7	78	51	I/O	ST	
RC8	81	52	I/O	ST	
RC9	84	55	I/O	ST	
RC10	71	45	I/O	ST	
RC11	35	24	I/O	ST	
RC12	63	39	I/O	ST	
RC13	73	47	I	ST	
RC15	64	40	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

TABLE 1-6: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTD					
RD1	6	—	I/O	ST	PORTD is a bidirectional I/O port
RD2	7	—	I/O	ST	
RD3	8	—	I/O	ST	
RD4	9	—	I/O	ST	
RD5	82	53	I/O	ST	
RD6	83	54	I/O	ST	
RD8(3)	68	42	I/O	ST	
RD12	79	—	I/O	ST	
RD13	80	—	I/O	ST	
RD14	47	—	I/O	ST	
RD15	48	—	I/O	ST	
PORTE					
RE0	52	—	I/O	ST	PORTE is a bidirectional I/O port
RE1	53	—	I/O	ST	
RE8	18	—	I/O	ST	
RE9	19	—	I/O	ST	
RE12	41	27	I/O	ST	
RE13	42	28	I/O	ST	
RE14	43	29	I/O	ST	
RE15	44	30	I/O	ST	
PORTF					
RF0	87	58	I/O	ST	PORTF is a bidirectional I/O port
RF1	88	59	I/O	ST	
RF5	61	—	I/O	ST	
RF6	91	—	I/O	ST	
RF7	92	—	I/O	ST	
RF9	28	—	I/O	ST	
RF10	29	—	I/O	ST	
RF12	40	—	I/O	ST	
RF13	39	—	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

TABLE 1-6: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTG					
RG0	90	—	I/O	ST	PORTG is a bidirectional I/O port
RG1	89	—	I/O	ST	
RG6	10	4	I/O	ST	
RG7	11	5	I/O	ST	
RG8	12	6	I/O	ST	
RG9	14	8	I/O	ST	
RG10	17	—	I/O	ST	
RG11	38	—	I/O	ST	
RG12	96	—	I/O	ST	
RG13	97	—	I/O	ST	
RG14	95	—	I/O	ST	
RG15	1	—	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

TABLE 1-7: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Universal Asynchronous Receiver Transmitter 1					
U1RX	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	O	—	UART1 Transmit
U1CTS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2					
U2RX	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	O	—	UART2 Transmit
U2CTS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3					
U3RX	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	O	—	UART3 Transmit
U3CTS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4					
U4RX	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	O	—	UART4 Transmit
U4CTS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5					
U5RX	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	O	—	UART5 Transmit
U5CTS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6					
U6RX	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	O	—	UART6 Transmit
U6CTS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-8: SPI1 THROUGH SPI 6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Serial Peripheral Interface 1					
SCK1	72	46	I/O	ST/CMOS	SPI1 Synchronous Serial Clock Input/Output
SDI1	PPS	PPS	I	ST	SPI1 Data In
SDO1	PPS	PPS	O	CMOS	SPI1 Data Out
SS1	PPS	PPS	I/O	ST/CMOS	SPI1 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 2					
SCK2	70	44	I/O	ST/CMOS	SPI2 Synchronous Serial Clock Input/output
SDI2	PPS	PPS	I	ST	SPI2 Data In
SDO2	PPS	PPS	O	CMOS	SPI2 Data Out
SS2	PPS	PPS	I/O	ST/CMOS	SPI2 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 3					
SCK3	PPS	PPS	I/O	ST/CMOS	SPI3 Synchronous Serial Clock Input/Output
SDI3	PPS	PPS	I	ST	SPI3 Data In
SDO3	PPS	PPS	O	CMOS	SPI3 Data Out
SS3	PPS	PPS	I/O	ST/CMOS	SPI3 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 4					
SCK4	PPS	PPS	I/O	ST/CMOS	SPI4 Synchronous Serial Clock Input/Output
SDI4	PPS	PPS	I	ST	SPI4 Data In
SDO4	PPS	PPS	O	CMOS	SPI4 Data Out
SS4	PPS	PPS	I/O	ST/CMOS	SPI4 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 5					
SCK5	PPS	PPS	I/O	ST/CMOS	SPI5 Synchronous Serial Clock Input/Output
SDI5	PPS	PPS	I	ST	SPI5 Data In
SDO5	PPS	PPS	O	CMOS	SPI5 Data Out
SS5	PPS	PPS	I/O	ST/CMOS	SPI5 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 6					
SCK6	PPS	PPS	I/O	ST/CMOS	SPI6 Synchronous Serial Clock Input/Output
SDI6	PPS	PPS	I	ST	SPI6 Data In
SDO6	PPS	PPS	O	CMOS	SPI6 Data Out
SS6	PPS	PPS	I/O	ST/CMOS	SPI6 Slave Synchronization Or Frame Pulse I/O

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-9: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Timer1 through Timer9					
T1CK	51	33	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar					
RTCC	27	18	O	—	Real-Time Clock Alarm/Seconds Output (not in VBAT power domain, requires V_{DD})

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-10: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PMA0	44	30	O	TTL/CMOS	Parallel Master Port Address (Demultiplexed Master mode) or Address/ Data (Multiplexed Master modes)
PMA1	43	29	O	TTL/CMOS	
PMA2	14	8	O	TTL/CMOS	
PMA3	12	6	O	TTL/CMOS	
PMA4	11	5	O	TTL/CMOS	
PMA5	10	4	O	TTL/CMOS	
PMA6	29	16	O	TTL/CMOS	
PMA7	28	22	O	TTL/CMOS	
PMA8	50	32	O	TTL/CMOS	
PMA9	49	31	O	TTL/CMOS	
PMA10	42	28	O	TTL/CMOS	
PMA11	41	27	O	TTL/CMOS	
PMA12	35	24	O	TTL/CMOS	
PMA13	34	23	O	TTL/CMOS	
PMA14	71	45	O	TTL/CMOS	
PMA15	70	44	O	TTL/CMOS	
PMA16	77	—	O	TTL/CMOS	
PMA17	78	—	O	TTL/CMOS	
PMA18	91	—	O	TTL/CMOS	
PMA19	92	—	O	TTL/CMOS	
PMA20	95	—	O	TTL/CMOS	
PMA21	96	—	O	TTL/CMOS	
PMA22	97	—	O	TTL/CMOS	
PMA23	1	—	O	TTL/CMOS	
PMCS1	71	45	O	TTL/CMOS	Parallel Master Port Chip Select 1 for PMA(13:0)
PMCS2	70	44	O	TTL/CMOS	Parallel Master Port Chip Select 2 for PMA(14:0)
PMPRD	82	53	O	TTL/CMOS	Parallel Master Port Read Strobe
PMWR	81	52	O	TTL/CMOS	Parallel Master Port Write Strobe
PMCS1A	97	—	O	TTL/CMOS	Parallel Master Port Chip Select 1 for PMA(21:0)
PMCS2A	1	—	O	TTL/CMOS	Parallel Master Port Chip Select 2 for PMA(22:0)

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-10: PMP PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PMD0	93	60	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	94	61	I/O	TTL/ST	
PMD2	98	62	I/O	TTL/ST	
PMD3	99	63	I/O	TTL/ST	
PMD4	100	64	I/O	TTL/ST	
PMD5	3	1	I/O	TTL/ST	
PMD6	4	2	I/O	TTL/ST	
PMD7	5	3	I/O	TTL/ST	
PMD8	90	—	I/O	TTL/ST	
PMD9	89	—	I/O	TTL/ST	
PMD10	88	—	I/O	TTL/ST	
PMD11	87	—	I/O	TTL/ST	
PMD12	79	—	I/O	TTL/ST	
PMD13	80	—	I/O	TTL/ST	
PMD14	83	—	I/O	TTL/ST	
PMD15	84	—	I/O	TTL/ST	
PMALH	43	29	O	TTL/CMOS	Parallel Master Port Address Latch Enable High Byte (Multiplexed Master modes)
PMALL	44	30	O	—	Parallel Master Port Address Latch Enable Low Byte (Multiplexed Master modes)

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select