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PIC32MM0064GPL036 FAMILY

32-Bit Flash Microcontroller with MIPS32® microAptiv™ UC Core with Low Power and Low Pin Count

Operating Conditions

- 2.0V to 3.6V, -40ºC to +85ºC, DC to 25 MHz

Low-Power Modes

- Low-Power modes:
  - Idle: CPU off, peripherals run from system clock
  - Sleep: CPU and peripherals off:
    - Fast wake-up Sleep with retention
    - Low-power Sleep with retention
- 0.5 µA Sleep Current for Regulator Retention mode and 5 µA for Regulator Standby mode
- On-Chip 1.8V Voltage Regulator (VREG)
- On-Chip Ultra Low-Power Retention Regulator

High-Performance 32-Bit RISC CPU

- microAptiv™ UC 32-Bit Core with 5-Stage Pipeline
- microMIPS™ Instruction Set for 35% Smaller Code and 98% Performance compared to MIPS32 Instructions
- DC-25 MHz Operating Frequency
- 3.17 CoreMark®/MHz (79 CoreMark) Performance
- 1.53 DMIPS/MHz (37 DMIPS) (Dhrystone 2.1) Performance
- 16-Bit/32-Bit Wide Instructions with 32-Bit Wide Data Path
- Two Sets of 32 Core Register Files (32-bit) to Reduce Interrupt Latency
- Single-Cycle 32x16 Multiply and Two-Cycle 32x32 Multiply
- Hardware Divide Unit
- 64-Bit, Zero Wait State Flash with ECC to Maximize Endurance/Retention

Microcontroller Features

- Low Pin Count Packages, Ranging from 20 to 36 Pins, including UQFN as Small as 4x4 mm
- Up to 64K Flash Memory:
  - 20,000 erase/write cycle endurance
  - 20 years minimum data retention
  - Self-programmable under software control
- Up to 8K Data Memory
- Pin-Compatible with Most PIC24 MCU/dsPIC® DSC Devices
- Multiple Interrupt Vectors with Individually Programmable Priority
- Fail-Safe Clock Monitor mode
- Configurable Watchdog Timer with On-Chip, Low-Power RC Oscillator
- Programmable Code Protection
- Selectable Oscillator Options including:
  - High-precision, 8 MHz internal Fast RC (FRC) oscillator
  - High-speed crystal/resonator oscillator or external clock
  - 2x/3x/4x/6x/12x/24x PLL, which can be clocked from the FRC or primary oscillator

Peripheral Features

- Atomic Set, Clear and Invert Operation on Select Peripheral Registers
- High-Current Sink/Source 11 mA/16 mA on All Ports
- Independent, Low-Power 32 kHz Timer Oscillator
- Two 4-Wire SPI modules (up to 25 Mbps):
  - 16-byte FIFO
  - I^2S mode
- Two UARTs:
  - RS-232, RS-485 and LIN/J2602 support
  - IrDA® with on-chip hardware encoder and decoder
- External Edge and Level Change Interrupt on All Ports
- CRC module
- Hardware Real-Time Clock and Calendar (RTCC)
- Up to 20 Peripheral Pin Select (PPS) Remappable Pins
- Seven Total 16-Bit Timers:
  - Timer1: Dedicated 16-bit timer/counter
  - Two additional 16-bit timers in each MCCP and SCCP module
- Capture/Compare/PWM/Timer modules:
  - Two 16-bit timers or one 32-bit timer in each module
  - PWM resolution down to 21 ns
  - One Multiple Output (MCCP) module:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Six PWM outputs
    - Programmable dead time
    - Auto-shutdown
  - Two Single Output (SCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Single PWM output
- Reference Clock Output (REFO)
- Two Configurable Logic Cells (CLC) with Internal Connections to Select Peripherals and PPS

Debug Features

- Two Programming and Debugging Interfaces:
  - 2-wire ICSP™ interface with non-intrusive access and real-time data exchange with application
  - 4-wire MIPS® standard Enhanced JTAG interface
- IEEE Standard 1149.2 Compatible (JTAG) Boundary Scan

Analog Features

- Two Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit DAC with Output Pin
- Up to 14-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit, 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit, 300K samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0064GPL036 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (Channels)	Comparators	CRC	RTCC	JTAG	Packages
							UART(1)/LIN/J2602	16-Bit Timers	MCCP(3)	SCCP(4)	CLC	SPI(2)/I2S						
PIC32MM0016GPL020	20	16	4	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0032GPL020	20	32	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0064GPL020	20	64	8	16/16	7	8	2	1	1	2	2	2	11	2	Yes	Yes	Yes	SSOP/QFN
PIC32MM0016GPL028	28	16	4	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/SOIC/ QFN/UQFN
PIC32MM0032GPL028	28	32	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SSOP/ SOIC/ QFN/UQFN
PIC32MM0064GPL028	28	64	8	22/19	7	8	2	1	1	2	2	2	12	2	Yes	Yes	Yes	SPDIP/SSOP/ SOIC/QFN/ UQFN
PIC32MM0016GPL036	36/40	16	4	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0032GPL036	36/40	32	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN
PIC32MM0064GPL036	36/40	64	8	29/20	7	8	2	1	1	2	2	2	14	2	Yes	Yes	Yes	VQFN/UQFN

Note 1: UART1 has assigned pins. UART2 is remappable.

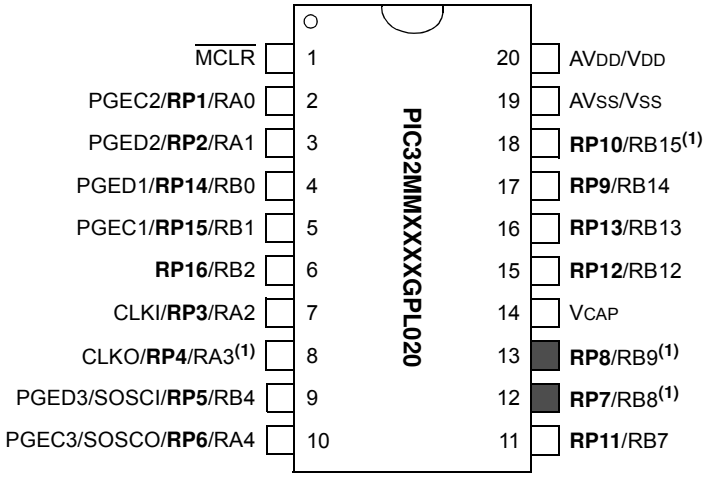
2: SPI1 has assigned pins. SPI2 is remappable.

3: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

Pin Diagrams

20-Pin SSOP



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

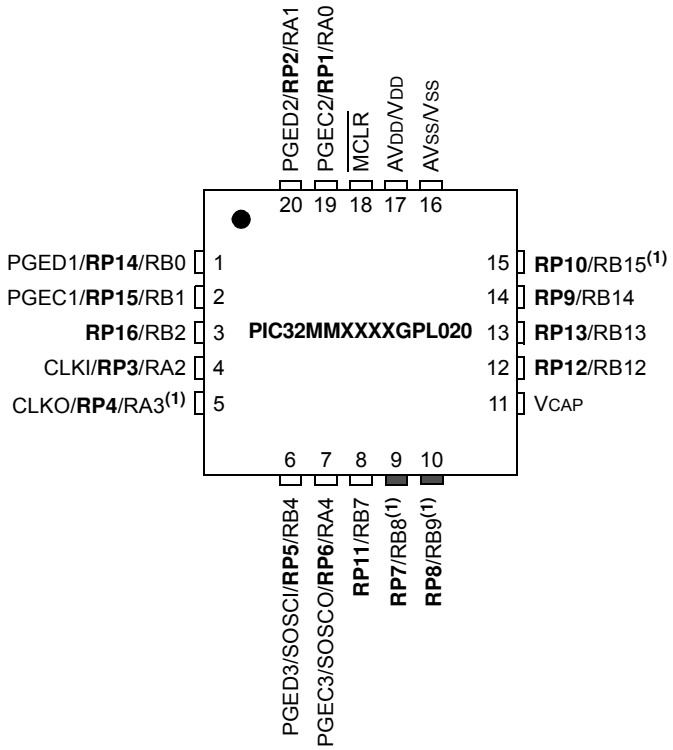
TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN SSOP DEVICES

Pin	Function	Pin	Function
1	MCLR	11	**RP11**/RB7
2	PGEC2/VREF+/AN0/**RP1**/OCM1E/INT3/RA0	12	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)
3	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	13	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
4	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	14	VCAP
5	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	15	TDO/AN7/LVDIN/**RP12**/RB12
6	AN4/**RP16**/RB2	16	TDI/AN8/**RP13**/RB13
7	OSC1/CLKI/AN5/C1INB/**RP3**/OCM1C/RA2	17	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
8	OSC2/CLKO/AN6/C1INA/**RP4**/OCM1D/RA3(1)	18	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
9	PGED3/SOSCI/**RP5**/RB4	19	AVSS/VSS
10	PGEC3/SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	20	AVDD/VDD

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

20-Pin QFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

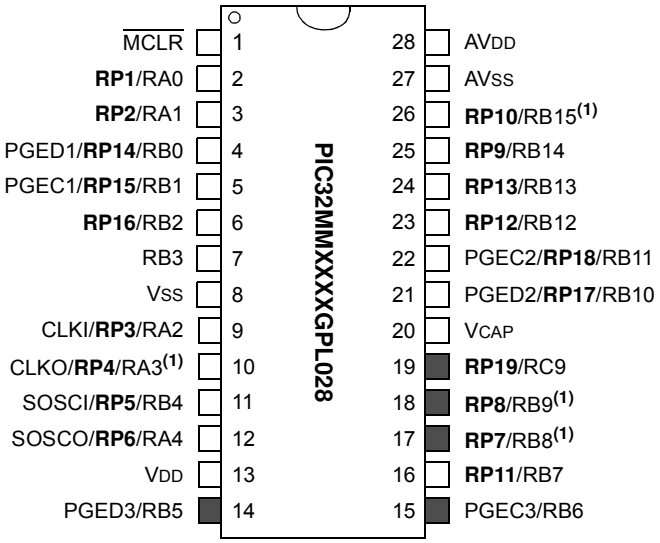
TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN QFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	11	VCAP
2	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	12	TDO/AN7/LVDIN/**RP12**/RB12
3	AN4/**RP16**/RB2	13	TDI/AN8/**RP13**/RB13
4	OSC1/CLKI/AN5/C1INB/**RP3**/OCM1C/RA2	14	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
5	OSC2/CLKO/AN6/C1INA/**RP4**/OCM1D/RA3(1)	15	AN10/REFCLKO/**RP10**/U1RX/$\overline{SS1}$/FSYNC1/INT0/RB15(1)
6	PGED3/SOSCI/**RP5**/RB4	16	AVSS/VSS
7	PGEC3/SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	17	AVDD/VDD
8	**RP11**/RB7	18	$\overline{MCLR}$
9	TCK/**RP7**/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	19	PGEC2/VREF+/AN0/**RP1**/OCM1E/INT3/RA0
10	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)	20	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

28-Pin SPDIP(2)/SSOP/SOIC



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

2: Only PIC32MM0064GPL028 comes in a 28-pin SPDIP package.

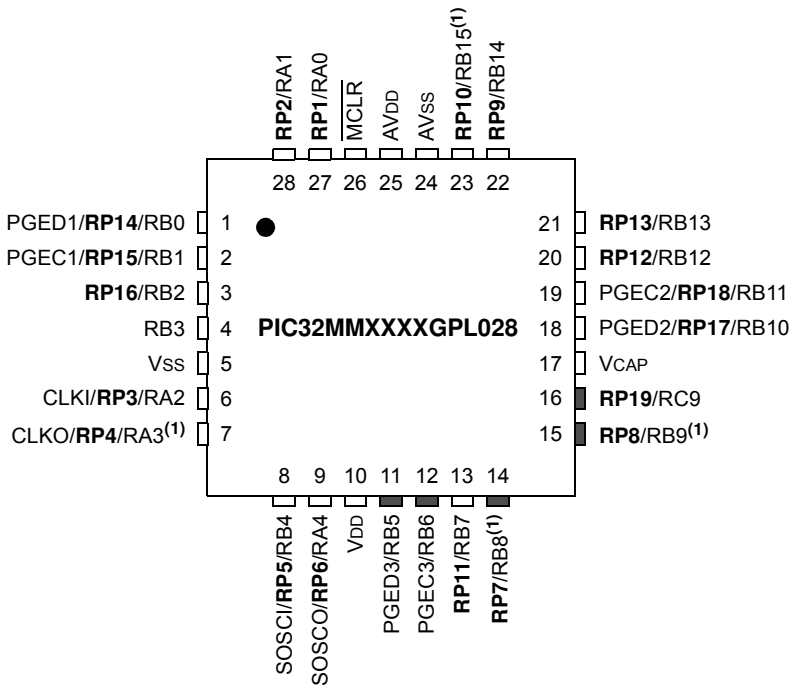
TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN SPDIP/SSOP/SOIC DEVICES

Pin	Function	Pin	Function
1	MCLR	15	PGEC3/RB6
2	VREF+/AN0/**RP1**/OCM1E/INT3/RA0	16	**RP11**/RB7
3	VREF-/AN1/**RP2**/OCM1F/RA1	17	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)
4	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	18	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
5	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	19	**RP19**/RC9
6	AN4/C1INB/**RP16**/RB2	20	VCAP
7	AN11/C1INA/RB3	21	PGED2/TDO/**RP17**/RB10
8	VSS	22	PGEC2/TDI/**RP18**/RB11
9	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	23	AN7/LVDIN/**RP12**/RB12
10	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	24	AN8/**RP13**/RB13
11	SOSCI/**RP5**/RB4	25	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
12	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	26	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
13	VDD	27	AVSS
14	PGED3/RB5	28	AVDD

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

28-Pin QFN/UQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

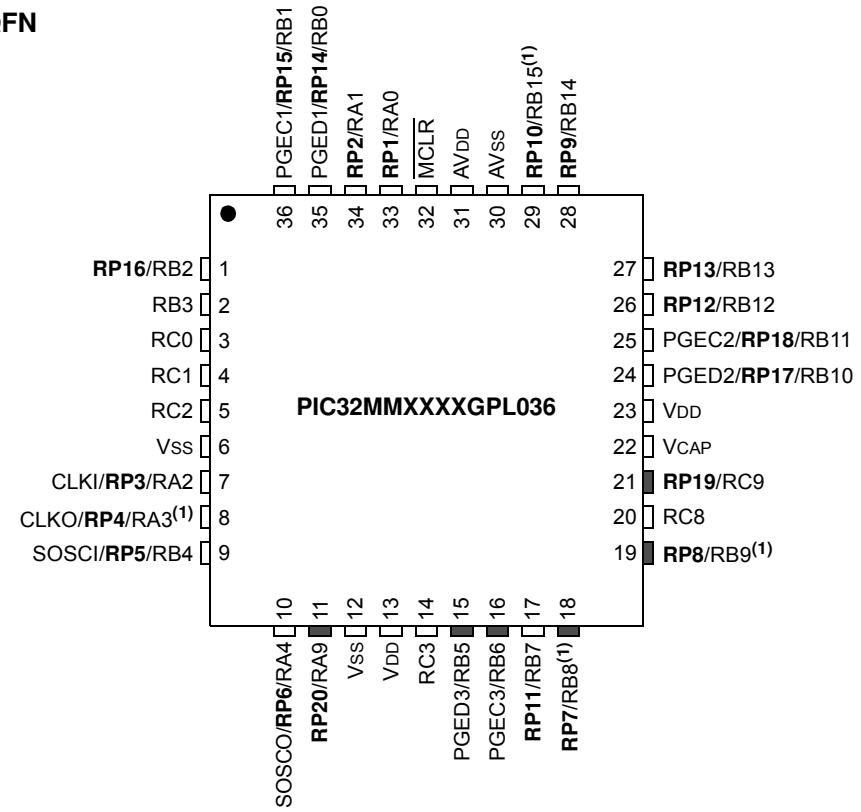
TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	15	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	16	**RP19**/RC9
3	AN4/C1INB/**RP16**/RB2	17	VCAP
4	AN11/C1INA/RB3	18	PGED2/TDO/**RP17**/RB10
5	VSS	19	PGEC2/TDI/**RP18**/RB11
6	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	20	AN7/LVDIN/**RP12**/RB12
7	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	21	AN8/**RP13**/RB13
8	SOSCI/**RP5**/RB4	22	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
9	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	23	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
10	VDD	24	AVSS
11	PGED3/RB5	25	AVDD
12	PGEC3/RB6	26	MCLR
13	**RP11**/RB7	27	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
14	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)	28	VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

36-Pin VQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

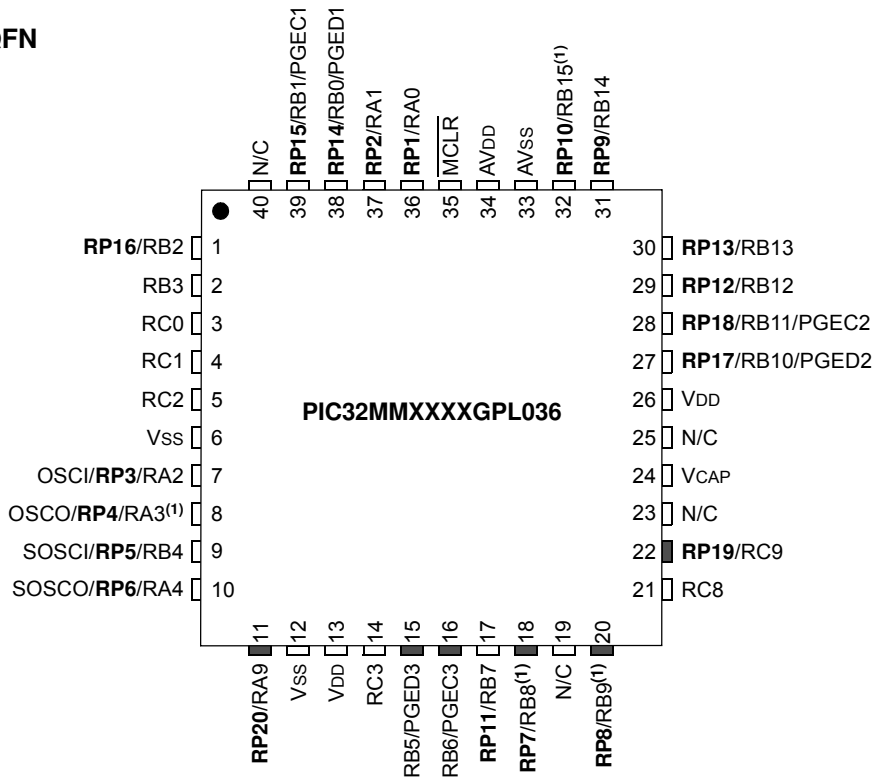
TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN VQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP16**/RB2	19	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	AN11/C1INA/RB3	20	RC8
3	AN12/RC0	21	**RP19**/RC9
4	AN13/RC1	22	VCAP
5	RC2	23	VDD
6	VSS	24	PGED2/TDO/**RP17**/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	PGEC2/TDI/**RP18**/RB11
8	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	26	AN7/LVDIN/**RP12**/RB12
9	SOSCI/**RP5**/RB4	27	AN8/**RP13**/RB13
10	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	28	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
11	**RP20**/RA9	29	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
12	VSS	30	AVSS
13	VDD	31	AVDD
14	RC3	32	MCLR
15	PGED3/RB5	33	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	PGEC3/RB6	34	VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP11**/RB7	35	PGED1/AN2/C1IND/C2INB/**RP14**/RB0
18	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

40-Pin UQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP16**/RB2	21	RC8
2	AN11/C1INA/RB3	22	**RP19**/RC9
3	AN12/RC0	23	N/C
4	AN13/RC1	24	VCAP
5	RC2	25	N/C
6	VSS	26	VDD
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	27	PGED2/TDO/**RP17**/RB10
8	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	28	PGEC2/TDI/**RP18**/RB11
9	SOSCI/**RP5**/RB4	29	AN7/LVDIN/**RP12**/RB12
10	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	30	AN8/**RP13**/RB13
11	**RP20**/RA9	31	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
12	VSS	32	AN10/REFCLKO/**RP10**/U1RX/$\overline{SS1}$/FSYNC1/INT0/RB15(1)
13	VDD	33	AVSS
14	RC3	34	AVDD
15	PGED3/RB5	35	$\overline{MCLR}$
16	PGEC3/RB6	36	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
17	**RP11**/RB7	37	VREF-/AN1/**RP2**/OCM1F/RA1
18	TCK/**RP7**/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	38	PGED1/AN2/C1IND/C2INB/**RP14**/RB0
19	N/C	39	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1
20	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)	40	N/C

Note 1: Pin has an increased current drive strength.

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 5. "Flash Programming"** (DS60001121)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupts"** (DS60001108)
- **Section 10. "Power-Saving Modes"** (DS60001130)
- **Section 14. "Timers"** (DS60001105)
- **Section 19. "Comparator"** (DS60001110)
- **Section 21. "UART"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359)
- **Section 28. "RTCC with Timestamp"** (DS60001362)
- **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381)
- **Section 33. "Programming and Diagnostics"** (DS61129)
- **Section 36. "Configurable Logic Cell"** (DS60001363)
- **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 59. "Oscillators with DCO"** (DS60001329)
- **Section 60. "32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS60001336)
- **Section 62. "Dual Watchdog Timer"** (DS60001365)

NOTES:

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0064GPL036 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0064GPL036 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0064GPL036 FAMILY BLOCK DIAGRAM

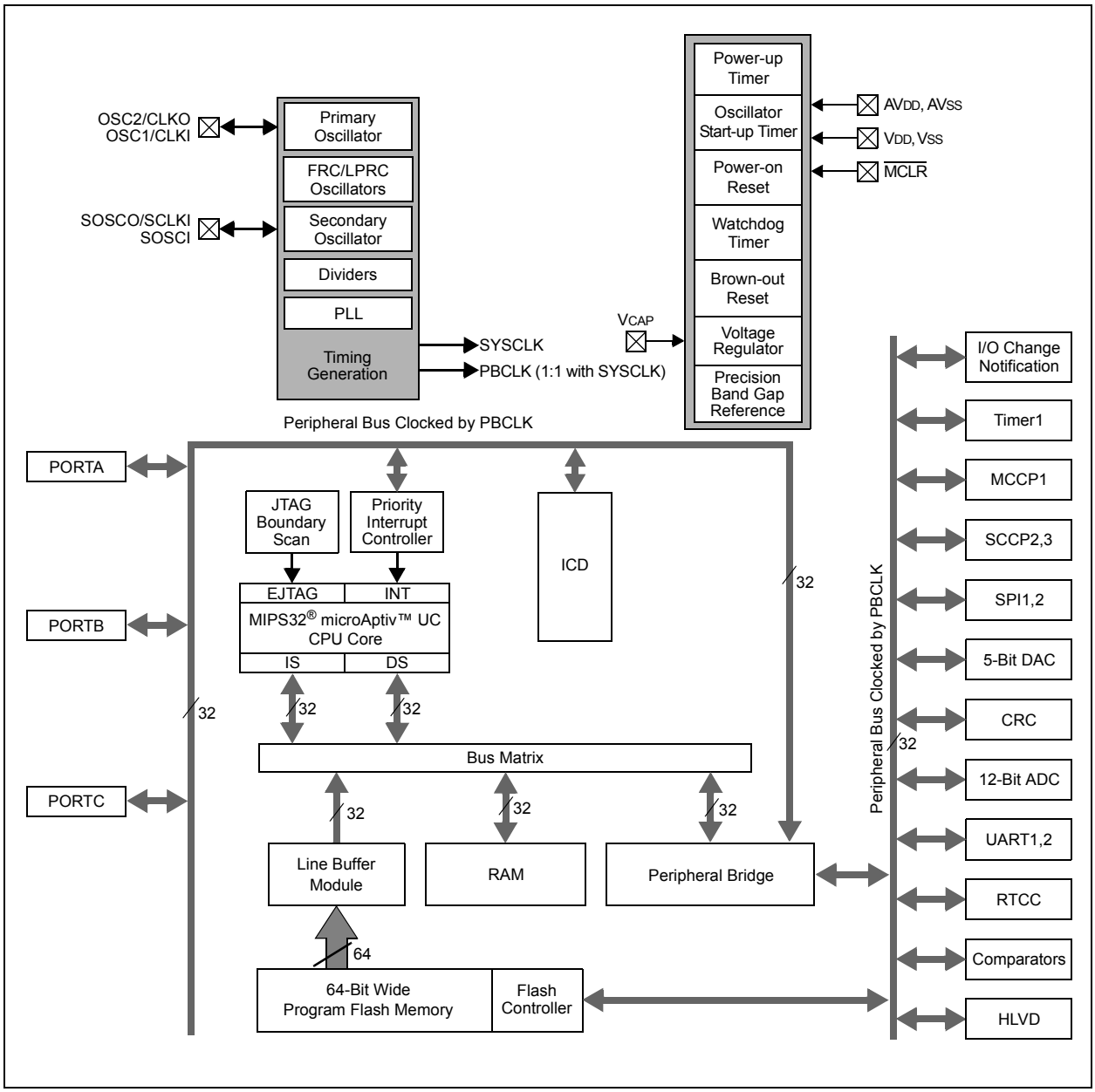


TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
AN0	19	2	27	2	33	36	I	ANA	Analog-to-Digital Converter input channels
AN1	20	3	28	3	34	37	I	ANA	
AN2	1	4	1	4	35	38	I	ANA	
AN3	2	5	2	5	36	39	I	ANA	
AN4	3	6	3	6	1	1	I	ANA	
AN5	4	7	6	9	7	7	I	ANA	
AN6	5	8	7	10	8	8	I	ANA	
AN7	12	15	20	23	26	29	I	ANA	
AN8	13	16	21	24	27	30	I	ANA	
AN9	14	17	22	25	28	31	I	ANA	
AN10	15	18	23	26	29	32	I	ANA	
AN11	—	—	4	7	2	2	I	ANA	
AN12	—	—	—	—	3	3	I	ANA	
AN13	—	—	—	—	4	4	I	ANA	
AVDD	17	20	25	28	31	34	P	—	Analog modules power supply
AVSS	16	19	24	27	30	33	P	—	Analog modules ground
C1INA	5	8	4	7	2	2	I	ANA	Comparator 1 Input A
C1INB	4	7	3	6	1	1	I	ANA	Comparator 1 Input B
C1INC	2	5	2	5	36	39	I	ANA	Comparator 1 Input C
C1IND	1	4	1	4	35	38	I	ANA	Comparator 1 Input D
C1OUT	14	17	22	25	28	31	O	DIG	Comparator 1 output
C2INA	2	5	2	5	36	39	I	ANA	Comparator 2 Input A
C2INB	1	4	1	4	35	38	I	ANA	Comparator 2 Input B
C2OUT	10	13	15	18	19	20	O	DIG	Comparator 2 output
CLKI	4	7	6	9	7	7	I	ST	External Clock input (EC mode)
CLKO	5	8	7	10	8	8	O	DIG	System clock output
CDAC1	14	17	22	25	28	31	O	ANA	Digital-to-Analog Converter output
FSYNC1	15	18	23	26	29	32	I/O	ST/DIG	SPI1 frame signal input or output
INT0	15	18	23	26	29	32	I	ST	External Interrupt 0
INT1	14	17	22	25	28	31	I	ST	External Interrupt 1
INT2	10	13	15	18	19	20	I	ST	External Interrupt 2
INT3	19	2	27	2	33	36	I	ST	External Interrupt 3
LVDIN	12	15	20	23	26	29	I	ANA	High/Low-Voltage Detect input
$\overline{MCLR}$	18	1	26	1	32	35	I	ST	Master Clear (device Reset)
OCM1A	9	12	14	17	18	18	O	DIG	MCCP1 Output A
OCM1B	10	13	15	18	19	20	O	DIG	MCCP1 Output B
OCM1C	4	7	6	9	7	7	O	DIG	MCCP1 Output C
OCM1D	5	8	7	10	8	8	O	DIG	MCCP1 Output D
OCM1E	19	2	27	2	33	36	O	DIG	MCCP1 Output E
OCM1F	20	3	28	3	34	37	O	DIG	MCCP1 Output F
OSC1	4	7	6	9	7	7	—	—	Primary Oscillator crystal
OSC2	5	8	7	10	8	8	—	—	Primary Oscillator crystal

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
PGEC1	2	5	2	5	36	39	I	ST	ICSP Port 1 programming clock input
PGEC2	19	2	19	22	25	28	I	ST	ICSP Port 2 programming clock input
PGEC3	7	10	12	15	16	16	I	ST	ICSP Port 3 programming clock input
PGED1	1	4	1	4	35	38	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	20	3	18	21	24	27	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	6	9	11	14	15	15	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	7	10	9	12	10	10	I	ST	Real-Time Clock 50/60 Hz clock input
RA0	19	2	27	2	33	36	I/O	ST/DIG	PORTA digital I/O
RA1	20	3	28	3	34	37	I/O	ST/DIG	PORTA digital I/O
RA2	4	7	6	9	7	7	I/O	ST/DIG	PORTA digital I/O
RA3	5	8	7	10	8	8	I/O	ST/DIG	PORTA digital I/O
RA4	7	10	9	12	10	10	I/O	ST/DIG	PORTA digital I/O
RA9	—	—	—	—	11	11	I/O	ST/DIG	PORTA digital I/O
RB0	1	4	1	4	35	38	I/O	ST/DIG	PORTB digital I/O
RB1	2	5	2	5	36	39	I/O	ST/DIG	PORTB digital I/O
RB2	3	6	3	6	1	1	I/O	ST/DIG	PORTB digital I/O
RB3	—	—	4	7	2	2	I/O	ST/DIG	PORTB digital I/O
RB4	6	9	8	11	9	9	I/O	ST/DIG	PORTB digital I/O
RB5	—	—	11	14	15	15	I/O	ST/DIG	PORTB digital I/O
RB6	—	—	12	15	16	16	I/O	ST/DIG	PORTB digital I/O
RB7	8	11	13	16	17	17	I/O	ST/DIG	PORTB digital I/O
RB8	9	12	14	17	18	18	I/O	ST/DIG	PORTB digital I/O
RB9	10	13	15	18	19	20	I/O	ST/DIG	PORTB digital I/O
RB10	—	—	18	21	24	27	I/O	ST/DIG	PORTB digital I/O
RB11	—	—	19	22	25	28	I/O	ST/DIG	PORTB digital I/O
RB12	12	15	20	23	26	29	I/O	ST/DIG	PORTB digital I/O
RB13	13	16	21	24	27	30	I/O	ST/DIG	PORTB digital I/O
RB14	14	17	22	25	28	31	I/O	ST/DIG	PORTB digital I/O
RB15	15	18	23	26	29	32	I/O	ST/DIG	PORTB digital I/O
RC0	—	—	—	—	3	3	I/O	ST/DIG	PORTC digital I/O
RC1	—	—	—	—	4	4	I/O	ST/DIG	PORTC digital I/O
RC2	—	—	—	—	5	5	I/O	ST/DIG	PORTC digital I/O
RC3	—	—	—	—	14	14	I/O	ST/DIG	PORTC digital I/O
RC8	—	—	—	—	20	21	I/O	ST/DIG	PORTC digital I/O
RC9	—	—	16	19	21	22	I/O	ST/DIG	PORTC digital I/O
REFCLKI	10	13	15	18	19	20	I	ST	Reference clock input
REFCLKO	15	18	23	26	29	32	O	DIG	Reference clock output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
RP1	19	2	27	2	33	36	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	20	3	28	3	34	37	I/O	ST/DIG	
RP3	4	7	6	9	7	7	I/O	ST/DIG	
RP4	5	8	7	10	8	8	I/O	ST/DIG	
RP5	6	9	8	11	9	9	I/O	ST/DIG	
RP6	7	10	9	12	10	10	I/O	ST/DIG	
RP7	9	12	14	17	18	18	I/O	ST/DIG	
RP8	10	13	15	18	19	20	I/O	ST/DIG	
RP9	14	17	22	25	28	31	I/O	ST/DIG	
RP10	15	18	23	26	29	32	I/O	ST/DIG	
RP11	8	11	13	16	17	17	I/O	ST/DIG	
RP12	12	15	20	23	26	29	I/O	ST/DIG	
RP13	13	16	21	24	27	30	I/O	ST/DIG	
RP14	1	4	1	4	35	38	I/O	ST/DIG	
RP15	2	5	2	5	36	39	I/O	ST/DIG	
RP16	3	6	3	6	1	1	I/O	ST/DIG	
RP17	—	—	18	21	24	27	I/O	ST/DIG	
RP18	—	—	19	22	25	28	I/O	ST/DIG	
RP19	—	—	16	19	21	22	I/O	ST/DIG	
RP20	—	—	—	—	11	11	I/O	ST/DIG	
RTCC	14	17	22	25	28	31	O	DIG	Real-Time Clock alarm/seconds output
SCK1	9	12	14	17	18	18	I/O	ST/DIG	SPI1 clock (input or output)
SCLKI	7	10	9	12	10	10	I	ST	Secondary Oscillator external clock input
SDI1	14	17	22	25	28	31	I	ST	SPI1 data input
SDO1	10	13	15	18	19	20	O	DIG	SPI1 data output
SOSCI	6	9	8	11	9	9	—	—	Secondary Oscillator crystal
SOSCO	7	10	9	12	10	10	—	—	Secondary Oscillator crystal
$\overline{SS1}$	15	18	23	26	29	32	I	ST	SPI1 slave select input
T1CK	10	13	15	18	19	20	I	ST	Timer1 external clock input
T1G	10	13	15	18	19	20	I	ST	Timer1 clock gate input
TCK	9	12	14	17	18	18	I	ST	JTAG clock input
TDI	13	16	19	22	25	28	I	ST	JTAG data input
TDO	12	15	18	21	24	27	O	DIG	JTAG data output
TMS	10	13	15	18	19	20	I	ST	JTAG mode select input
U1BCLK	10	13	15	18	19	20	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{U1CTS}$	9	12	14	17	18	18	I	ST	UART1 transmission control input
$\overline{U1RTS}$	10	13	15	18	19	20	O	DIG	UART1 reception control output
U1RX	15	18	23	26	29	32	I	ST	UART1 receive data input
U1TX	14	17	22	25	28	31	O	DIG	UART1 transmit data output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
VCAP	11	14	17	20	22	24	P	—	Core voltage regulator filter capacitor connection
VDD	17	20	10,25	13,28	13,23,31	13,26, 34	P	—	Digital modules power supply
VREF-	20	3	28	3	34	37	I	ANA	ADC negative reference
VREF+	19	2	27	2	33	36	I	ANA	ADC and DAC positive reference
VSS	16	19	5,24	8,27	6,12,30	6,12, 33	P	—	Digital modules ground

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0064GPL036 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pin (see **Section 2.4 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **Section 2.7 "External Oscillator Pins"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

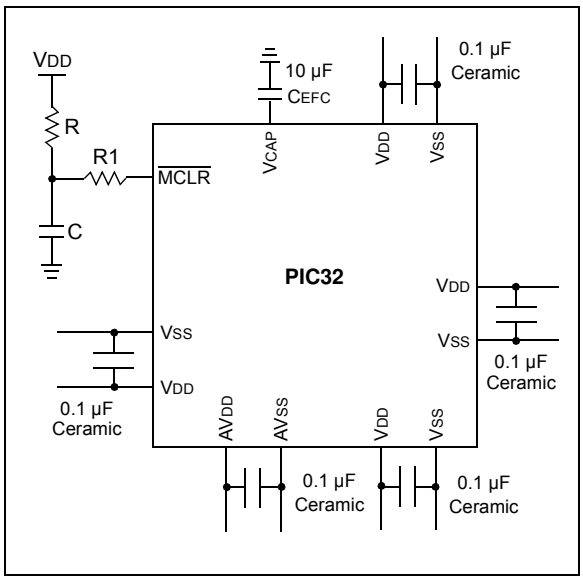
2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides for two specific device functions:

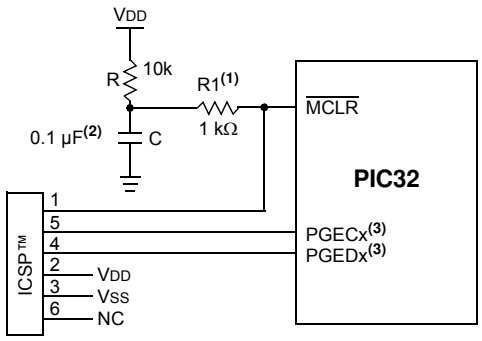
- Device Reset
- Device Programming and Debugging

Pulling The $\overline{MCLR}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{MCLR}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{MCLR}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS(1,2,3)



Note 1: 470Ω ≤ R1 ≤ 1 kΩ will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met without interfering with the debug/programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.4 Capacitor on Internal Voltage Regulator (V_{CAP})

A low-ESR (<1 Ohm) capacitor is required on the V_{CAP} pin, which is used to stabilize the internal voltage regulator output. The V_{CAP} pin must not be connected to V_{DD} and must have a C_{EFC} capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. The recommended value of the C_{EFC} capacitor is 10 µF. On the printed circuit board, it should be placed as close to the V_{CAP} pin as possible. If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to this capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Input Voltage High (VIH) and Input Voltage Low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™ In-Circuit Emulator.

For more information on MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available from the Microchip web site.

- *"Using MPLAB® ICD 3* In-Circuit Debugger" (poster) (DS51765)
- *"Development Tools Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide" (*DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector, and the JTAG pins on the device, as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

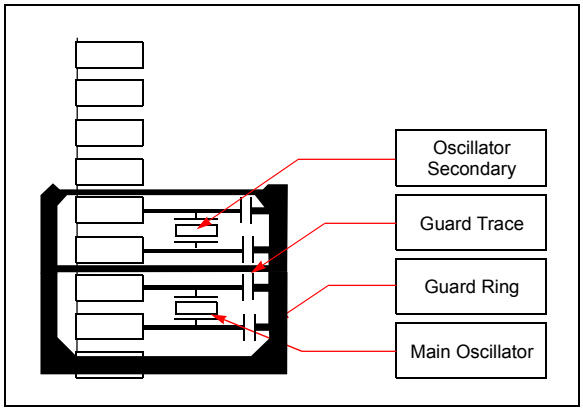
Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Input Voltage High (VIH) and Input Voltage Low (VIL) requirements.

2.7 External Oscillator Pins

The PIC32MM0064GPL036 family has options for two external oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

To minimize power consumption, unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic low or logic high state.

Alternatively, inputs can be reserved by ensuring the pin is always configured as an input and externally connecting the pin to VSS or VDD. A current-limiting resistor may be used to create this connection if there is any risk of inadvertently configuring the pin as an output with the logic output state opposite of the chosen power rail.

NOTES:

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32® microAptiv™ UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32® microAptiv™ UC microprocessor core is the heart of the PIC32MM0064GPL036 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

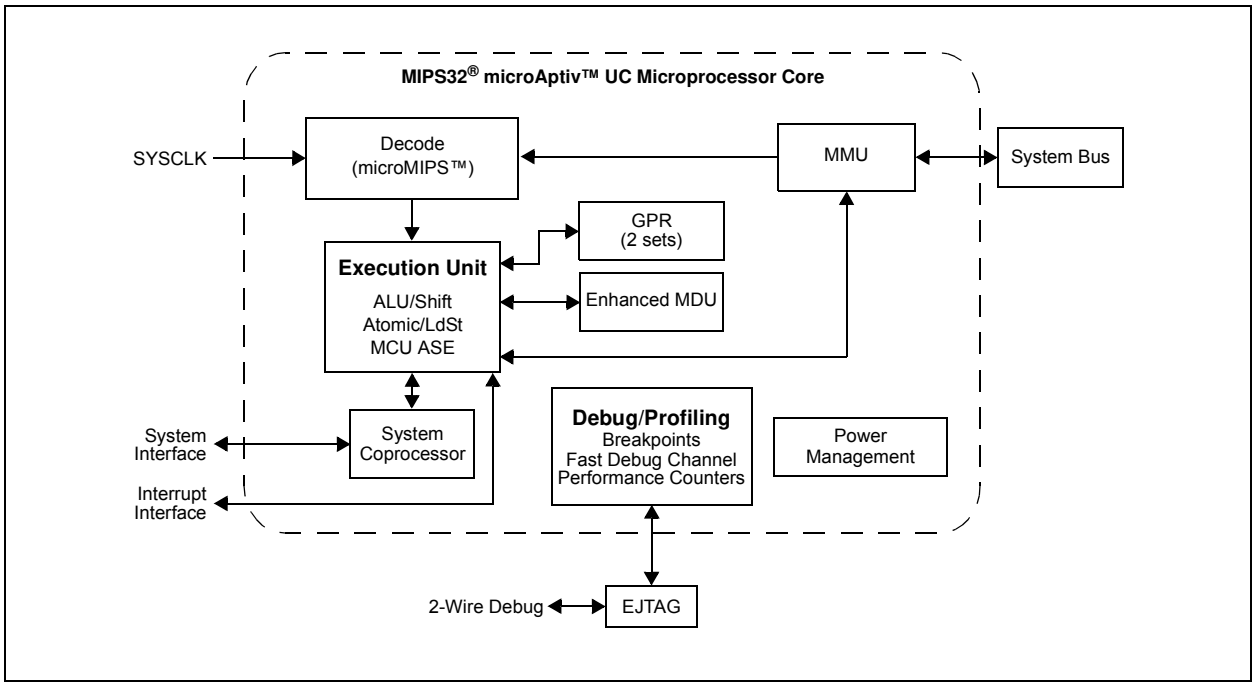
3.1 Features

The PIC32MM0064GPL036 family processor core key features include:

- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
  - Multiply-add and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero and one detect instructions
  - `WAIT` instruction
  - Conditional move instructions
  - Vectored interrupts
  - Atomic interrupt enable/disable
  - One GPR shadow set to minimize latency of interrupts
  - Bit field manipulation instructions
- microMIPS™ Instruction Set:
  - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
  - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
  - Added seventeen new and thirty-five MIPS32® corresponding commonly used instructions in 16-bit opcode format.
  - Stack Pointer implicit in instruction.
  - MIPS32 assembly and ABI compatible.
- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
  - Configurable using high-performance multiplier array.
  - Maximum issue rate of one 32x16 multiply per clock.
  - Maximum issue rate of one 32x32 multiply every other clock.
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
  - No minimum frequency: 0 MHz.
  - Power-Down mode (triggered by `WAIT` instruction).
- EJTAG Debug/Profiling:
  - CPU control with start, stop and single stepping.
  - Software breakpoints via the `SDBBP` instruction.
  - Optional simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
  - PC and/or load/store address sampling for profiling.
  - Performance counters.
  - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0064GPL036 family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



3.2 Architecture Overview

The MIPS32® microAptiv™ UC microprocessor core in the PIC32MM0064GPL036 family devices contains several logic blocks, working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Power Management
- microMIPS Instructions Decoder
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous Multiply/Divide Unit (MDU). The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid Stalls when executing instruction streams where data producing instructions are followed closely by consumers for their results
- Leading zero/one detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The microAptiv UC core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows the long-running MDU operations to be partially masked by system Stalls and/or other Integer Unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, Result/Accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown (‘32’ of 32x16) represents the rs operand. The second number (‘16’ of 32x16) represents the rt operand. The microAptiv UC core only checks the value of the rt operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back, 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU. Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (rs) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit wide rs, 15 iterations are skipped, and for a 24-bit wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline Stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be re-issued), and latency (number of cycles until a result is available) for the microAptiv UC core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU`, `MADD/MADDU`, `MSUB/MSUBU`	16 bits	1	1
	32 bits	2	2
`MUL` (GPR destination)	16 bits	2	1
	32 bits	3	2
`DIV/DIVU`	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32