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PIC32MM0256GPM064 FAMILY

32-Bit Flash Microcontroller with MIPS32® microAptiv™ UC Core, Low Power and USB

Operating Conditions

- 2.0V to 3.6V, -40ºC to +85ºC, DC to 25 MHz

Low-Power Modes

- Low-Power modes:
  - Idle – CPU off, peripherals run from system clock
  - Sleep – CPU and peripherals off:
    - Fast wake-up Sleep with retention
    - Low-power Sleep with retention
- 0.65 µA Sleep current for RAM Retention Regulator mode and 5 µA for Regulator Standby mode
- On-Chip 1.8V Voltage Regulator (VREG)
- On-Chip Ultra Low-Power Retention Regulator

High-Performance 32-Bit RISC CPU

- microAptiv™ UC 32-Bit Core with 5-Stage Pipeline
- microMIPS™ Instruction Set for 35% Smaller Code and 98% Performance compared to MIPS32 Instructions
- 1.53 DMIPS/MHz (37 DMIPS) (Dhrystone 2.1) Performance
- 3.17 CoreMark®/MHz (79 CoreMark) Performance
- 16-Bit/32-Bit Wide Instructions with 32-Bit Wide Data Path
- Two Sets of 32 Core Register Files (32-bit) to Reduce Interrupt Latency
- Single-Cycle 32x16 Multiply and Two-Cycle 32x32 Multiply
- 64-Bit, Zero Wait State Flash with ECC to Maximize Endurance/Retention

Microcontroller Features

- Up to 256K Flash Memory
  - 20,000 Erase/Write Cycle Endurance
  - 20 Years Minimum Data Retention
  - Self-Programmable under Software Control
- Up to 32K SRAM Memory
- Multiple Interrupt Vectors with Individually Programmable Priority
- Fail-Safe Clock Monitor mode
- Configurable Watchdog Timer with On-Chip, Low-Power RC Oscillator
- Programmable Code Protection
- Selectable Oscillator Options Including:
  - High-precision, 8 MHz (FRC) internal RC oscillator – 2x/3x/4x/6x/12x/24x PLL, which can be clocked from FRC or the Primary Oscillator
  - Primary high-speed, crystal/resonator oscillator or external clock

Peripheral Features

- USB 2.0 Compliant Full-Speed and Low-Speed Device, Host and On-The-Go (OTG) Controller:
  - Dedicated DMA
  - Device mode operation from FRC oscillator; no crystal oscillator required
- Atomic Set, Clear and Invert Operation on Select Peripheral Registers
- High-Current Sink/Source
- Independent, Low-Power 32 kHz Timer Oscillator
- Three 4-Wire SPI modules:
  - 16-byte FIFO
  - Variable width
  - I^2S mode
- Three I^2C Master and Slave w/Address Masking and IPMI Support
- Three Enhanced Addressable UARTs:
  - RS-232, RS-485 and LIN/J2602 support
  - IrDA® with on-chip hardware encoder and decoder
- External Edge and Level Change Interrupt on All Ports
- Hardware Real-Time Clock and Calendar (RTCC)
- Up to 24 Peripheral Pin Select (PPS) Remappable Pins
- 21 Total 16-Bit Timers:
  - Three dedicated 16-bit timers/counters
  - Two can be concatenated to form a 32-bit timer
  - Two additional 16-bit timers in each MCCP and SCCP module, totaling 18
- Capture/Compare/PWM/Timer modules:
  - Two 16-bit timers or one 32-bit timer in each module
  - PWM resolution down to 21 ns
  - Three Multiple Output (MCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Six PWM outputs
    - Programmable dead time
    - Auto-shutdown
  - Six Single Output (SCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Single PWM output
- Reference Clock Output (REFO)
- Four Configurable Logic Cells (CLC) with Internal Connections to Select Peripherals and PPS
- 4-Channel Hardware DMA with Automatic Data Size Detection and CRC Engine

Debug Features

- Two Programming and Debugging Interfaces:
  - 2-wire ICSP™ interface with non-intrusive access and real-time data exchange with application
  - 4-wire MIPS® standard Enhanced JTAG interface
- IEEE Standard 1149.2 Compatible (JTAG) Boundary Scan

Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

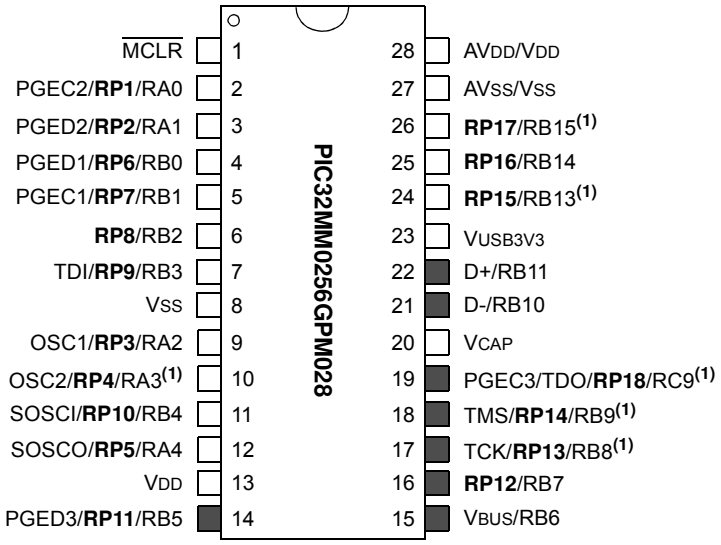
TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (External Channels)	Comparators	CRC	RTCC	I^2C	USB	Packages
							Dedicated 16-Bit Timers	UART(1)/LIN/J2602	MCCP(4)	SCCP(3)	CLC	SPI(2)/I^2S							
PIC32MM0064GPM028	28	64	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0128GPM028	28	128	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0256GPM028	28	256	32	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0064GPM036	36/40	64	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0128GPM036	36/40	128	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0256GPM036	36/40	256	32	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0064GPM048	48	64	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0128GPM048	48	128	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0256GPM048	48	256	32	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0064GPM064	64	64	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0128GPM064	64	128	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0256GPM064	64	256	32	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP

Note 1: UART1 has assigned pins. UART2 and UART3 are remappable.
2: SPI1 and SPI3 have assigned pins. SPI2 is remappable.
3: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.
4: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

Pin Diagrams

28-Pin SSOP



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

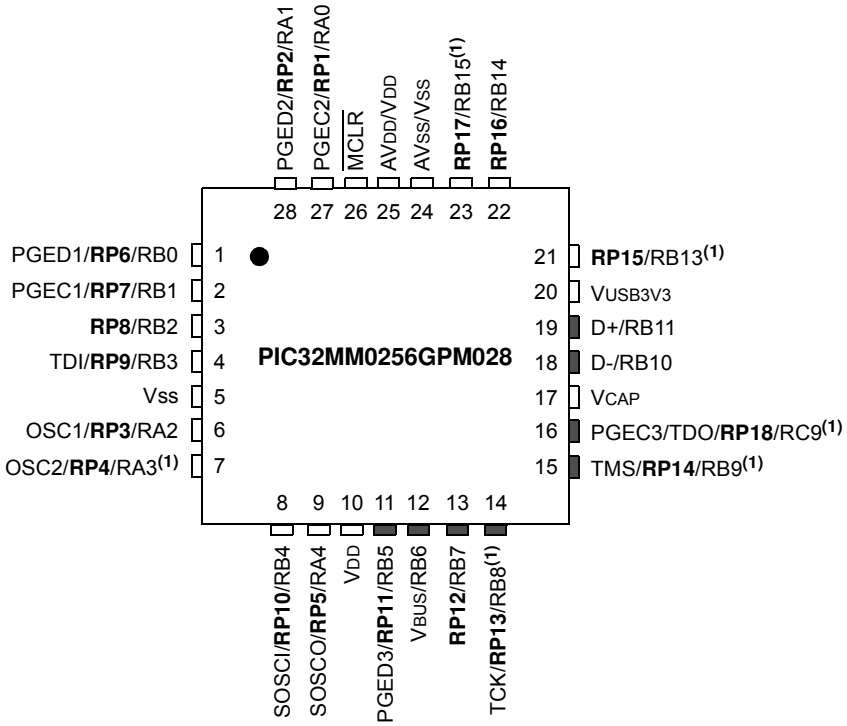
TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN SSOP DEVICES

Pin	Function	Pin	Function
1	MCLR	15	VBUS/RB6
2	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0	16	**RP12**/SDA3/SDI3/OCM3F/RB7
3	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	17	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)
4	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	18	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
5	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	19	PGEC3/TDO/**RP18**/ASCL1(2)/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9(1)
6	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	20	VCAP
7	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	21	D-/RB10
8	VSS	22	D+/RB11
9	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	23	VUSB3V3
10	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	24	AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13(1)
11	SOSCI/AN7/**RP10**/OCM3C/RB4	25	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
12	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	26	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
13	VDD	27	AVSS/VSS
14	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	28	AVDD/VDD

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

28-Pin QFN/UQFN



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

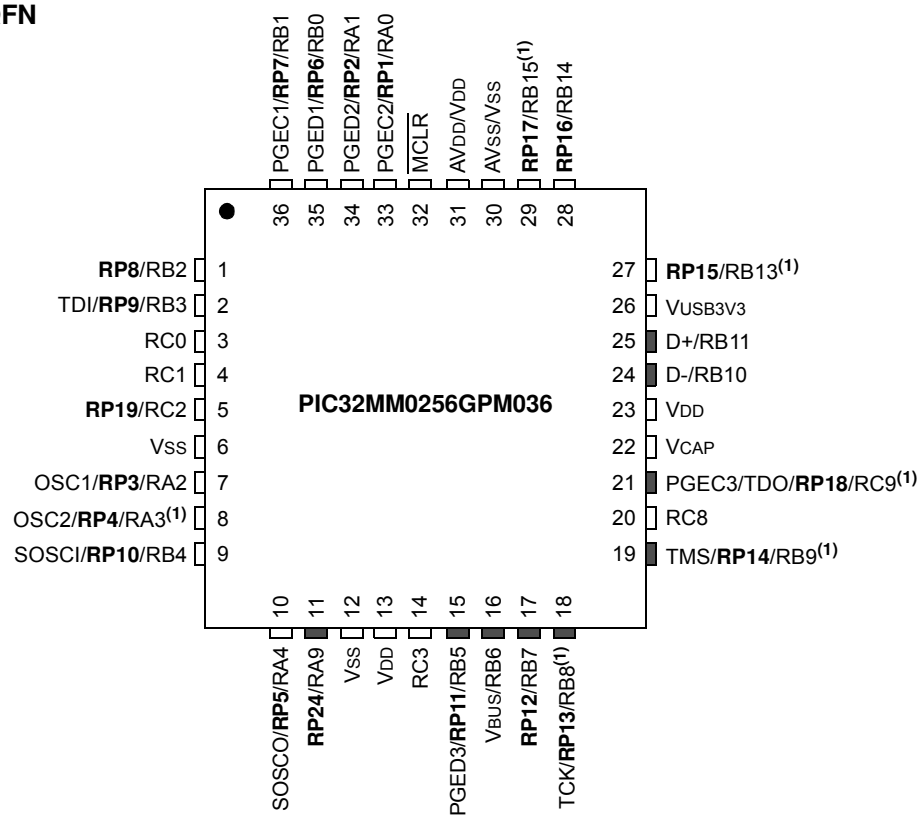
TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	15	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
2	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	16	PGEC3/TDO/**RP18**/ASCL1(2)/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9(1)
3	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	17	VCAP
4	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	18	D-/RB10
5	VSS	19	D+/RB11
6	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	20	VUSB3V3
7	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	21	AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13(1)
8	SOSCI/AN7/**RP10**/OCM3C/RB4	22	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
9	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	23	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
10	VDD	24	AVSS/VSS
11	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	25	AVDD/VDD
12	VBUS/RB6	26	MCLR
13	**RP12**/SDA3/SDI3/OCM3F/RB7	27	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
14	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)	28	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

36-Pin QFN



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

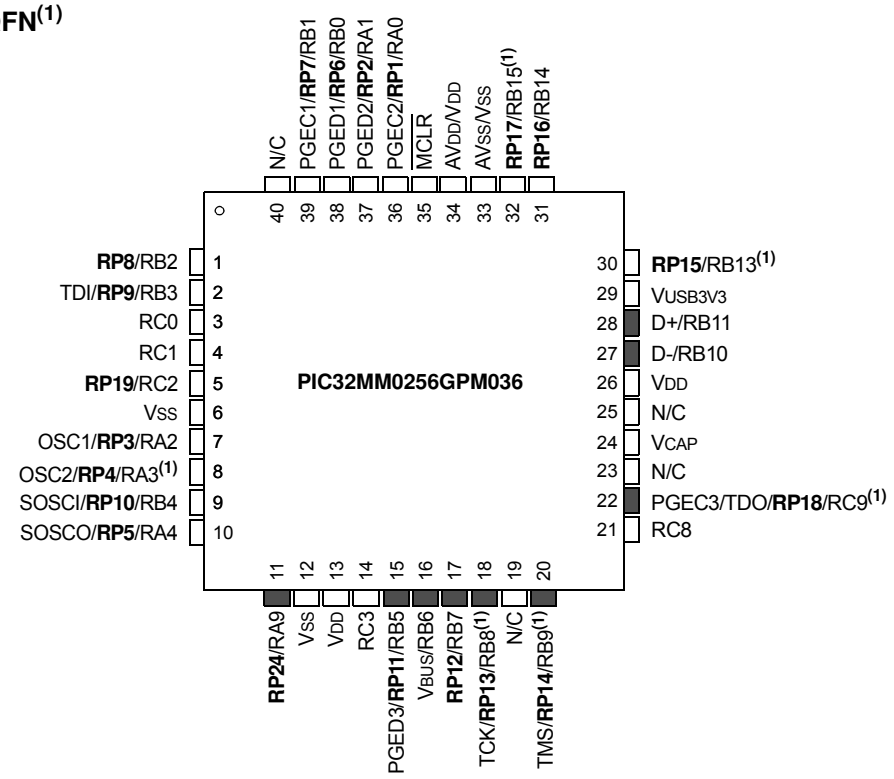
TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN QFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	19	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	20	AN14/LVDIN/C2INC/RC8
3	AN12/C2IND/T2CK/T2G/RC0	21	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/SDO3/RC9(1)
4	AN13/T3CK/T3G/RC1	22	VCAP
5	**RP19**/OCM2A/RC2	23	VDD
6	VSS	24	D-/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	D+/RB11
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	26	VUSB3V3
9	SOSCI/AN7/**RP10**/OCM3C/RB4	27	AN8/**RP15**/SCL3/SCK3/RB13(1)
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	28	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
11	**RP24**/OCM3A/RA9	29	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
12	VSS	30	AVSS/VSS
13	VDD	31	AVDD/VDD
14	RC3	32	MCLR
15	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	33	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	VBUS/RB6	34	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP12**/SDA3/SDI3/OCM3F/RB7	35	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
18	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

40-Pin UQFN(1)



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

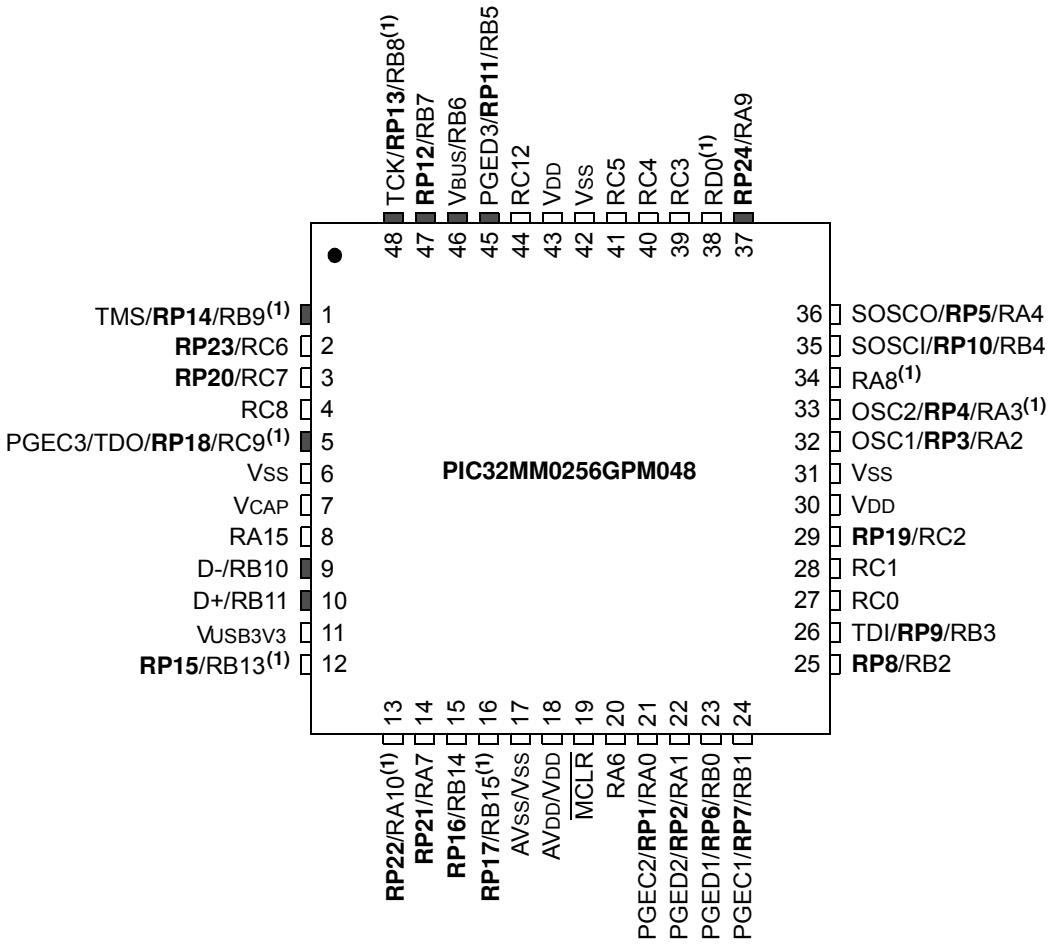
TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	21	AN14/LVDIN/C2INC/RC8
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	22	PGEC3/TDO/**RP18**/ASCL1(2)/SDO3/USBOEN/RC9(1)
3	AN12/C2IND/T2CK/T2G/RC0	23	N/C
4	AN13/T3CK/T3G/RC1	24	VCAP
5	**RP19**/OCM2A/RC2	25	N/C
6	VSS	26	VDD
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	27	D-/RB10
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	28	D+/RB11
9	SOSCI/AN7/**RP10**/OCM3C/RB4	29	VUSB3V3
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	30	AN8/**RP15**/SCL3/SCK3/RB13(1)
11	**RP24**/OCM3A/RA9	31	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
12	VSS	32	AN10/C3INA/REFCLKO/**RP17**/U1RX/$\overline{SS1}$/FSYNC1/OCM2B/INT0/RB15(1)
13	VDD	33	AVSS/VSS
14	RC3	34	AVDD/VDD
15	PGED3/**RP11**/ASDA1(2)/USBID/$\overline{SS3}$/FSYNC3/OCM3E/RB5	35	$\overline{MCLR}$
16	VBUS/RB6	36	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
17	**RP12**/SDA3/SDI3/OCM3F/RB7	37	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
18	TCK/**RP13**/SCL1/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	38	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
19	N/C	39	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1
20	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/OCM1B/INT2/RB9(1)	40	N/C

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

48-Pin UQFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

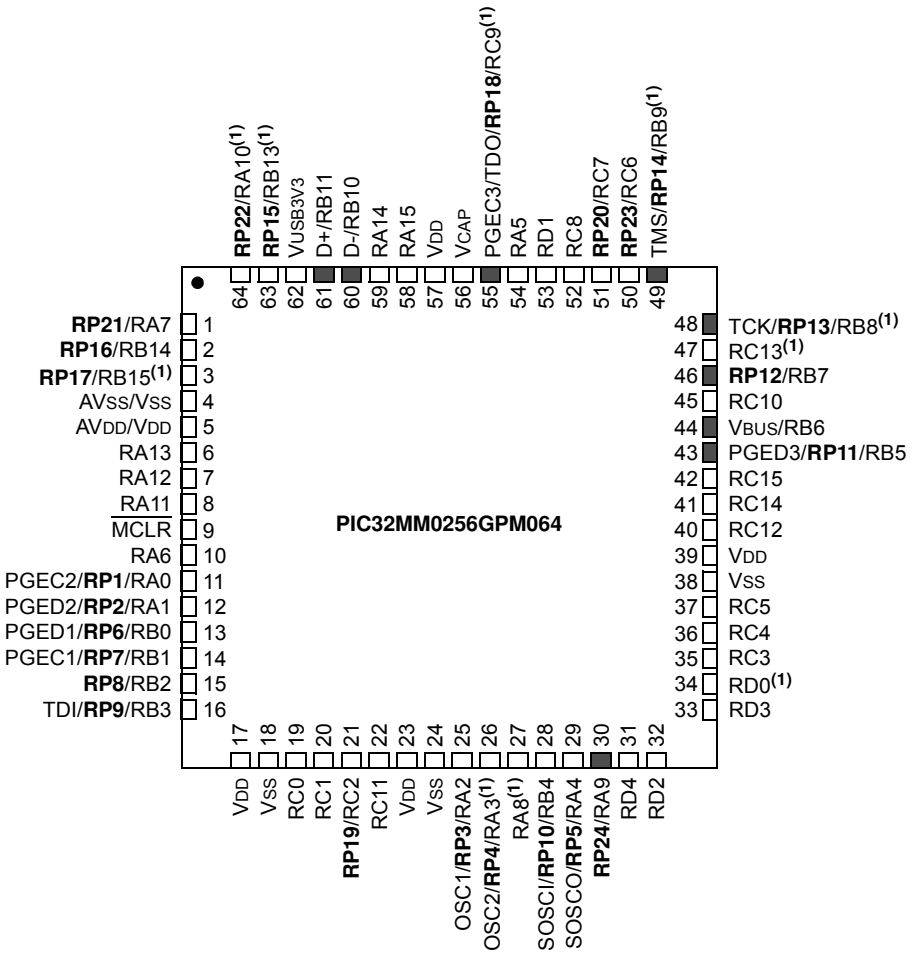
TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 48-PIN UQFN/TQFP DEVICES

Pin	Function	Pin	Function
1	TMS/**RP14**/SDA1/OCM1B/INT2/RB9(1)	25	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2
2	**RP23**/RC6	26	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3
3	**RP20**/RC7	27	AN12/C2IND/T2CK/T2G/RC0
4	AN14/LVDIN/C2INC/RC8	28	AN13/T3CK/T3G/RC1
5	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1)	29	**RP19**/OCM2A/RC2
6	VSS	30	VDD
7	VCAP	31	VSS
8	RTCC/RA15	32	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2
9	D-/RB10	33	OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1)
10	D+/RB11	34	SDO3/RA8(1)
11	VUSB3V3	35	SOSCI/AN7/**RP10**/OCM3C/RB4
12	AN8/**RP15**/SCL3/RB13(1)	36	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4
13	**RP22**/SCK3/RA10(1)	37	**RP24**/OCM3A/RA9
14	**RP21**/SDI3/RA7	38	REFCLKI/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/RD0(1)
15	CVREF/AN9/C3INB/**RP16**/VBUSON/SDI1/OCM3B/INT1/RB14	39	OCM2B/RC3
16	AN10/C3INA/REFCLKO/**RP17**/$\overline{\text{SS1}}$/FSYNC1/INT0/RB15(1)	40	OCM1E/INT3/RC4
17	AVSS/VSS	41	AN15/OCM1D/RC5
18	AVDD/VDD	42	VSS
19	$\overline{\text{MCLR}}$	43	VDD
20	AN19/U1RX/RA6	44	U1TX/RC12
21	PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0	45	PGED3/**RP11**/ASDA1(2)/USBID/$\overline{\text{SS3}}$/FSYNC3/OCM3E/RB5
22	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	46	VBUS/RB6
23	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	47	**RP12**/SDA3/OCM3F/RB7
24	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	48	TCK/**RP13**/SCL1/$\overline{\text{U1CTS}}$/SCK1/OCM1A/RB8(1)

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

64-Pin QFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 64-PIN QFN/TQFP DEVICES

Pin	Function	Pin	Function
1	**RP21**/SDI3/RA7	33	OCM3B/RD3
2	CVREF/AN9/C3INB/**RP16**/VBUSON/RB14	34	REFCLKI/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/RD0(1)
3	AN10/C3INA/REFCLKO/**RP17**/RB15(1)	35	OCM2B/RC3
4	AVSS	36	OCM1E/INT3/RC4
5	AVDD	37	AN15/OCM1D/RC5
6	AN16/$\overline{\text{U1CTS}}$/RA13	38	VSS
7	AN17/OCM1A/RA12	39	VDD
8	AN18/RA11	40	U1TX/RC12
9	$\overline{\text{MCLR}}$	41	OCM3D/RC14
10	AN19/U1RX/RA6	42	OCM3E/RC15
11	PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0	43	PGED3/**RP11**/ASDA1(2)/USBID/RB5
12	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	44	VBUS/RB6
13	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	45	OCM3F/RC10
14	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	46	**RP12**/SDA3/RB7
15	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	47	SCK1/RC13(1)
16	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	48	TCK/**RP13**/SCL1/RB8(1)
17	VDD	49	TMS/**RP14**/SDA1/INT2/RB9(1)
18	VSS	50	**RP23**/RC6
19	AN12/C2IND/T2CK/T2G/RC0	51	**RP20**/RC7
20	AN13/T3CK/T3G/RC1	52	AN14/LVDIN/C2INC/RC8
21	**RP19**/OCM2A/RC2	53	OCM1B/RD1
22	$\overline{\text{SS3}}$/FSYNC3/RC11	54	OCM3A/RA5
23	VDD	55	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1)
24	VSS	56	VCAP
25	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	57	VDD
26	OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1)	58	RTCC/RA15
27	SDO3/RA8(1)	59	OCM3C/RA14
28	SOSCI/AN7/**RP10**/RB4	60	D-/RB10
29	SOSCO/SCLKI/**RP5**/PWRLCLK/RA4	61	D+/RB11
30	**RP24**/RA9	62	VUSB3V3
31	SDI1/INT1/RD4	63	AN8/**RP15**/SCL3/RB13(1)
32	$\overline{\text{SS1}}$/FSYNC1/INT0/RD2	64	**RP22**/SCK3/RA10(1)

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Table of Contents

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 5. "Flash Programming"** (DS60001121)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupts"** (DS61108)
- **Section 10. "Power-Saving Modes"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 14. "Timers"** (DS60001105)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference"** (DS61109)
- **Section 21. "UART"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 24. "Inter-Integrated Circuit™ (I^2C™)"** (DS61116)
- **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359)
- **Section 27. "USB On-The-Go (OTG)"** (DS61126)
- **Section 28. "RTCC with Timestamp"** (DS60001362)
- **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381)
- **Section 31. "DMA Controller"** (DS60001117)
- **Section 33. "Programming and Diagnostics"** (DS61129)
- **Section 36. "Configurable Logic Cell"** (DS60001363)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 59. "Oscillators with DCO"** (DS60001329)
- **Section 62. "Dual Watchdog Timer"** (DS60001365)

NOTES:

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0256GPM064 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0256GPM064 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0256GPM064 FAMILY BLOCK DIAGRAM

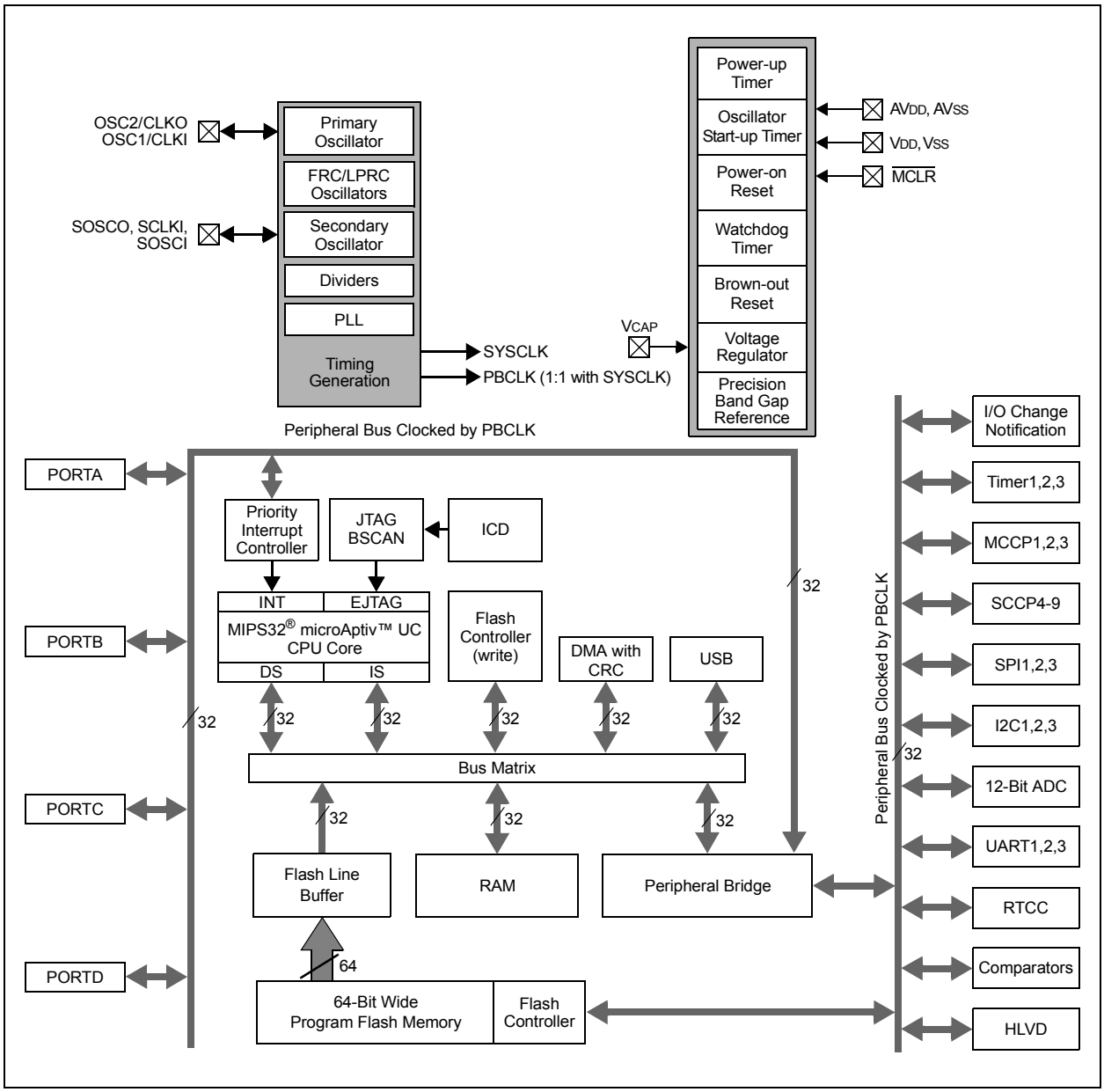


TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
AN0	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter input channels
AN1	3	28	34	37	22	12	I	ANA	
AN2	4	1	35	38	23	13	I	ANA	
AN3	5	2	36	39	24	14	I	ANA	
AN4	6	3	1	1	25	15	I	ANA	
AN5	9	6	7	7	32	25	I	ANA	
AN6	10	7	8	8	33	26	I	ANA	
AN7	11	8	9	9	35	28	I	ANA	
AN8	24	21	27	30	12	63	I	ANA	
AN9	25	22	28	31	15	2	I	ANA	
AN10	26	23	29	32	16	3	I	ANA	
AN11	7	4	2	2	26	16	I	ANA	
AN12	—	—	3	3	27	19	I	ANA	
AN13	—	—	4	4	28	20	I	ANA	
AN14	—	—	20	21	4	52	I	ANA	
AN15	—	—	—	—	41	37	I	ANA	
AN16	—	—	—	—	—	6	I	ANA	
AN17	—	—	—	—	—	7	I	ANA	
AN18	—	—	—	—	—	8	I	ANA	
AN19	—	—	—	—	—	10	I	ANA	
AV_{DD}	28	25	31	34	18	5	P	—	Analog modules power supply
AV_{SS}	27	24	30	33	17	4	P	—	Analog modules ground
C1INA	7	4	2	2	26	16	I	ANA	Comparator 1 Input A
C1INB	6	3	1	1	25	15	I	ANA	Comparator 1 Input B
C1INC	5	2	36	39	24	14	I	ANA	Comparator 1 Input C
C1IND	4	1	35	38	23	13	I	ANA	Comparator 1 Input D
C2INA	5	2	36	39	24	14	I	ANA	Comparator 2 Input A
C2INB	4	1	35	38	23	13	I	ANA	Comparator 2 Input B
C2INC	—	—	20	21	4	52	I	ANA	Comparator 2 Input C
C2IND	—	—	3	3	27	19	I	ANA	Comparator 2 Input D
C3INA	26	23	29	32	16	3	I	ANA	Comparator 3 Input A
C3INB	25	22	28	31	15	2	I	ANA	Comparator 3 Input B
C3INC	4	1	35	38	23	13	I	ANA	Comparator 3 Input C
C3IND	10	7	8	8	33	26	I	ANA	Comparator 3 Input D
CLKI	9	6	7	7	32	25	I	ST	External Clock source input (EC mode)
CLKO	10	7	8	8	33	26	O	DIG	System clock output
CV_{REF}	25	22	28	31	15	2	O	ANA	Comparator voltage reference output
CV_{REF+}	2	27	33	36	21	11	I	ANA	Positive comparator voltage reference input
D+	22	19	25	28	10	61	I/O	—	USB transceiver differential plus line
D-	21	18	24	27	9	60	I/O	—	USB transceiver differential minus line
FSYNC1	26	23	29	32	16	32	I/O	ST/DIG	SPI1 frame signal input or output
FSYNC3	14	11	15	15	45	22	I/O	ST/DIG	SPI3 frame signal input or output

Legend: ST = Schmitt Trigger input buffer; I2C = I^2C/SMBus input buffer; DIG = Digital input/output; ANA = Analog level input/output; P = Power

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
INT0	26	23	29	32	16	32	I	ST	External Interrupt 0
INT1	25	22	28	31	15	31	I	ST	External Interrupt 1
INT2	18	15	19	20	1	49	I	ST	External Interrupt 2
INT3	2	27	33	36	40	36	I	ST	External Interrupt 3
LVDIN	24	21	20	21	4	52	I	ANA	High/Low-Voltage Detect input
$\overline{MCLR}$	1	26	32	35	19	9	I	ST	Master Clear (device Reset)
OCM1A	17	14	18	18	48	7	O	DIG	MCCP1 Output A
OCM1B	18	15	19	20	1	53	O	DIG	MCCP1 Output B
OCM1C	9	6	7	7	32	25	O	DIG	MCCP1 Output C
OCM1D	10	7	8	8	41	37	O	DIG	MCCP1 Output D
OCM1E	2	27	33	36	40	36	O	DIG	MCCP1 Output E
OCM1F	3	28	34	37	22	12	O	DIG	MCCP1 Output F
OCM2A	19	16	5	5	29	21	O	DIG	MCCP2 Output A
OCM2B	26	23	29	32	39	35	O	DIG	MCCP2 Output B
OCM2C	4	1	35	38	23	13	O	DIG	MCCP2 Output C
OCM2D	5	2	36	39	24	14	O	DIG	MCCP2 Output D
OCM2E	6	3	1	1	25	15	O	DIG	MCCP2 Output E
OCM2F	7	4	2	2	26	16	O	DIG	MCCP2 Output F
OCM3A	24	21	11	11	37	54	O	DIG	MCCP3 Output A
OCM3B	25	22	28	31	15	33	O	DIG	MCCP3 Output B
OCM3C	11	8	9	9	35	59	O	DIG	MCCP3 Output C
OCM3D	12	9	10	10	36	41	O	DIG	MCCP3 Output D
OCM3E	14	11	15	15	45	42	O	DIG	MCCP3 Output E
OCM3F	16	13	17	17	47	45	O	DIG	MCCP3 Output F
OSC1	9	6	7	7	32	25	—	—	Primary Oscillator crystal
OSC2	10	7	8	8	33	26	—	—	Primary Oscillator crystal
PGEC1	5	2	36	39	24	14	I	ST	ICSP™ Port 1 programming clock input
PGEC2	2	27	33	36	21	11	I	ST	ICSP Port 2 programming clock input
PGEC3	19	16	21	22	5	55	I	ST	ICSP Port 3 programming clock input
PGED1	4	1	35	38	23	13	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	3	28	34	37	22	12	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	14	11	15	15	45	43	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	12	9	10	10	36	29	I	ST	Real-Time Clock 50/60 Hz clock input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RA0	2	27	33	36	21	11	I/O	ST/DIG	PORTA digital I/Os
RA1	3	28	34	37	22	12	I/O	ST/DIG	
RA2	9	6	7	7	32	25	I/O	ST/DIG	
RA3	10	7	8	8	33	26	I/O	ST/DIG	
RA4	12	9	10	10	36	29	I/O	ST/DIG	
RA5	—	—	—	—	—	54	I/O	ST/DIG	
RA6	—	—	—	—	20	10	I/O	ST/DIG	
RA7	—	—	—	—	14	1	I/O	ST/DIG	
RA8	—	—	—	—	34	27	I/O	ST/DIG	
RA9	—	—	11	11	37	30	I/O	ST/DIG	
RA10	—	—	—	—	13	64	I/O	ST/DIG	
RA11	—	—	—	—	—	8	I/O	ST/DIG	
RA12	—	—	—	—	—	7	I/O	ST/DIG	
RA13	—	—	—	—	—	6	I/O	ST/DIG	
RA14	—	—	—	—	—	59	I/O	ST/DIG	
RA15	—	—	—	—	8	58	I/O	ST/DIG	
RB0	4	1	35	38	23	13	I/O	ST/DIG	PORTB digital I/Os
RB1	5	2	36	39	24	14	I/O	ST/DIG	
RB2	6	3	1	1	25	15	I/O	ST/DIG	
RB3	7	4	2	2	26	16	I/O	ST/DIG	
RB4	11	8	9	9	35	28	I/O	ST/DIG	
RB5	14	11	15	15	45	43	I/O	ST/DIG	
RB6	15	12	16	16	46	44	I/O	ST/DIG	
RB7	16	13	17	17	47	46	I/O	ST/DIG	
RB8	17	14	18	18	48	48	I/O	ST/DIG	
RB9	18	15	19	20	1	49	I/O	ST/DIG	
RB10	21	18	24	27	9	60	I/O	ST/DIG	
RB11	22	19	25	28	10	61	I/O	ST/DIG	
RB13	24	21	27	30	12	63	I/O	ST/DIG	
RB14	25	22	28	31	15	2	I/O	ST/DIG	
RB15	26	23	29	32	16	3	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RC0	—	—	3	3	27	19	I/O	ST/DIG	PORTC digital I/Os
RC1	—	—	4	4	28	20	I/O	ST/DIG	
RC2	—	—	5	5	29	21	I/O	ST/DIG	
RC3	—	—	14	14	39	35	I/O	ST/DIG	
RC4	—	—	—	—	40	36	I/O	ST/DIG	
RC5	—	—	—	—	41	37	I/O	ST/DIG	
RC6	—	—	—	—	2	50	I/O	ST/DIG	
RC7	—	—	—	—	3	51	I/O	ST/DIG	
RC8	—	—	20	21	4	52	I/O	ST/DIG	
RC9	19	16	21	22	5	55	I/O	ST/DIG	
RC10	—	—	—	—	—	45	I/O	ST/DIG	
RC11	—	—	—	—	—	22	I/O	ST/DIG	
RC12	—	—	—	—	44	40	I/O	ST/DIG	
RC13	—	—	—	—	—	47	I/O	ST/DIG	
RC14	—	—	—	—	—	41	I/O	ST/DIG	
RC15	—	—	—	—	—	42	I/O	ST/DIG	
RD0	—	—	—	—	38	34	I/O	ST/DIG	PORTD digital I/Os
RD1	—	—	—	—	—	53	I/O	ST/DIG	
RD2	—	—	—	—	—	32	I/O	ST/DIG	
RD3	—	—	—	—	—	33	I/O	ST/DIG	
RD4	—	—	—	—	—	31	I/O	ST/DIG	
REFCLKI	18	15	19	20	38	34	I	ST	External reference clock input
REFCLKO	26	23	29	32	16	3	O	ST	External reference clock output
RP1	2	27	33	36	21	11	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	3	28	34	37	22	12	I/O	ST/DIG	
RP3	9	6	7	7	32	25	I/O	ST/DIG	
RP4	10	7	8	8	33	26	I/O	ST/DIG	
RP5	12	9	10	10	36	29	I/O	ST/DIG	
RP6	4	1	35	38	23	13	I/O	ST/DIG	
RP7	5	2	36	39	24	14	I/O	ST/DIG	
RP8	6	3	1	1	25	15	I/O	ST/DIG	
RP9	7	4	2	2	26	16	I/O	ST/DIG	
RP10	11	8	9	9	35	28	I/O	ST/DIG	
RP11	14	11	15	15	45	43	I/O	ST/DIG	
RP12	16	13	17	17	47	46	I/O	ST/DIG	
RP13	17	14	18	18	48	48	I/O	ST/DIG	
RP14	18	15	19	20	1	49	I/O	ST/DIG	
RP15	24	21	27	30	12	63	I/O	ST/DIG	
RP16	25	22	28	31	15	2	I/O	ST/DIG	
RP17	26	23	29	32	16	3	I/O	ST/DIG	
RP18	19	16	21	22	5	55	I/O	ST/DIG	
RP19	—	—	5	5	29	21	I/O	ST/DIG	
RP20	—	—	—	—	3	51	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer; I2C = I^2C/SMBus input buffer; DIG = Digital input/output; ANA = Analog level input/output; P = Power

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RP21	—	—	—	—	14	1	I/O	ST/DIG	Remappable peripherals (input or output)
RP22	—	—	—	—	13	64	I/O	ST/DIG	
RP23	—	—	—	—	2	50	I/O	ST/DIG	
RP24	—	—	11	11	37	30	I/O	ST/DIG	
RTCC	25	22	28	31	8	58	O	DIG	Real-Time Clock/Calendar alarm/seconds output
SCK1	17	14	18	18	48	47	I/O	ST/DIG	SPI1 clock (input or output)
SCK3	24	21	27	30	13	64	I/O	ST/DIG	SPI3 clock (input or output)
SCL1	17	14	18	18	48	48	I/O	I2C	I2C1 synchronous serial clock input/output
ASCL1	19	16	21	22	5	55	I/O	I2C	Alternate I2C1 synchronous serial clock input/ output
SCL2	7	4	2	2	26	16	I/O	I2C	I2C2 synchronous serial clock input/output
SCL3	24	21	27	30	12	63	I/O	I2C	I2C3 synchronous serial clock input/output
SCLKI	12	9	10	10	36	29	I	ST	Secondary Oscillator digital clock input
SDA1	18	15	19	20	1	49	I/O	I2C	I2C1 data input/output
ASDA1	14	11	15	15	45	43	I/O	I2C	Alternate I2C1 data input/output
SDA2	6	3	1	1	25	15	I/O	I2C	I2C2 data input/output
SDA3	16	13	17	17	47	46	I/O	I2C	I2C3 data input/output
SDI1	25	22	28	31	15	31	I	ST	SPI1 data input
SDI3	16	13	17	17	14	1	I	ST	SPI3 data input
SDO1	18	15	19	20	38	34	O	DIG	SPI1 data output
SDO3	19	16	21	22	34	27	O	DIG	SPI3 data output
SOSCI	11	8	9	9	35	28	—	—	Secondary Oscillator crystal
SOSCO	12	9	10	10	36	29	—	—	Secondary Oscillator crystal
$\overline{SS1}$	26	23	29	32	16	32	I	ST	SPI1 slave select input
$\overline{SS3}$	14	11	15	15	45	22	I	ST	SPI3 slave select input
T1CK	18	15	19	20	38	34	I	ST	Timer1 external clock input
T2CK	18	15	3	3	27	19	I	ST	Timer2 external clock input
T3CK	19	16	4	4	28	20	I	ST	Timer3 external clock input
T1G	18	15	19	20	38	34	I	ST	Timer1 clock gate input
T2G	18	15	3	3	27	19	I	ST	Timer2 clock gate input
T3G	19	16	4	4	28	20	I	ST	Timer3 clock gate input
TCK	17	14	18	18	48	48	I	ST	JTAG clock input
TDI	7	4	2	2	26	16	I	ST	JTAG data input
TDO	19	16	21	22	5	55	O	DIG	JTAG data output
TMS	18	15	19	20	1	49	I	ST	JTAG mode select input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
U1BCLK	18	15	19	20	38	34	O	DIG	UART1 IrDA® 16x baud clock output
U1CTS	17	14	18	18	48	6	I	ST	UART1 Clear-to-Send
U1RTS	18	15	19	20	38	34	O	DIG	UART1 Ready-to-Send
U1RX	26	23	29	32	20	10	I	ST	UART1 receive data input
U1TX	25	22	28	31	44	40	O	DIG	UART1 transmit data output
USBID	14	11	15	15	45	43	I	ST	USB OTG ID (OTG mode only)
USBOEN	19	16	21	22	5	55	O	—	USB transceiver output enable flag
VBUSON	25	22	28	31	15	2	O	—	USB host and On-The-Go (OTG) bus power control output
VBUS	15	12	16	16	46	44	P	—	USB VBUS connection (5V nominal)
VUSB3V3	23	20	26	29	11	62	P	—	USB transceiver power input (3.3V nominal)
VCAP	20	17	22	24	7	56	P	—	Core voltage regulator filter capacitor connection
VDD	13,28	10,25	13,23,31	13,26, 34	18,30, 43	17,23, 39,57	P	—	Digital modules power supply
VREF-	3	28	34	37	22	12	I	ANA	Analog-to-Digital Converter negative reference
VREF+	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter positive reference
VSS	8,27	5,24	6,12,30	6,12,33	6,17,31, 42	18,24, 38	P	—	Digital modules ground

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0256GPM064 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pin (see **Section 2.4 "Voltage Regulator Pin (VCAP)"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **Section 2.7 "External Oscillator Pins"**)
- VUSB3V3 pin, this pin must be powered for USB operation (see **Section 18.4 "Powering the USB Transceiver"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

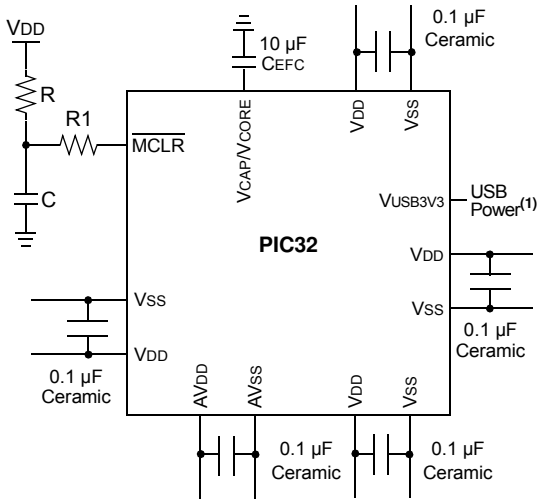
2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: Refer to **Section 18.4 "Powering the USB Transceiver"** for requirements of this pin.

2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

- Device Reset
- Device Programming and Debugging

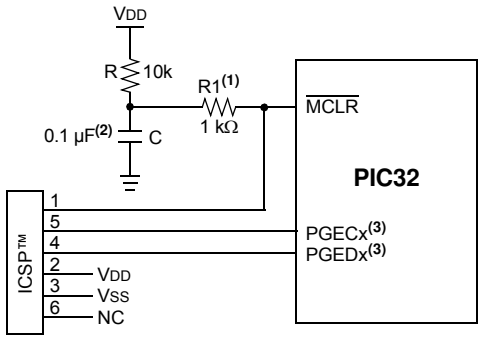
Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

Note: When MCLR is used to wake the device from Retention Sleep, a POR Reset will occur.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS(1,2,3)



Note 1: 470Ω ≤ R1 ≤ 1 kΩ will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin V_{IH} and V_{IL} specifications are met without interfering with the debugger/programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

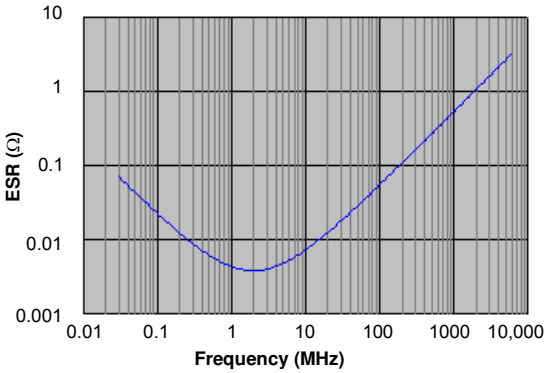
2.4 Voltage Regulator Pin (VCAP)

A low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the output voltage of the on-chip voltage regulator. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 "Electrical Characteristics"** for additional information.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM319R61C106KE15D	10 µF	±10%	16V	-55 to +85ºC