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PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

32-bit XLP Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog

Operating Conditions

- 2.5V to 3.6V, -40ºC to +85ºC, DC to 72 MHz
- 2.5V to 3.6V, -40ºC to +105ºC, DC to 72 MHz

Core: 72 MHz/116 DMIPS MIPS32® M4K®

- MIPS16e® mode for up to 40% smaller code size
- Code-efficient (C and Assembly) architecture
- Single-cycle (MAC) 32x16 and two-cycle 32x32 multiply

Clock Management

- 0.9% internal oscillator
- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Fast wake-up and start-up

Power Management

- Various power management options for extreme power reduction (VBAT, Deep Sleep, Sleep, and Idle)
- Deep Sleep current: 673 nA (typical)
- Integrated POR and BOR
- Programmable High/Low-Voltage Detect (HLVD) on VDD

Audio Interface Features

- Data communication: I^2S, LJ, RJ, and DSP modes
- Control interface: SPI and I^2C
- Master clock:
  - Generation of fractional clock frequencies
  - Can be synchronized with USB clock
  - Can be tuned in run-time

Advanced Analog Features

- ADC Module:
  - 10-bit 1.1 Msps rate with one S&H
  - Up to 10 analog inputs on 28-pin devices and 13 analog inputs on 44-pin devices
- Flexible and independent ADC trigger sources
- Charge Time Measurement Unit (CTMU):
  - Supports mTouch™ capacitive touch sensing
  - Provides high-resolution time measurement (1 ns)
  - On-chip temperature measurement capability
- Comparators:
  - Up to three Analog Comparator modules
  - Programmable references with 32 voltage points

Timers/Output Compare/Input Capture

- Five General Purpose Timers:
  - Five 16-bit and up to two 32-bit Timers/Counters
- Five Output Compare (OC) modules
- Five Input Capture (IC) modules
- Peripheral Pin Select (PPS) to allow function remap
- Real-Time Clock and Calendar (RTCC) module

Communication Interfaces

- USB 2.0-compliant Full-speed OTG controller
- Two UART modules (17.5 Mbps):
  - Supports LIN 2.0 protocols and IrDA® support
- Two 4-wire SPI modules (25 Mbps)
- Two I^2C modules (up to 1 Mbaud) with SMBus support
- PPS to allow function remap
- Parallel Master Port (PMP)

Direct Memory Access (DMA)

- Four channels of hardware DMA with automatic data size detection
- Two additional channels dedicated for USB
- Programmable Cyclic Redundancy Check (CRC)

Input/Output

- 10 mA source/sink on all I/O pins and up to 14 mA on non-standard VOH
- 5V-tolerant pins
- Selectable open drain, pull-ups, and pull-downs
- External interrupts on all I/O pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 2 -40ºC to +105ºC) (planned)
- Class B Safety Library, IEC 60730 (planned)

Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited program and six complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan

Integrated Software Libraries and Tools

- C/C++ compiler with native DSP/fractional support
- MPLAB® Harmony Integrated Software Framework
- USB stack

Packages

Type	SOIC	QFN		TQFP
Pin Count	28	28	44	44
I/O Pins (up to)	21	21	34	34
Contact/Lead Pitch	1.27	0.65	0.65	0.80
Dimensions	17.90x10.30x2.65	6x6x0.9	8x8x0.9	10x10x1.0

Note: All dimensions are in millimeters (mm) unless specified.

TABLE 1: PIC32MX1XX 28/44-PIN XLP (GENERAL PURPOSE) FAMILY FEATURES

Device	Pins	Program Memory (KB)(1)	Data Memory (KB)	Remappable Peripherals					Analog Comparators	I²C™	PMP	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	VBAT	Packages
				Remappable Pins	Timers(2)/Capture/ Compare/PWM	UART	SPI/I²S	External Interrupts(3)											
PIC32MX154F128B	28	128+12	32	20	5/5/5/5	2	2	5	3	2	Y	4/2	Y	10	Y	21	Y	N	SOIC, QFN
PIC32MX154F128D	44			30										13		35		N	TQFP, QFN
PIC32MX155F128B	28			19										9		20		Y	SOIC, QFN
PIC32MX155F128D	44			29										12		35		Y	TQFP, QFN
PIC32MX174F256B	28	256+12	64	20	5/5/5/5	2	2	5	3	2	Y	4/2	Y	10	Y	21	Y	N	SOIC, QFN
PIC32MX174F256D	44			30										13		35		N	TQFP, QFN
PIC32MX175F256B	28			19										9		20		Y	SOIC, QFN
PIC32MX175F256D	44			29										12		35		Y	TQFP, QFN

Note 1: This device features 12 KB of Boot Flash memory.
2: Four out of five timers are remappable.
3: Four out of five external interrupts are remappable.

TABLE 2: PIC32MX2XX 28/44-PIN XLP (USB) FAMILY FEATURES

Device	Pins	Program Memory (KB)(1)	Data Memory (KB)	Remappable Peripherals					Analog Comparators	USB On-The-Go (OTG)	I²C™	PMP	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	VBAT	Packages
				Remappable Pins	Timers(2)/Capture/ Compare/PWM	UART	SPI/I²S	External Interrupts(3)												
PIC32MX254F128B	28	128+12	32	17	5/5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	17	Y	N	SOIC, QFN
PIC32MX254F128D	44			29											13		35		N	TQFP, QFN
PIC32MX255F128B	28			16											8		16		Y	SOIC, QFN
PIC32MX255F128D	44			28											12		35		Y	TQFP, QFN
PIC32MX274F256B	28	256+12	64	17	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	17	Y	N	SOIC, QFN
PIC32MX274F256D	44			29											13		35		N	TQFP, QFN
PIC32MX275F256B	28			16											8		16		Y	SOIC, QFN
PIC32MX275F256D	44			28											12		35		Y	TQFP, QFN

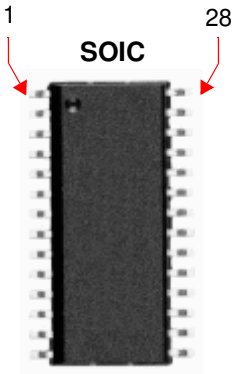
Note 1: This device features 12 KB of Boot Flash memory.
2: Four out of five timers are remappable.
3: Four out of five external interrupts are remappable.

Pin Diagrams

TABLE 3: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITH VBAT

28-PIN SOIC (TOP VIEW)(1,2,3)

PIC32MX155F128B
PIC32MX175F256B



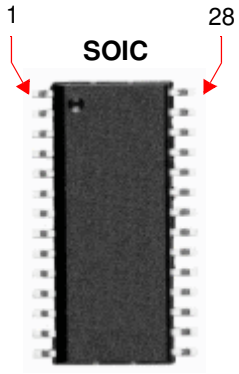
Pin #	Full Pin Name	Pin #	Full Pin Name
1	MCLR	15	PGEC3/RPB6/ASCL2/PMD6/RB6
2	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA1/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	VREF-/AN1/RPA1/ASCL1/CTED2/PMRD/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12//RB1	19	VSS
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	20	VCAP
7	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/RB3	21	PGED1/RPB10/CTED11/PMD2/RB10
8	VSS	22	PGEC1/TMS/RPB11/PMD1/RB11
9	OSC1/CLKI/RPA2/RA2	23	AN12/PMD0/RB12
10	OSC2/CLKO/RPA3/PMA0/RA3	24	VBAT
11	SOSCI/RPB4/RB4(4)	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
12	SOSCO/RPA4/T1CK/CTED9/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	VDD	27	AVSS
14	PGED3/RPB5/ASDA2/PMD7/RB5	28	AVDD

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This is an input-only pin.

TABLE 4: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITHOUT VBAT

28-PIN SOIC (TOP VIEW)(1,2,3)

PIC32MX154F128B
PIC32MX174F256B



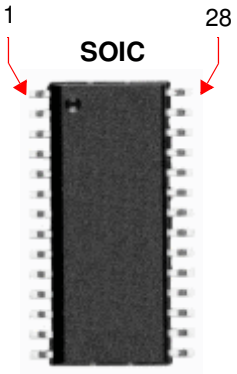
Pin #	Full Pin Name	Pin #	Full Pin Name
1	$\overline{\text{MCLR}}$	15	PGEC3/RPB6/ASCL2/PMD6/RB6
2	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA1/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	VREF-/AN1/RPA1/ASCL1/CTED2/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12//RB1	19	VSS
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	20	VCAP
7	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	21	PGED1/RPB10/CTED11/PMD2/RB10
8	VSS	22	PGEC1/TMS/RPB11/PMD1/RB11
9	OSC1/CLKI/RPA2/RA2	23	AN12/PMD0/RB12
10	OSC2/CLKO/RPA3/PMA0/RA3	24	AN11/RPB13/CTPLS/PMRD/RB13
11	SOSCI/RPB4/RB4(4)	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
12	SOSCO/RPA4/T1CK/CTED9/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	VDD	27	AVSS
14	PGED3/RPB5/ASDA2/PMD7/RB5	28	AVDD

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This is an input-only pin.

TABLE 5: PIN NAMES FOR 28-PIN USB DEVICES WITH VBAT

28-PIN SOIC (TOP VIEW)(1,2,3)

PIC32MX255F128B
PIC32MX275F256B



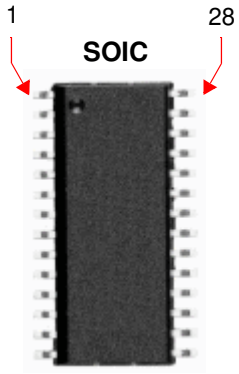
Pin #	Full Pin Name	Pin #	Full Pin Name
1	MCLR	15	VBUS
2	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1	19	VSS
6	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	20	VCAP
7	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMWR/RB3	21	D+
8	VSS	22	D-
9	OSC1/CLKI/RPA2/RA2	23	VUSB3V3
10	OSC2/CLKO/RPA3/PMA0/RA3	24	VBAT
11	SOSCI/RPB4/CTED11/RB4(4)	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
12	SOSCO/RPA4/T1CK/CTED9/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	VDD	27	AVSS
14	TMS/RPB5/USBID/PMRD/RB5	28	AVDD

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This is an input-only pin.

TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES WITHOUT VBAT

28-PIN SOIC (TOP VIEW)(1,2,3)

PIC32MX254F128B
PIC32MX274F256B



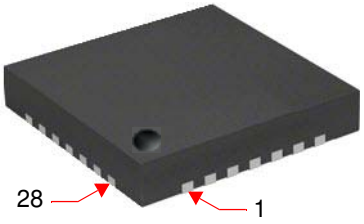
Pin #	Full Pin Name	Pin #	Full Pin Name
1	$\overline{\text{MCLR}}$	15	VBUS
2	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1	19	VSS
6	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	20	VCAP
7	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	21	D+
8	VSS	22	D-
9	OSC1/CLKI/RPA2/RA2	23	VUSB3V3
10	OSC2/CLKO/RPA3/PMA0/RA3	24	AN11/RPB13/CTPLS/PMRD/RB13
11	SOSCI/RPB4/CTED11/RB4(4)	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
12	SOSCO/RPA4/T1CK/CTED9/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	VDD	27	AVSS
14	TMS/RPB5/USBID/RB5	28	AVDD

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This is an input-only pin.

TABLE 7: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITH VBAT

28-PIN QFN (TOP VIEW)(1,2,3.4)

PIC32MX155F128D
PIC32MX175F256D



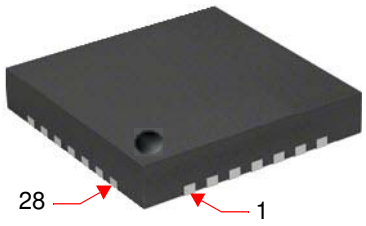
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1	16	VSS
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/RB3	18	PGED1/RPB10/CTED11/PMD2/RB10
5	VSS	19	PGEC1/TMS/RPB11/PMD1/RB11
6	OSC1/CLKI/RPA2/RA2	20	AN12/PMD0/RB12
7	OSC2/CLKO/RPA3/PMA0/RA3	21	VBAT
8	SOSCI/RPB4/RB4(5)	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
9	SOSCO/RPA4/T1CK/CTED9/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	VDD	24	AVSS
11	PGED3/RPB5/ASDA2/PMD7/RB5	25	AVDD
12	PGEC3/RPB6/ASCL2/PMD6/RB6	26	$\overline{\text{MCLR}}$
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	VREF+/AN0/C3INC/RPA0ASDA1//CTED1/PMA1/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	VREF-/AN1/RPA1/ASCL1/CTED2/PMRD/RA1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.
5: This is an input-only pin.

TABLE 8: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITHOUT VBAT

28-PIN QFN (TOP VIEW)(1,2,3.4)

PIC32MX154F128B
PIC32MX174F256B



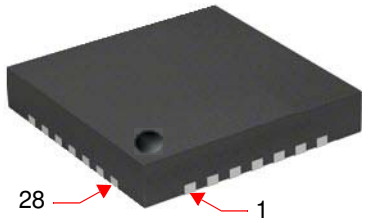
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1	16	VSS
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	18	PGED1/RPB10/CTED11/PMD2/RB10
5	VSS	19	PGEC1/TMS/RPB11/PMD1/RB11
6	OSC1/CLKI/RPA2/RA2	20	AN12/PMD0/RB12
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4(5)	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
9	SOSCO/RPA4/T1CK/CTED9/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	VDD	24	AVSS
11	PGED3/RPB5/ASDA2/PMD7/RB5	25	AVDD
12	PGEC3/RPB6/ASCL2/PMD6/RB6	26	$\overline{\text{MCLR}}$
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA1/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	VREF-/AN1/RPA1/ASCL1/CTED2/RA1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.
5: This is an input-only pin.

TABLE 9: PIN NAMES FOR 28-PIN USB DEVICES WITH VBAT

28-PIN QFN (TOP VIEW)(1,2,3,4)

PIC32MX255F128B
PIC32MX275F256B



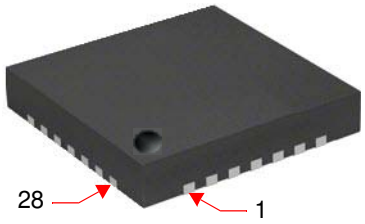
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1/RB1	16	VSS
3	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	VCAP
4	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMWR/RB3	18	D+
5	VSS	19	D-
6	OSC1/CLKI/RPA2/RA2	20	VUSB3V3
7	OSC2/CLKO/RPA3/PMA0/RA3	21	VBAT
8	SOSCI/RPB4/CTED11/RB4(5)	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
9	SOSCO/RPA4/T1CK/CTED9/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	VDD	24	AVSS
11	TMS/RPB5/USBID/PMRD/RB5	25	AVDD
12	VBUS	26	MCLR
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.
5: This is an input-only pin.

TABLE 10: PIN NAMES FOR 28-PIN USB DEVICES WITHOUT VBAT

28-PIN QFN (TOP VIEW)(1,2,3,4)

PIC32MX254F128B
PIC32MX274F256B



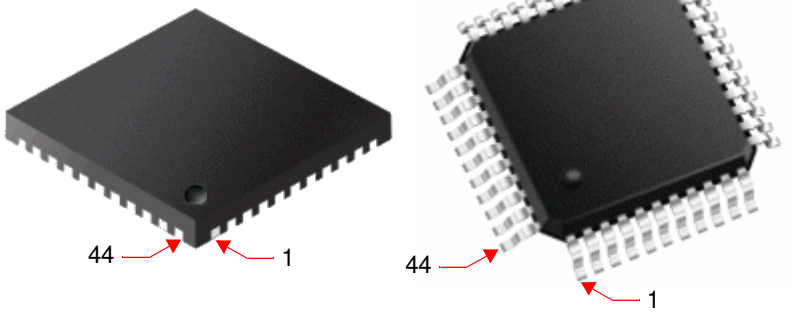
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1/RB1	16	VSS
3	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	VCAP
4	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	18	D+
5	VSS	19	D-
6	OSC1/CLKI/RPA2/RA2	20	VUSB3V3
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/CTED11/RB4(5)	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
9	SOSCO/RPA4/T1CK/CTED9/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	VDD	24	AVSS
11	TMS/RPB5/USBID/RB5	25	AVDD
12	VBUS	26	$\overline{\text{MCLR}}$
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.
5: This is an input-only pin.

TABLE 11: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES WITH VBAT

44-PIN QFN AND TQFP (TOP VIEW)(1,2,3,5)

PIC32MX155F128D
PIC32MX175F256D



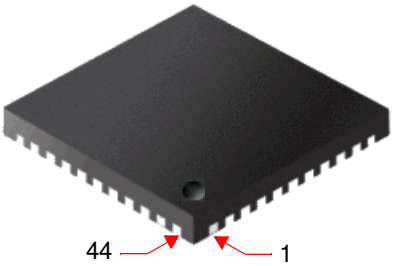
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMA2/RB3
3	RPC7/PMCS1/RC7	25	AN6/RPC0/RC0
4	RPC8/PMD5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMD6/RC9	27	AN8/RPC2/PMWR/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	PGED1/RPB10/CTED11/PMA8/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC1/TMS/RPB11/PMA9/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMD2/RA8
11	VBAT	33	SOSCI/RPB4/RB4
12	PGED4/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4/TCK/CTED8/PMD3/RA7	35	TDI/RPA9/PMD1/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14	36	RPC3/PMRD/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15	37	RPC4/PMD4/RC4
16	AVSS	38	RPC5/PMD7/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/RA0	41	PGED3/RPB5/ASDA2/PMA3/RB5
20	VREF-/AN1/RPA1/ASCL1/CTED2/RA1	42	PGEC3/RPB6/ASCL2/PMA6/RB6
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMA5/INT0/RB7
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMA4/RB8

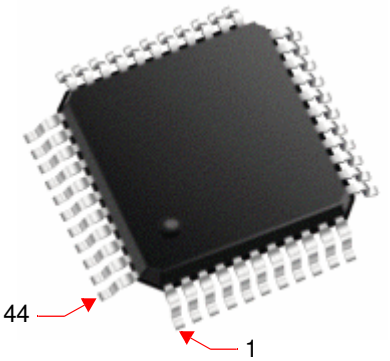
Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.

TABLE 12: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES WITHOUT VBAT

44-PIN QFN AND TQFP (TOP VIEW)(1,2,3,5)

PIC32MX154F128D
PIC32MX174F256D





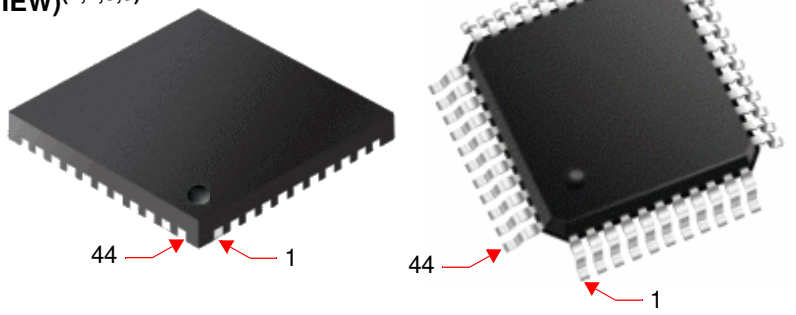
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMA2/RB3
3	RPC7/PMCS1/RC7	25	AN6/RPC0/RC0
4	RPC8/PMD5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMD6/RC9	27	AN8/RPC2/PMWR/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	PGED1/RPB10/CTED11/PMA8/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC1/TMS/RPB11/PMA9/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMD2/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/CTED11/RB4
12	PGED4/PMA10/RA10	34	SOSCO/RPA4/T1CK/RA4
13	PGEC4/TCK/CTED8/PMD3/RA7	35	TDI/RPA9/PMD1/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15	37	RPC4/PMD4/RC4
16	AVSS	38	RPC5/PMD7/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/RA0	41	PGED3/RPB5/ASDA2/PMA3/RB5
20	VREF-/AN1/RPA1/ASCL1/CTED2/RA1	42	PGEC3/RPB6/ASCL2/PMA6/RB6
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMA5/INT0/RB7
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMA4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.

TABLE 13: PIN NAMES FOR 44-PIN USB DEVICES WITH VBAT

44-PIN QFN AND TQFP (TOP VIEW)(1,2,3,5)

PIC32MX255F128D
PIC32MX275F256D



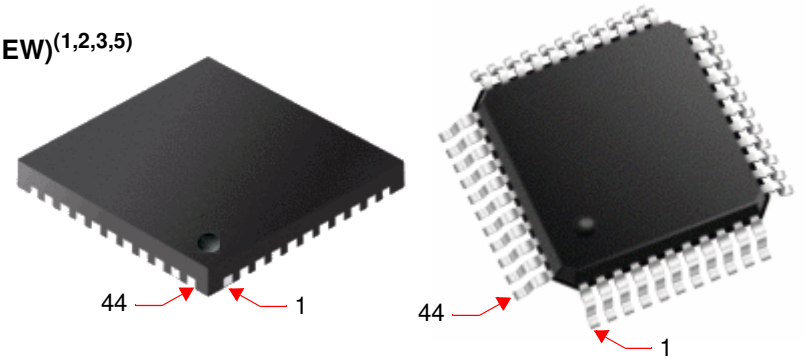
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9	23	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMA8/RB2
2	RPC6/PMA1/RC6	24	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMA2/RB3
3	RPC7/PMCS1/RC7	25	AN6/RPC0/RC0
4	RPC8/PMD5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMD6/RC9	27	AN8/RPC2/PMWR/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	D+	30	OSC1/CLKI/RPA2/RA2
9	D-	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMD2/RA8
11	VBAT	33	SOSCI/RPB4/CTED11/RB4
12	PGED4/PMD0/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4/TCK/CTED8/PMD3/RA7	35	TDI/RPA9/PMD1/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14	36	AN12/RPC3/PMRD/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15	37	RPC4/PMD4/RC4
16	AVSS	38	RPC5/PMD7/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA3/RA0	41	TMS/RPB5/USBID/RB5
20	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMA6/RA1	42	VBUS
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMA10/RB0	43	RPB7/CTED3/PMA5/INT0/RB7
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMA9/RB1	44	RPB8/SCL1/CTED10/PMA4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.

TABLE 14: PIN NAMES FOR 44-PIN USB DEVICES WITHOUT VBAT

44-PIN QFN AND TQFP (TOP VIEW)(1,2,3,5)

PIC32MX254F128D
PIC32MX274F256D



Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9	23	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMA8/RB2
2	RPC6/PMA1/RC6	24	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMA2/RB3
3	RPC7/PMCS1/RC7	25	AN6/RPC0/RC0
4	RPC8/PMD5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMD6/RC9	27	AN8/RPC2/PMWR/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	D+	30	OSC1/CLKI/RPA2/RA2
9	D-	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMD2/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/CTED11/RB4
12	PGED4/PMD0/RA10	34	SOSCO/RPA4/T1CK/RA4
13	PGEC4/TCK/CTED8/PMD3/RA7	35	TDI/RPA9/PMD1/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15	37	RPC4/PMD4/RC4
16	AVSS	38	RPC5/PMD7/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA3/RA0	41	TMS/RPB5/USBID/RB5
20	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMA6/RA1	42	VBUS
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMA10/RB0	43	RPB7/CTED3/PMA5/INT0/RB7
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMA9/RB1	44	RPB8/SCL1/CTED10/PMA4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **12.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See **12.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: Shaded pins are 5V tolerant.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: http://www.microchip.com/pic32

- **Section 1. "Introduction"** (DS60001127)
- **Section 2. "CPU"** (DS60001113)
- **Section 3. "Memory Organization"** (DS60001115)
- **Section 4. "Prefetch Cache"** (DS60001119)
- **Section 5. "Flash Program Memory"** (DS60001121)
- **Section 6. "Oscillator Configuration"** (DS60001112)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog Timer and Power-up Timer"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (C_{VREF})"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)
- **Section 38. "High/Low Voltage Detect (HLVD)"** (*DS number pending*)

NOTES:

1.0 DEVICE OVERVIEW

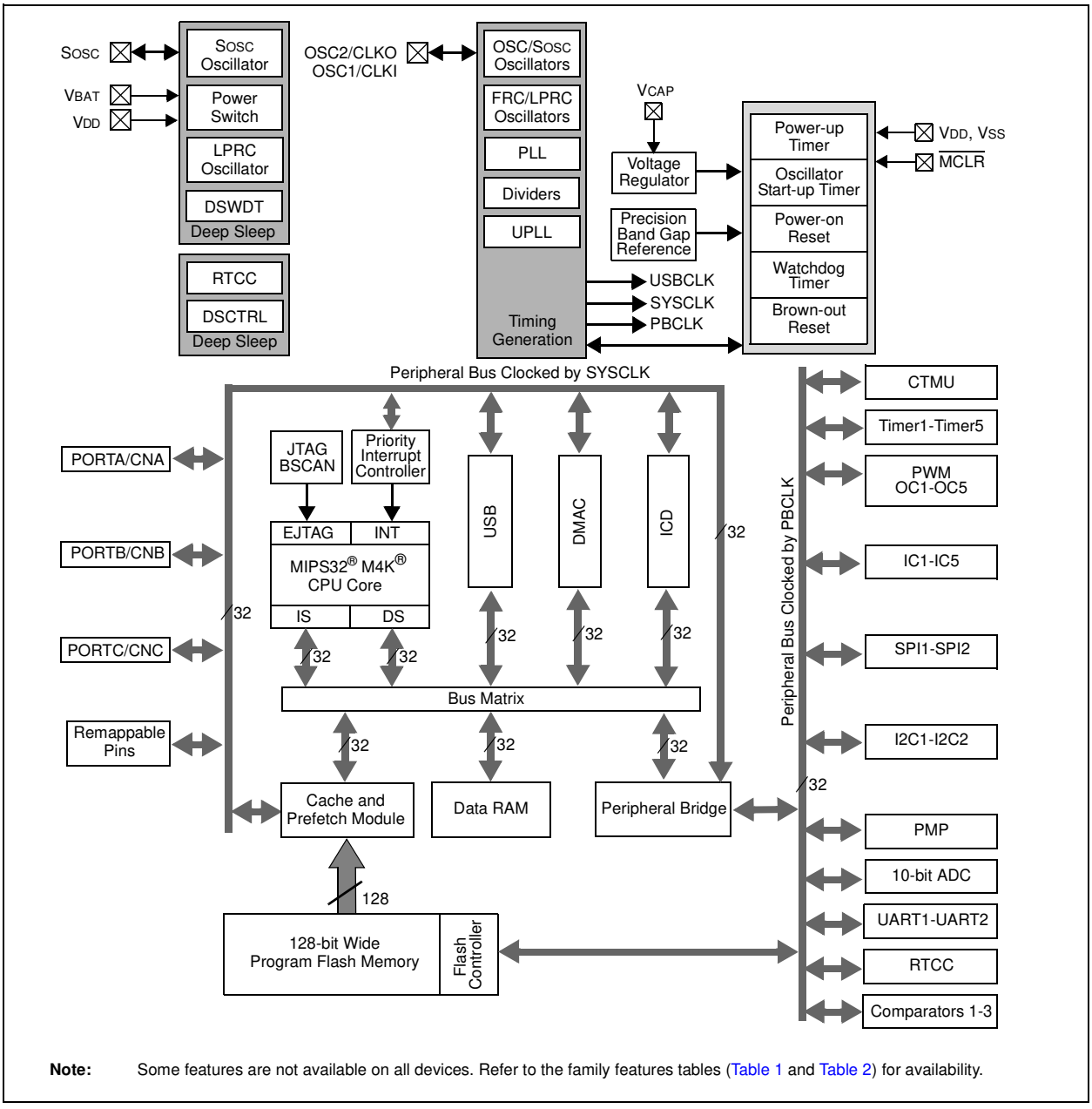
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX1XX/2XX 28/44-pin XLP Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/44-pin XLP Family of devices.

Table 1-1 through Table 1-16 list the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM



Note: Some features are not available on all devices. Refer to the family features tables (Table 1 and Table 2) for availability.

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number[1]			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Analog-to-Digital Converter						
AN0	27	2	19	I	Analog	Analog input channels.
AN1	28	3	20	I	Analog	
AN2	1	4	21	I	Analog	
AN3	2	5	22	I	Analog	
AN4	3	6	23	I	Analog	
AN5	4	7	24	I	Analog	
AN6	—	—	25	I	Analog	
AN7	—	—	26	I	Analog	
AN8	—	—	27	I	Analog	
AN9	23	26	15	I	Analog	
AN10	22	25	14	I	Analog	
AN11[3]	21	24	11	I	Analog	
AN12	20[2]	23[2]	10	I	Analog	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

2: Pin number for General Purpose devices only.

3: This pin is not available on VBAT devices.

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Oscillators						
CLKI	6	9	30	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	7	10	31	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	6	9	30	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	7	10	31	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	8	11	33	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	9	12	34	O	—	32.768 kHz low-power oscillator crystal output.
REFCLKI	PPS	PPS	PPS	I	ST	Reference Input Clock
REFCLKO	PPS	PPS	PPS	O	—	Reference Output Clock

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

TABLE 1-3: IC1 THROUGH IC5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Input Capture						
IC1	PPS	PPS	PPS	I	ST	Input Capture Input 1-5
IC2	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

TABLE 1-4: OC1 THROUGH OC5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Output Compare						
OC1	PPS	PPS	PPS	O	—	Output Compare Output 1-5
OC2	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
External Interrupts						
INT0	13	16	43	I	ST	External Interrupt 0-4
INT1	PPS	PPS	PPS	I	ST	
INT2	PPS	PPS	PPS	I	ST	
INT3	PPS	PPS	PPS	I	ST	
INT4	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

TABLE 1-6: PORTA THROUGH PORTC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
PORT A						
RA0	27	2	19	I/O	ST	PORTA is a bidirectional I/O port
RA1	28	3	20	I/O	ST	
RA2	6	9	30	I/O	ST	
RA3	7	10	31	I/O	ST	
RA4	9	12	34	I/O	ST	
RA7	—	—	13	I/O	ST	
RA8	—	—	32	I/O	ST	
RA9	—	—	35	I/O	ST	
RA10	—	—	12	I/O	ST	
PORTB						
RB0	1	4	21	I/O	ST	PORTB is a bidirectional I/O port
RB1	2	5	22	I/O	ST	
RB2	3	6	23	I/O	ST	
RB3	4	7	24	I/O	ST	
RB4	8	11	33	I/O	ST	
RB5	11	14	41	I/O	ST	
RB6	12(2)	15(2)	42(4)	I/O	ST	
RB7	13	16	43	I/O	ST	
RB8	14	17	44	I/O	ST	
RB9	15	18	1	I/O	ST	
RB10	18(4)	21(4)	8(4)	I/O	ST	
RB11	19(4)	22(4)	9(4)	I/O	ST	
RB12	20(4)	23(4)	10(4)	I/O	ST	
RB13	21(3)	24(3)	11(3)	I/O	ST	
RB14	22	25	14	I/O	ST	
RB15	23	26	15	I/O	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

2: Pin number for General Purpose devices only.

3: This pin is not available for devices with VBAT.

4: This pin is not available for devices with USB.

TABLE 1-6: PORTA THROUGH PORTC PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
PORTC						
RC0	—	—	25	I/O	ST	PORTC is a bidirectional I/O port
RC1	—	—	26	I/O	ST	
RC2	—	—	27	I/O	ST	
RC3	—	—	36	I/O	ST	
RC4	—	—	37	I/O	ST	
RC5	—	—	38	I/O	ST	
RC6	—	—	2	I/O	ST	
RC7	—	—	3	I/O	ST	
RC8	—	—	4	I/O	ST	
RC9	—	—	5	I/O	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

2: Pin number for General Purpose devices only.

3: This pin is not available for devices with VBAT.

4: This pin is not available for devices with USB.

TABLE 1-7: TIMER1 THROUGH TIMER5 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Timer1 through Timer5						
T1CK	9	12	34	I	ST	Timer1-5 External Clock Input
T2CK	PPS	PPS	PPS	I	ST	
T3CK	PPS	PPS	PPS	I	ST	
T4CK	PPS	PPS	PPS	I	ST	
T5CK	PPS	PPS	PPS	I	ST	
Real-Time Clock and Calendar						
RTCC	4	7	24	O	ST	Real-Time Clock Alarm Output

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.

TABLE 1-8: UART1 AND UART2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			
Universal Asynchronous Receiver Transmitter 2						
$\overline{U1CTS}$	PPS	PPS	PPS	I	ST	UART1 Clear to Send
$\overline{U1RTS}$	PPS	PPS	PPS	O	—	UART1 Ready to Send
U1RX	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	O	—	UART1 Transmit
Universal Asynchronous Receiver Transmitter 2						
$\overline{U2CTS}$	PPS	PPS	PPS	I	ST	UART2 Clear to Send
$\overline{U2RTS}$	PPS	PPS	PPS	O	—	UART2 Ready to Send
U2RX	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	O	—	UART2 Transmit

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the "**Pin Diagrams**" section for device pin availability.