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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM)
with Audio/Graphics/Touch (HMI), USB, and Advanced Analog**

Operating Conditions: 2.3V to 3.6V

- -40°C to +105°C (DC to 80 MHz)
- -40°C to +85°C (DC to 100 MHz)
- 0°C to +70°C (DC to 120 MHz)

Core: 120 MHz/150 DMIPS MIPS32® M4K®

- MIPS16e® mode for up to 40% smaller code size
- Code-efficient (C and Assembly) architecture
- Single-cycle (MAC) 32x16 and two-cycle 32x32 multiply

Clock Management

- 0.9% internal oscillator
- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Fast wake-up and start-up

Power Management

- Low-power management modes (Sleep and Idle)
- Integrated Power-on Reset, Brown-out Reset, and High Voltage Detect
- 0.5 mA/MHz dynamic current (typical)
- 50 µA IPD current (typical)

Audio/Graphics/Touch HMI Features

- External graphics interface with up to 34 PMP pins
- Audio data communication: I²S, LJ, RJ, USB
- Audio data control interface: SPI and I²C
- Audio data master clock:
 - Generation of fractional clock frequencies
 - Can be synchronized with USB clock
 - Can be tuned in run-time
- Charge Time Measurement Unit (CTMU):
 - Supports mTouch™ capacitive touch sensing
 - Provides high-resolution time measurement (1 ns)

Advanced Analog Features

- ADC Module:
 - 10-bit 1 Msps rate with one Sample and Hold (S&H)
 - Up to 28 analog inputs
 - Can operate during Sleep mode
- Flexible and independent ADC trigger sources
- On-chip temperature measurement capability
- Comparators:
 - Two dual-input Comparator modules
 - Programmable references with 32 voltage points

Packages

Type	QFN		TQFP		VTLA
Pin Count	64	64	100	100	124
I/O Pins (up to)	53	53	85	85	85
Contact/Lead Pitch	0.50	0.50	0.40	0.50	0.50
Dimensions	9x9x0.9	10x10x1	12x12x1	14x14x1	9x9x0.9

Note: All dimensions are in millimeters (mm) unless specified.

Timers/Output Compare/Input Capture

- Five General Purpose Timers:
 - Five 16-bit and up to two 32-bit Timers/Counters
- Five Output Compare (OC) modules
- Five Input Capture (IC) modules
- Peripheral Pin Select (PPS) to allow function remap
- Real-Time Clock and Calendar (RTCC) module

Communication Interfaces

- USB 2.0-compliant Full-speed OTG controller
- Up to five UART modules (20 Mbps):
 - LIN 2.1 protocols and IrDA® support
- Two 4-wire SPI modules (25 Mbps)
- Two I²C modules (up to 1 Mbaud) with SMBus support
- PPS to allow function remap
- Parallel Master Port (PMP)

Direct Memory Access (DMA)

- Four channels of hardware DMA with automatic data size detection
- 32-bit Programmable Cyclic Redundancy Check (CRC)
- Two additional channels dedicated to USB

Input/Output

- 15 mA or 12 mA source/sink for standard VOH/VOL and up to 22 mA for non-standard VOH1
- 5V-tolerant pins
- Selectable open drain, pull-ups, and pull-downs
- External interrupts on all I/O pins

Qualification and Class B Support

- AEC-Q100 REVH (Grade 2 -40°C to +105°C) planned
- Class B Safety Library, IEC 60730

Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited program and six complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan

PIC32MX330/350/370/430/450/470

TABLE 1: PIC32MX330/350/370/430/450/470 CONTROLLER FAMILY FEATURES

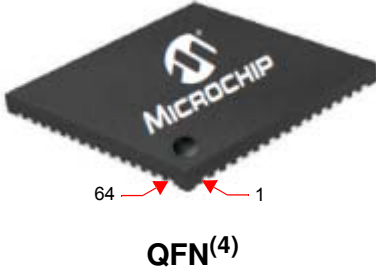
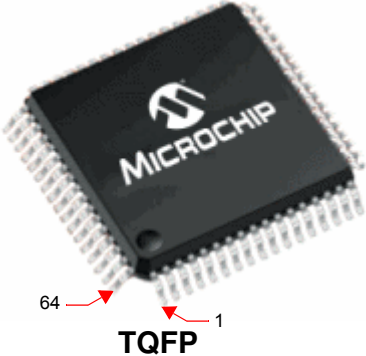
Device	Pins	Packages	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Peripherals					10-bit 1 Msps ADC (Channels)	Analog Comparators	USB On-The-Go (OTG)	CTMU	I ² C	PMP	RTCC	DMA Channels (Programmable/Dedicated)	I/O Pins	JTAG	Trace
					Remappable Pins	Timers/Capture/Compare ⁽²⁾	UART	SPI/I ² S	External Interrupts ⁽³⁾											
PIC32MX330F064H	64	QFN, TQFP	64+12	16	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX330F064L	100	TQFP	64+12	16	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
	124	VTLA																		
PIC32MX350F128H	64	QFN, TQFP	128+12	32	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX350F128L	100	TQFP	128+12	32	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
	124	VTLA																		
PIC32MX350F256H	64	QFN, TQFP	256+12	64	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX350F256L	100	TQFP	256+12	64	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
	124	VTLA																		
PIC32MX370F512H	64	QFN, TQFP	512+12	128	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX370F512L	100	TQFP	512+12	128	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
	124	VTLA																		
PIC32MX430F064H	64	QFN, TQFP	64+12	16	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX430F064L	100	TQFP	64+12	16	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
	124	VTLA																		
PIC32MX450F128H	64	QFN, TQFP	128+12	32	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX450F128HB (see Note 4)	64	QFN, TQFP	128+12	32	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX450F128L	100	TQFP	128+12	32	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
	124	VTLA																		
PIC32MX450F256H	64	QFN, TQFP	256+12	64	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX450F256L	100	TQFP	256+12	64	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
	124	VTLA																		
PIC32MX470F512H	64	QFN, TQFP	512+12	128	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX470F512L	100	TQFP	512+12	128	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
	124	VTLA																		
PIC32MX470F512LB (see Note 4)	100	TQFP	512+12	128	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
	124	VTLA																		

- Note 1:** All devices feature 12 KB of Boot Flash memory.
Note 2: Four out of five timers are remappable.
Note 3: Four out of five external interrupts are remappable.
Note 4: This PIC32 device is targeted to specific audio software packages that are tracked for licensing royalty purposes. All peripherals and electrical characteristics are identical to their corresponding base part numbers

PIC32MX330/350/370/430/450/470

Device Pin Tables

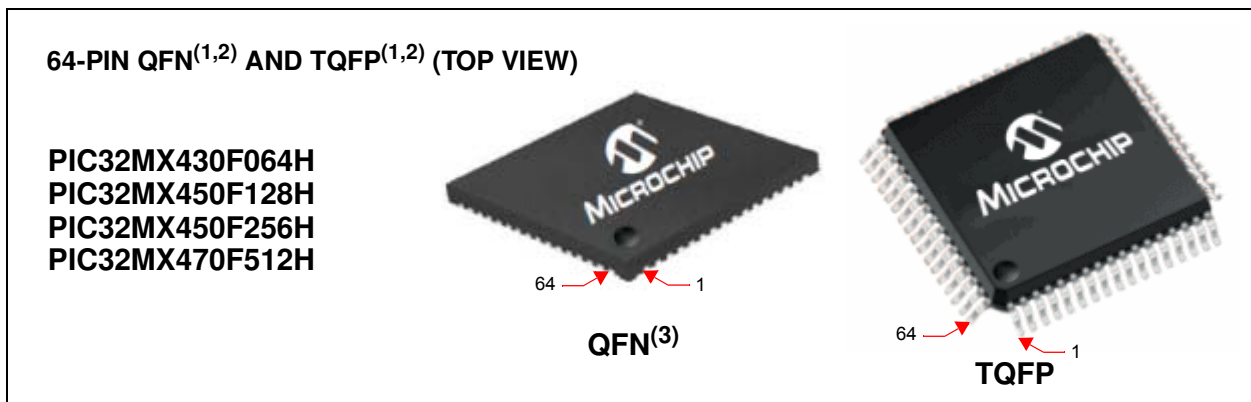
TABLE 2: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN ^(1,2,3,4) AND TQFP ^(1,2,3,4) (TOP VIEW)			
<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>PIC32MX330F064H PIC32MX350F128H PIC32MX350F256H PIC32MX370F512H</p>  <p>QFN(4)</p> </div> <div style="text-align: center;">  <p>TQFP</p> </div> </div>			
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	RPF3/RF3
2	AN23/PMD6/RE6	34	RPF2/RF2
3	AN27/PMD7/RE7	35	RPF6/SCK1/INT0/RF6
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	SDA1/RG3
5	AN17/C1INC/RPG7/PMA4/RG7	37	SCL1/RG2
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/RB5	43	RPD9/RD9
12	AN4/C1INB/RB4	44	RPD10/PMCS2/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMCS1/RD11
14	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	46	RPD0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3/RB7	50	AN25/RPD2/RD2
19	AVDD	51	AN26/RPD3/RD3
20	AVSS	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10/RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	55	RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 "Peripheral Pin Select"](#) for restrictions.
 - 2: Every I/O port pin (RBx-RGx), with the exception of RF6, can be used as a change notification pin (CNBx-CNGx). See [Section 12.0 "I/O Ports"](#) for more information.
 - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: RPF6 (pin 35) is only available for output functions.

PIC32MX330/350/370/430/450/470

TABLE 3: PIN NAMES FOR 64-PIN DEVICES



Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	USBID/RF3
2	AN23/PMD6/RE6	34	VBUS
3	AN27/PMD7/RE7	35	VUSB3V3
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN17/C1INC/RPG7/PMA4/RG7	37	D+
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	Vss	41	Vss
10	VDD	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/VBUSON/RB5	43	RPD9/SDA1/RD9
12	AN4/C1INB/RB4	44	RPD10/SCL1/PMCS2/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMCS1/RD11
14	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	46	RPD0/INT0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3//RB7	50	AN25/RPD2/SCK1/RD2
19	AVDD	51	AN26/RPD3/RD3
20	AVss	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10//RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11//PMA13/RB10	55	RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	Vss	57	VDD
26	VDD	58	RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

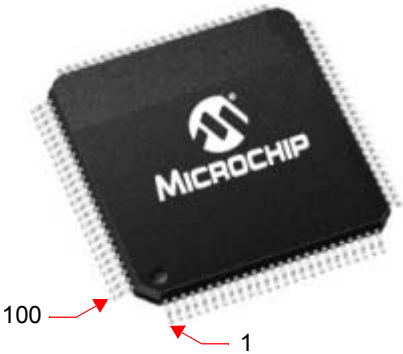
- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
 - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See [Section 12.0 “I/O Ports”](#) for more information.
 - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

PIC32MX330/350/370/430/450/470

TABLE 4: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)^(1,2,3)

PIC32MX330F064L
PIC32MX350F128L
PIC32MX350F256L
PIC32MX370F512L



Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	Vss
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	RPF13/RF13
5	AN27/PMD7/RE7	40	RPF12/RF12
6	RPC1/RC1	41	AN12/PMA11/RB12
7	RPC2/RC2	42	AN13/PMA10/RB13
8	RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	Vss
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	RPD14/RD14
13	MCLR	48	RPD15/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	Vss	50	RPF5/PMA8/RF5
16	VDD	51	RPF3/RF3
17	TMS/CTED1/RA0	52	RPF2/RF2
18	RPE8/RE8	53	RPF8/RF8
19	RPE9/RE9	54	RPF7/RF7
20	AN5/C1INA/RPB5/RB5	55	RPF6/SCK1/INT0/RF6
21	AN4/C1INB/RB4	56	SDA1/RG3
22	PGED3/AN3/C2INA/RPB3/RB3	57	SCL1/RG2
23	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	Vss
31	AVSS	66	RPA14/RA14
32	AN8/RPB8/CTED10/RB8	67	RPA15/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/PMCS2/RD10

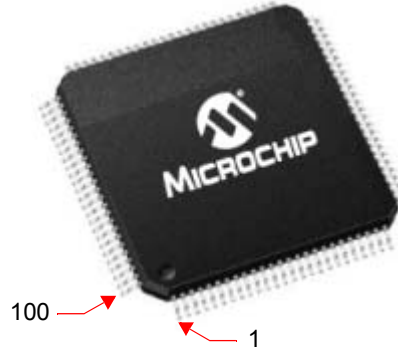
- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
 - 2: Every I/O port pin (RAX-RGX), with the exception of RF6, can be used as a change notification pin (CNAX-CNGX). See [Section 12.0 “I/O Ports”](#) for more information.
 - 3: RPF6 (pin 55) and RPF7 (pin 54) are only remappable for input functions.

PIC32MX330/350/370/430/450/470

TABLE 4: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)^(1,2,3)

PIC32MX330F064L
 PIC32MX350F128L
 PIC32MX350F256L
 PIC32MX370F512L

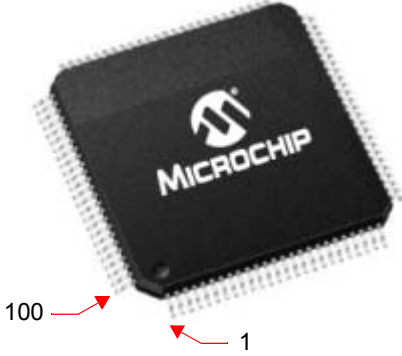


Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMCS1/RD11	86	VDD
72	RPD0/RD0	87	RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	Vss	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	TRCLK/RA6
77	AN25/RPD2/RD2	92	TRD3/CTED8/RA7
78	AN26/RPD3/RD3	93	PMD0/RE0
79	RPD12/PMD12/RD12	94	PMD1/RE1
80	PMD13/RD13	95	TRD2/RG14
81	RPD4/PMWR/RD4	96	TRD1/RG12
82	RPD5/PMRD/RD5	97	TRD0/RG13
83	PMD14/RD6	98	AN20/PMD2/RE2
84	PMD15/RD7	99	RPE3/CTPLS/PMD3/RE3
85	VCAP	100	AN21/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
 - 2: Every I/O port pin (RAX-RGX), with the exception of RF6, can be used as a change notification pin (CNAX-CNGX). See [Section 12.0 “I/O Ports”](#) for more information.
 - 3: RPF6 (pin 55) and RPF7 (pin 54) are only remappable for input functions.

PIC32MX330/350/370/430/450/470

TABLE 5: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW) ^(1,2)			
<p>PIC32MX430F064L PIC32MX450F128L PIC32MX450F256L PIC32MX470F512L</p> 			
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	Vss
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	RPF13/RF13
5	AN27/PMD7/RE7	40	RPF12/RF12
6	RPC1/RC1	41	AN12/PMA11/RB12
7	RPC2/RC2	42	AN13/PMA10/RB13
8	RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	Vss
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	RPD14/RD14
13	MCLR	48	RPD15/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	Vss	50	RPF5/PMA8/RF5
16	VDD	51	USBID/RF3
17	TMS/CTED1/RA0	52	RPF2/RF2
18	RPE8/RE8	53	RPF8/RF8
19	RPE9/RE9	54	VBUS
20	AN5/C1INA/RPB5/VBUSON/RB5	55	VUSB3v3
21	AN4/C1INB/RB4	56	D-
22	PGED3/AN3/C2INA/RPB3/RB3	57	D+
23	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	Vss
31	AVss	66	SCL1/RPA14/RA14
32	AN8/RPB8/CTED10/RB8	67	SDA1/RPA15/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/SCK1/PMCS2/RD10

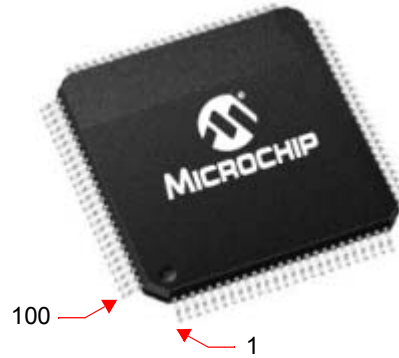
- Note** 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
- 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See [Section 12.0 “I/O Ports”](#) for more information.

PIC32MX330/350/370/430/450/470

TABLE 5: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)^(1,2)

PIC32MX430F064L
 PIC32MX450F128L
 PIC32MX450F256L
 PIC32MX470F512L

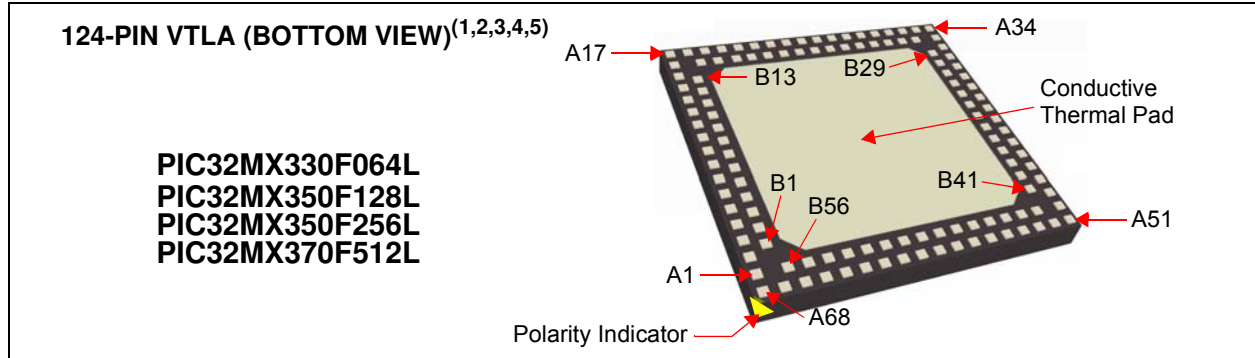


Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMCS1/RD11	86	VDD
72	RPD0/INT0/RD0	87	RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	VSS	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	TRCLK/RA6
77	AN25/RPD2/RD2	92	TRD3/CTED8/RA7
78	AN26/RPD3/RD3	93	PMD0/RE0
79	RPD12/PMD12/RD12	94	PMD1/RE1
80	PMD13/RD13	95	TRD2/RG14
81	RPD4/PMWR/RD4	96	TRD1/RG12
82	RPD5/PMRD/RD5	97	TRD0/RG13
83	PMD14/RD6	98	AN20/CTPLS/PMD2/RE2
84	PMD15/RD7	99	RPE3/PMD3/RE3
85	VCAP	100	AN21/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
 - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See [Section 12.0 “I/O Ports”](#) for more information.

PIC32MX330/350/370/430/450/470

TABLE 6: PIN NAMES FOR 124-PIN DEVICES

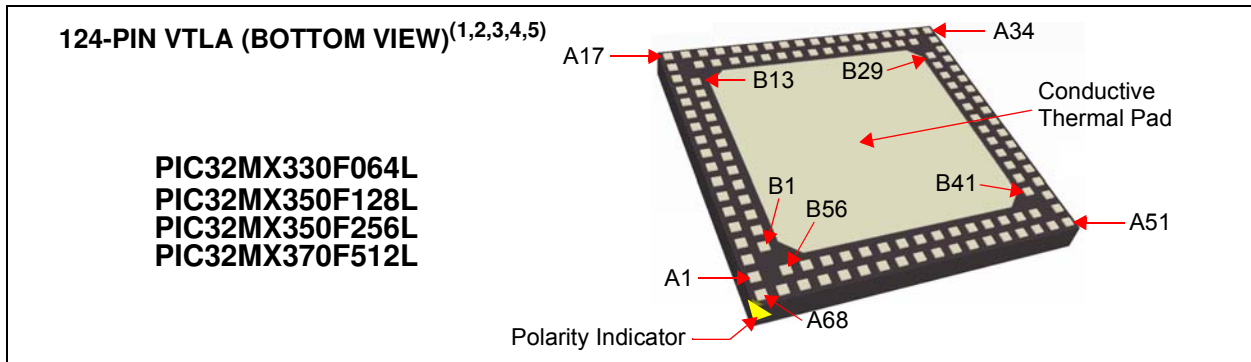


Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
A1	No Connect	A38	SDA1/RG3
A2	RG15	A39	SCL2/RA2
A3	Vss	A40	TDI/CTED9/RA4
A4	AN23/PMD6/RE6	A41	VDD
A5	RPC1/RC1	A42	OSC2/CLKO/RC15
A6	RPC3/RC3	A43	Vss
A7	AN16/C1IND/RPG6/SCK2/PMA5/RG6	A44	RPA15/RA15
A8	AN18/C2IND/RPG8/PMA3/RG8	A45	RPD9/RD9
A9	AN19/C2INC/RPG9/PMA2/RG9	A46	RPD11/PMCS1/RD11
A10	VDD	A47	SOSCI/IPC13/RC13
A11	RPE8/RE8	A48	VDD
A12	AN5/C1INA/RPB5/RB5	A49	No Connect
A13	PGED3/AN3/C2INA/RPB3/RB3	A50	No Connect
A14	VDD	A51	No Connect
A15	PGEC1/AN1/RPB1/CTED12/RB1	A52	AN24/RPD1/RD1
A16	No Connect	A53	AN26/RPD3/RD3
A17	No Connect	A54	PMD13/RD13
A18	No Connect	A55	RPD5/PMRD/RD5
A19	No Connect	A56	PMD15/RD7
A20	PGEC2/AN6/RPB6/RB6	A57	No Connect
A21	VREF-/CVREF-/PMA7/RA9	A58	No Connect
A22	AVDD	A59	VDD
A23	AN8/RPB8/CTED10/RB8	A60	RPF1/PMD10/RF1
A24	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	A61	RPG0/PMD8/RG0
A25	Vss	A62	TRD3/CTED8/RA7
A26	TCK/CTED2/RA1	A63	Vss
A27	RPF12/RF12	A64	PMD1/RE1
A28	AN13/PMA10/RB13	A65	TRD1/RG12
A29	AN15/RPB15/OCFB/CTED6/PMA0/RB15	A66	AN20/PMD2/RE2
A30	VDD	A67	AN21/PMD4/RE4
A31	RPD15/RD15	A68	No Connect
A32	RPF5/PMA8/RF5	B1	VDD
A33	No Connect	B2	AN22/RPE5/PMD5/RE5
A34	No Connect	B3	AN27/PMD7/RE7
A35	RPF3/RF3	B4	RPC2/RC2
A36	RPF2/RF2	B5	RPC4/CTED7/RC4
A37	RPF7/RF7	B6	AN17/C1INC/RPG7/PMA4/RG7

- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
 - 2: Every I/O port pin (RAX-RGx), with the exception of RF6, can be used as a change notification pin (CNAX-CNGx). See [Section 12.0 “I/O Ports”](#) for more information.
 - 3: RPF6 (bump B30) and RPF7 (bump A37) are only remappable for input functions.
 - 4: Shaded package bumps are 5V tolerant.
 - 5: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

PIC32MX330/350/370/430/450/470

TABLE 6: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)



Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
B7	MCLR	B32	SDA2/RA3
B8	Vss	B33	TDO/RA5
B9	TMS/CTED1/RA0	B34	OSC1/CLKI/RC12
B10	RPE9/RE9	B35	No Connect
B11	AN4/C1INB/RB4	B36	RPA14/RA14
B12	Vss	B37	RPD8/RTCC/RD8
B13	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	B38	RPD10/PMCS2/RD10
B14	PGED1/AN0/RPB0/RB0	B39	RPD0/RD0
B15	No Connect	B40	SOSCO/RPC14/T1CK/RC14
B16	PGED2/AN7/RPB7/CTED3/RB7	B41	Vss
B17	VREF+/CVREF+/PMA6/RA10	B42	AN25/RPD2/RD2
B18	AVss	B43	RPD12/PMD12/RD12
B19	AN9/RPB9/CTED4/RB9	B44	RPD4/PMWR/RD4
B20	AN11/PMA12/RB11	B45	PMD14/RD6
B21	VDD	B46	No Connect
B22	RPF13/RF13	B47	No Connect
B23	AN12/PMA11/RB12	B48	VCAP
B24	AN14/RPB14/CTED5/PMA1/RB14	B49	RPF0/PMD11/RF0
B25	Vss	B50	RPG1/PMD9/RG1
B26	RPD14/RD14	B51	TRCLK/RA6
B27	RPF4/PMA9/RF4	B52	PMD0/RE0
B28	No Connect	B53	VDD
B29	RPF8/RF8	B54	TRD2/RG14
B30	RPF6/SCKI/INT0/RF6	B55	TRD0/RG13
B31	SCL1/RG2	B56	RPE3/CTPLS/PMD3/RE3

- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
 - 2: Every I/O port pin (RAX-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See [Section 12.0 “I/O Ports”](#) for more information.
 - 3: RPF6 (bump B30) and RPF7 (bump A37) are only remappable for input functions.
 - 4: Shaded package bumps are 5V tolerant.
 - 5: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

PIC32MX330/350/370/430/450/470

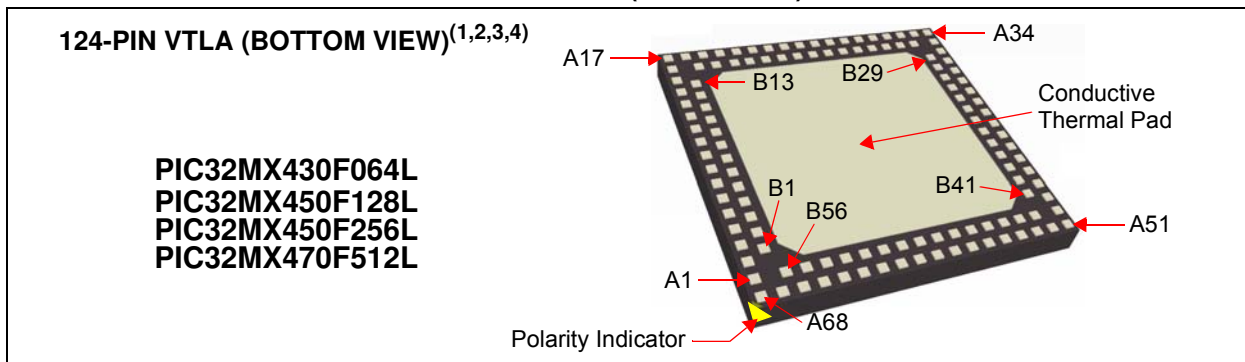
TABLE 7: PIN NAMES FOR 124-PIN DEVICES

Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
A1	No Connect	A38	D-
A2	RG15	A39	SCL2/RA2
A3	Vss	A40	TDI/CTED9/RA4
A4	AN23/PMD6/RE6	A41	Vdd
A5	RPC1/RC1	A42	OSC2/CLKO/RC15
A6	RPC3/RC3	A43	Vss
A7	AN16/C1IND/RPG6/SCK2/PMA5/RG6	A44	SDA1/RPA15/RA15
A8	AN18/C2IND/RPG8/PMA3/RG8	A45	RPD9/RD9
A9	AN19/C2INC/RPG9/PMA2/RG9	A46	RPD11/PMCS1/RD11
A10	Vdd	A47	SOSCI/IPC13/RC13
A11	RPE8/RE8	A48	Vdd
A12	AN5/C1INA/RPB5/VBUSON/RB5	A49	No Connect
A13	PGED3/AN3/C2INA/RPB3/RB3	A50	No Connect
A14	Vdd	A51	No Connect
A15	PGEC1/AN1/RPB1/CTED12/RB1	A52	AN24/RPD1/RD1
A16	No Connect	A53	AN26/RPD3/RD3
A17	No Connect	A54	PMD13/RD13
A18	No Connect	A55	RPD5/PMRD/RD5
A19	No Connect	A56	PMD15/RD7
A20	PGEC2/AN6/RPB6/RB6	A57	No Connect
A21	VREF-/CVREF-/PMA7/RA9	A58	No Connect
A22	AVdd	A59	Vdd
A23	AN8/RPB8/CTED10/RB8	A60	RPF1/PMD10/RF1
A24	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	A61	RPG0/PMD8/RG0
A25	Vss	A62	TRD3/CTED8/RA7
A26	TCK/CTED2/RA1	A63	Vss
A27	RPF12/RF12	A64	PMD1/RE1
A28	AN13/PMA10/RB13	A65	TRD1/RG12
A29	AN15/RPB15/OCFB/CTED6/PMA0/RB15	A66	AN20/PMD2/RE2
A30	Vdd	A67	AN21/PMD4/RE4
A31	RPD15/RD15	A68	No Connect
A32	RPF5/PMA8/RF5	B1	VDD
A33	No Connect	B2	AN22/RPE5/PMD5/RE5
A34	No Connect	B3	AN27/PMD7/RE7
A35	USBID/RF3	B4	RPC2/RC2
A36	RPF2/RF2	B5	RPC4/CTED7/RC4
A37	Vbus	B6	AN17/C1INC/RPG7/PMA4/RG7

- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 "Peripheral Pin Select"](#) for restrictions.
 - 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAX-CNGx). See [Section 12.0 "I/O Ports"](#) for more information.
 - 3: Shaded package bumps are 5V tolerant.
 - 4: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

PIC32MX330/350/370/430/450/470

TABLE 7: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)



Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
B7	MCLR	B32	SDA2/RA3
B8	Vss	B33	TDO/RA5
B9	TMS/CTED1/RA0	B34	OSC1/CLKI/RC12
B10	RPE9/RE9	B35	No Connect
B11	AN4/C1INB/RB4	B36	SCL1/RPA14/RA14
B12	Vss	B37	RPD8/RTCC/RD8
B13	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	B38	RPD10/SCK1/PMCS2/RD10
B14	PGED1/AN0/RPB0/RB0	B39	RPD0/INT0/RD0
B15	No Connect	B40	SOSCO/RPC14/T1CK/RC14
B16	PGED2/AN7/RPB7/CTED3/RB7	B41	Vss
B17	VREF+/CVREF+/PMA6/RA10	B42	AN25/RPD2/RD2
B18	AVss	B43	RPD12/PMD12/RD12
B19	AN9/RPB9/CTED4/RB9	B44	RPD4/PMWR/RD4
B20	AN11/PMA12/RB11	B45	PMD14/RD6
B21	VDD	B46	No Connect
B22	RPF13/RF13	B47	No Connect
B23	AN12/PMA11/RB12	B48	VCAP
B24	AN14/RPB14/CTED5/PMA1/RB14	B49	RPF0/PMD11/RF0
B25	Vss	B50	RPG1/PMD9/RG1
B26	RPD14/RD14	B51	TRCLK/RA6
B27	RPF4/PMA9/RF4	B52	PMD0/RE0
B28	No Connect	B53	VDD
B29	RPF8/RF8	B54	TRD2/RG14
B30	VUSB3v3	B55	TRD0/RG13
B31	D+	B56	RPE3/CTPLS/PMD3/RE3

- Note**
- 1: The RPN pins can be used by remappable peripherals. See [Table 1](#) for the available peripherals and [Section 12.3 “Peripheral Pin Select”](#) for restrictions.
 - 2: Every I/O port pin (RAX-RGX) can be used as a change notification pin (CNAX-CNGX). See [Section 12.0 “I/O Ports”](#) for more information.
 - 3: Shaded package bumps are 5V tolerant.
 - 4: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

PIC32MX330/350/370/430/450/470

Table of Contents

1.0	Device Overview	17
2.0	Guidelines for Getting Started with 32-bit MCUs.....	27
3.0	CPU.....	35
4.0	Memory Organization.....	39
5.0	Flash Program Memory.....	53
6.0	Resets	59
7.0	Interrupt Controller	63
8.0	Oscillator Configuration	73
9.0	Prefetch Cache.....	83
10.0	Direct Memory Access (DMA) Controller	93
11.0	USB On-The-Go (OTG).....	113
12.0	I/O Ports	137
13.0	Timer1	167
14.0	Timer2/3, Timer4/5	171
15.0	Watchdog Timer (WDT)	177
16.0	Input Capture.....	181
17.0	Output Compare.....	185
18.0	Serial Peripheral Interface (SPI).....	189
19.0	Inter-Integrated Circuit (I ² C).....	197
20.0	Universal Asynchronous Receiver Transmitter (UART).....	205
21.0	Parallel Master Port (PMP).....	213
22.0	Real-Time Clock and Calendar (RTCC).....	223
23.0	10-bit Analog-to-Digital Converter (ADC).....	233
24.0	Comparator	243
25.0	Comparator Voltage Reference (CVREF)	247
26.0	Charge Time Measurement Unit (CTMU)	251
27.0	Power-Saving Features	257
28.0	Special Features	261
29.0	Instruction Set	273
30.0	Development Support.....	275
31.0	Electrical Characteristics	279
32.0	DC and AC Device Characteristics Graphs.....	329
33.0	Packaging Information.....	333
	The Microchip Web Site	359
	Customer Change Notification Service	359
	Customer Support.....	359
	Product Identification System	360

PIC32MX330/350/370/430/450/470

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Referenced Sources

This device data sheet is based on the following individual sections of the “PIC32 Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: <http://www.microchip.com/pic32>.

- **Section 1. “Introduction”** (DS60001127)
- **Section 2. “CPU”** (DS60001113)
- **Section 3. “Memory Organization”** (DS60001115)
- **Section 4. “Prefetch Cache”** (DS60001119)
- **Section 5. “Flash Program Memory”** (DS60001121)
- **Section 6. “Oscillator Configuration”** (DS60001112)
- **Section 7. “Resets”** (DS60001118)
- **Section 8. “Interrupt Controller”** (DS60001108)
- **Section 9. “Watchdog Timer and Power-up Timer”** (DS60001114)
- **Section 10. “Power-Saving Features”** (DS60001130)
- **Section 12. “I/O Ports”** (DS60001120)
- **Section 13. “Parallel Master Port (PMP)”** (DS60001128)
- **Section 14. “Timers”** (DS60001105)
- **Section 15. “Input Capture”** (DS60001122)
- **Section 16. “Output Compare”** (DS60001111)
- **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104)
- **Section 19. “Comparator”** (DS60001110)
- **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109)
- **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107)
- **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106)
- **Section 24. “Inter-Integrated Circuit (I²C)”** (DS60001116)
- **Section 27. “USB On-The-Go (OTG)”** (DS60001126)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125)
- **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117)
- **Section 32. “Configuration”** (DS60001124)
- **Section 33. “Programming and Diagnostics”** (DS60001129)
- **Section 37. “Charge Time Measurement Unit (CTMU)”** (DS60001167)

PIC32MX330/350/370/430/450/470

NOTES:

PIC32MX330/350/370/430/450/470

1.0 DEVICE OVERVIEW

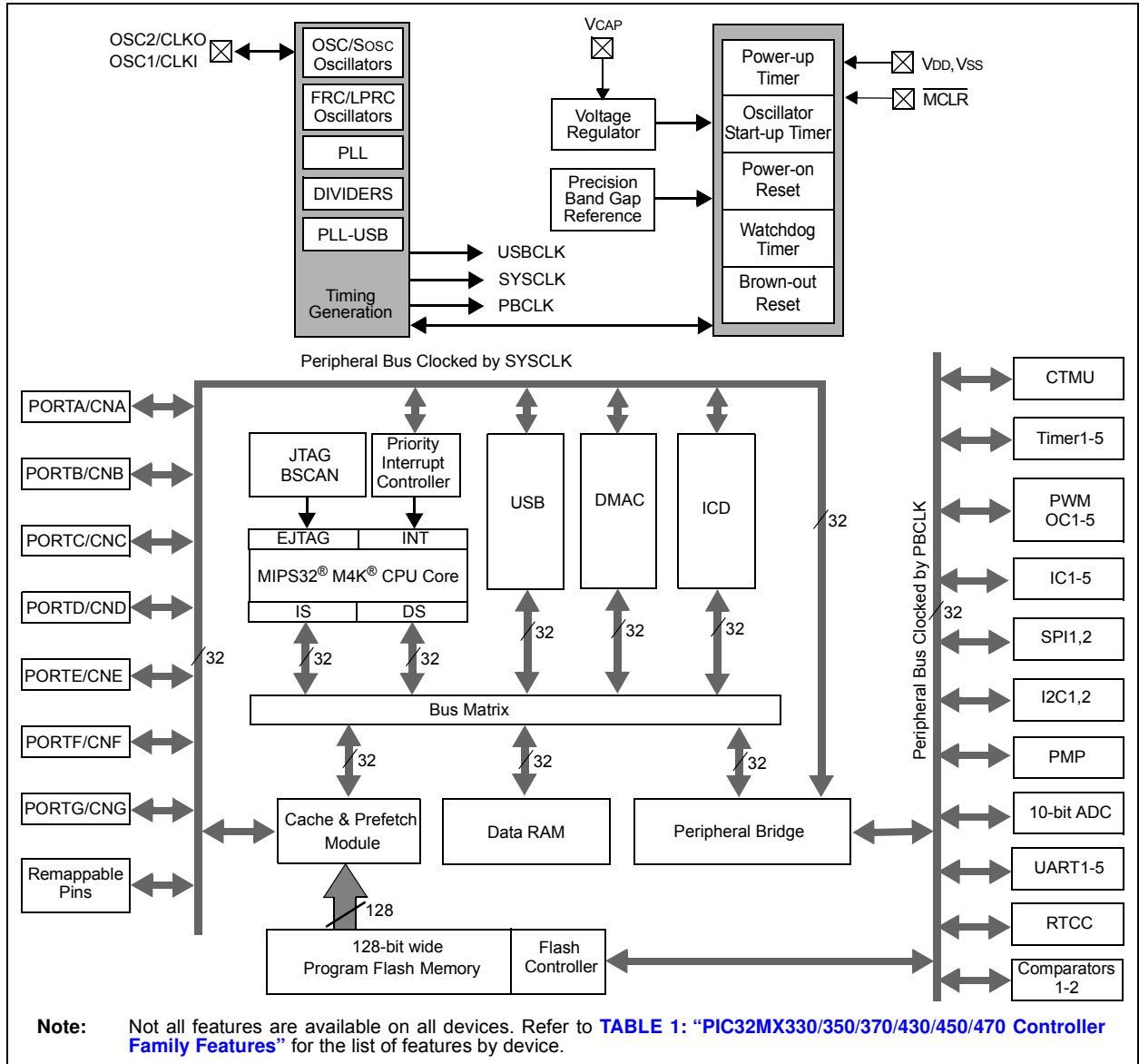
Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX330/350/370/430/450/470 devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX330/350/370/430/450/470 family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: PIC32MX330/350/370/430/450/470 BLOCK DIAGRAM



PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
AN0	16	25	B14	I	Analog	Analog input channels.
AN1	15	24	A15	I	Analog	
AN2	14	23	B13	I	Analog	
AN3	13	22	A13	I	Analog	
AN4	12	21	B11	I	Analog	
AN5	11	20	A12	I	Analog	
AN6	17	26	A20	I	Analog	
AN7	18	27	B16	I	Analog	
AN8	21	32	A23	I	Analog	
AN9	22	33	B19	I	Analog	
AN10	23	34	A24	I	Analog	
AN11	24	35	B20	I	Analog	
AN12	27	41	B23	I	Analog	
AN13	28	42	A28	I	Analog	
AN14	29	43	B24	I	Analog	
AN15	30	44	A29	I	Analog	
AN16	4	10	A7	I	Analog	
AN17	5	11	B6	I	Analog	
AN18	6	12	A8	I	Analog	
AN19	8	14	A9	I	Analog	
AN20	62	98	A66	I	Analog	
AN21	64	100	A67	I	Analog	
AN22	1	3	B2	I	Analog	
AN23	2	4	A4	I	Analog	
AN24	49	76	A52	I	Analog	
AN25	50	77	B42	I	Analog	
AN26	51	78	A53	I	Analog	
AN27	3	5	B3	I	Analog	
CLKI	39	63	B34	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	40	64	A42	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with the OSC2 pin function.
OSC1	39	63	B34	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	40	64	A42	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	73	A47	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	48	74	B40	O	—	32.768 kHz low-power oscillator crystal output.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 TTL = TTL input buffer

- Note 1:** This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices.

PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
IC1	PPS	PPS	PPS	I	ST	Capture Input 1-5
IC2	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	I	ST	
OC1	PPS	PPS	PPS	O	ST	Output Compare Output 1
OC2	PPS	PPS	PPS	O	ST	Output Compare Output 2
OC3	PPS	PPS	PPS	O	ST	Output Compare Output 3
OC4	PPS	PPS	PPS	O	ST	Output Compare Output 4
OC5	PPS	PPS	PPS	O	ST	Output Compare Output 5
OCFA	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	A29	I	ST	Output Compare Fault B Input
INT0	35 ⁽¹⁾ , 46 ⁽²⁾	55 ⁽¹⁾ , 72 ⁽²⁾	B30 ⁽¹⁾ , B39 ⁽²⁾	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	I	ST	External Interrupt 4
RA0	—	17	B9	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	A26	I/O	ST	
RA2	—	58	A39	I/O	ST	
RA3	—	59	B32	I/O	ST	
RA4	—	60	A40	I/O	ST	
RA5	—	61	B33	I/O	ST	
RA6	—	91	B51	I/O	ST	
RA7	—	92	A62	I/O	ST	
RA9	—	28	A21	I/O	ST	
RA10	—	29	B17	I/O	ST	
RA14	—	66	B36	I/O	ST	
RA15	—	67	A44	I/O	ST	

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PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
RB0	16	25	B14	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A15	I/O	ST	
RB2	14	23	B13	I/O	ST	
RB3	13	22	A13	I/O	ST	
RB4	12	21	B11	I/O	ST	
RB5	11	20	A12	I/O	ST	
RB6	17	26	A20	I/O	ST	
RB7	18	27	B16	I/O	ST	
RB8	21	32	A23	I/O	ST	
RB9	22	33	B19	I/O	ST	
RB10	23	34	A24	I/O	ST	
RB11	24	35	B20	I/O	ST	
RB12	27	41	B23	I/O	ST	
RB13	28	42	A28	I/O	ST	
RB14	29	43	B24	I/O	ST	
RB15	30	44	A29	I/O	ST	
RC1	—	6	A5	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	B4	I/O	ST	
RC3	—	8	A6	I/O	ST	
RC4	—	9	B5	I/O	ST	
RC12	39	63	B34	I/O	ST	
RC13	47	73	A47	I/O	ST	
RC14	48	74	B40	I/O	ST	
RC15	40	64	A42	I/O	ST	
RD0	46	72	B39	I/O	ST	PORTD is a bidirectional I/O port
RD1	49	76	A52	I/O	ST	
RD2	50	77	B42	I/O	ST	
RD3	51	78	A53	I/O	ST	
RD4	52	81	B44	I/O	ST	
RD5	53	82	A55	I/O	ST	
RD6	54	83	B45	I/O	ST	
RD7	55	84	A56	I/O	ST	
RD8	42	68	B37	I/O	ST	
RD9	43	69	A45	I/O	ST	
RD10	44	70	B38	I/O	ST	
RD11	45	71	A46	I/O	ST	
RD12	—	79	B43	I/O	ST	
RD13	—	80	A54	I/O	ST	
RD14	—	47	B26	I/O	ST	
RD15	—	48	A31	I/O	ST	

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PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
RE0	60	93	B52	I/O	ST	PORTE is a bidirectional I/O port
RE1	61	94	A64	I/O	ST	
RE2	62	98	A66	I/O	ST	
RE3	63	99	B56	I/O	ST	
RE4	64	100	A67	I/O	ST	
RE5	1	3	B2	I/O	ST	
RE6	2	4	A4	I/O	ST	
RE7	3	5	B3	I/O	ST	
RE8	—	18	A11	I/O	ST	
RE9	—	19	B10	I/O	ST	
RF0	58	87	B49	I/O	ST	PORTF is a bidirectional I/O port
RF1	59	88	A60	I/O	ST	
RF2	34 ⁽¹⁾	52	A36	I/O	ST	
RF3	33	51	A35	I/O	ST	
RF4	31	49	B27	I/O	ST	
RF5	32	50	A32	I/O	ST	
RF6	35 ⁽¹⁾	55 ⁽¹⁾	B30 ⁽¹⁾	I/O	ST	
RF7	—	54 ⁽¹⁾	A37 ⁽¹⁾	I/O	ST	
RF8	—	53	B29	I/O	ST	
RF12	—	40	A27	I/O	ST	
RF13	—	39	B22	I/O	ST	PORTG is a bidirectional I/O port
RG0	—	90	A61	I/O	ST	
RG1	—	89	B50	I/O	ST	
RG2	37 ⁽¹⁾	57 ⁽¹⁾	B31	I/O	ST	
RG3	36 ⁽¹⁾	56 ⁽¹⁾	A38	I/O	ST	
RG6	4	10	A7	I/O	ST	
RG7	5	11	B6	I/O	ST	
RG8	6	12	A8	I/O	ST	
RG9	8	14	A9	I/O	ST	
RG12	—	96	A65	I/O	ST	
RG13	—	97	B55	I/O	ST	
RG14	—	95	B54	I/O	ST	
RG15	—	1	A2	I/O	ST	
T1CK	48	74	B40	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	I	ST	Timer5 External Clock Input

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PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
$\overline{U1CTS}$	PPS	PPS	PPS	I	ST	UART1 Clear to Send
$\overline{U1RTS}$	PPS	PPS	PPS	O	—	UART1 Ready to Send
U1RX	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	O	—	UART1 Transmit
$\overline{U2CTS}$	PPS	PPS	PPS	I	ST	UART2 Clear to Send
$\overline{U2RTS}$	PPS	PPS	PPS	O	—	UART2 Ready to Send
U2RX	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	O	—	UART2 Transmit
$\overline{U3CTS}$	PPS	PPS	PPS	I	ST	UART3 Clear to Send
$\overline{U3RTS}$	PPS	PPS	PPS	O	—	UART3 Ready to Send
U3RX	PPS	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	PPS	O	—	UART3 Transmit
$\overline{U4CTS}$	PPS	PPS	PPS	I	ST	UART4 Clear to Send
$\overline{U4RTS}$	PPS	PPS	PPS	O	—	UART4 Ready to Send
U4RX	PPS	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	PPS	O	—	UART4 Transmit
$\overline{U5CTS}^{(3)}$	—	PPS	PPS	I	ST	UART5 Clear to Send
$\overline{U5RTS}^{(3)}$	—	PPS	PPS	O	—	UART5 Ready to Send
$U5RX^{(3)}$	—	PPS	PPS	I	ST	UART5 Receive
$U5TX^{(3)}$	—	PPS	PPS	O	—	UART5 Transmit
SCK1	35 ⁽¹⁾ , 50 ⁽²⁾	55 ⁽¹⁾ , 70 ⁽²⁾	B30 ⁽¹⁾ , B38 ⁽²⁾	I/O	ST	Synchronous Serial Clock Input/Output for SPI1
SDI1	PPS	PPS	PPS	O	—	SPI1 Data In
SDO1	PPS	PPS	PPS	I/O	ST	SPI1 Data Out
$\overline{SS1}$	PPS	PPS	PPS	I/O	—	SPI1 Slave Synchronization for Frame Pulse I/O
SCK2	4	10	A7	I/O	ST	Synchronous Serial Clock Input/Output for SPI2
SDI2	PPS	PPS	PPS	O	—	SPI2 Data In
SDO2	PPS	PPS	PPS	I/O	ST	SPI2 Data Out
$\overline{SS2}$	PPS	PPS	PPS	I/O	—	SPI2 Slave Synchronization for Frame Pulse I/O
SCL1	37 ⁽¹⁾ , 44 ⁽²⁾	57 ⁽¹⁾ , 66 ⁽²⁾	B31 ⁽¹⁾ , B36 ⁽²⁾	I/O	ST	Synchronous Serial Clock Input/Output for I2C1
SDA1	36 ⁽¹⁾ , 43 ⁽²⁾	56 ⁽¹⁾ , 67 ⁽²⁾	A38 ⁽¹⁾ , A44 ⁽²⁾	I/O	ST	Synchronous Serial Data Input/Output for I2C1
SCL2	32	58	A39	I/O	ST	Synchronous Serial Clock Input/Output for I2C2
SDA2	31	59	B32	I/O	ST	Synchronous Serial Data Input/Output for I2C2
TMS	23	17	B9	I	ST	JTAG Test Mode Select Pin
TCK	27	38	A26	I	ST	JTAG Test Clock Input Pin
TDI	28	60	A40	I	—	JTAG Test Clock Input Pin
TDO	24	61	B33	O	—	JTAG Test Clock Output Pin
RTCC	42	68	B37	O	—	Real-Time Clock Alarm Output

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PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
CVREF-	15	28	A21	I	Analog	Comparator Voltage Reference (Low)
CVREF+	16	29	B17	I	Analog	Comparator Voltage Reference (High)
CVREFOUT	23	34	A24	I	Analog	Comparator Voltage Reference (Output)
C1INA	11	20	A12	I	Analog	Comparator 1 Inputs
C1INB	12	21	B11	I	Analog	
C1INC	5	11	B6	I	Analog	
C1IND	4	10	A7	I	Analog	
C2INA	13	22	A13	I	Analog	Comparator 2 Inputs
C2INB	14	23	B13	I	Analog	
C2INC	8	14	A9	I	Analog	
C2IND	6	12	A8	I	Analog	
C1OUT	PPS	PPS	PPS	O	—	Comparator 1 Output
C2OUT	PPS	PPS	PPS	O	—	Comparator 2 Output
PMALL	30	44	A29	O	TTL/ST	Parallel Master Port Address Latch Enable Low Byte
PMALH	29	43	B24	O	TTL/ST	Parallel Master Port Address Latch Enable High Byte
PMA0	30	44	A29	O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	29	43	B24	O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA2	8	14	A9	O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA3	6	12	A8	O	TTL/ST	
PMA4	5	11	B6	O	TTL/ST	
PMA5	4	10	A7	O	TTL/ST	
PMA6	16	29	B17	O	TTL/ST	
PMA7	22	28	A21	O	TTL/ST	
PMA8	32	50	A32	O	TTL/ST	
PMA9	31	49	B27	O	TTL/ST	
PMA10	28	42	A28	O	TTL/ST	
PMA11	27	41	B23	O	TTL/ST	
PMA12	24	35	B20	O	TTL/ST	
PMA13	23	34	A24	O	TTL/ST	
PMA14	45	71	A46	O	TTL/ST	
PMA15	44	70	B38	O	TTL/ST	
PMCS1	45	71	A46	O	TTL/ST	
PMCS2	44	70	B38	O	TTL/ST	
PMD0	60	93	B52	I/O	TTL/ST	
PMD1	61	94	A64	I/O	TTL/ST	
PMD2	62	98	A66	I/O	TTL/ST	

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PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description	
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA				
PMD3	63	99	B56	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)	
PMD4	64	100	A67	I/O	TTL/ST		
PMD5	1	3	B2	I/O	TTL/ST		
PMD6	2	4	A4	I/O	TTL/ST		
PMD7	3	5	B3	I/O	TTL/ST		
PMD8	—	90	A61	I/O	TTL/ST		
PMD9	—	89	B50	I/O	TTL/ST		
PMD10	—	88	A60	I/O	TTL/ST		
PMD11	—	87	B49	I/O	TTL/ST		
PMD12	—	79	B43	I/O	TTL/ST		
PMD13	—	80	A54	I/O	TTL/ST		
PMD14	—	83	B45	I/O	TTL/ST		
PMD15	—	84	A56	I/O	TTL/ST		
PMRD	53	82	A55	O	—		Parallel Master Port Read Strobe
PMWR	52	81	B44	O	—		Parallel Master Port Write Strobe
VBus ⁽²⁾	34	54	A37	I	Analog	USB Bus Power Monitor	
VUSB3V3 ⁽²⁾	35	55	B30	P	—	USB internal transceiver supply. If the USB module is not used, this pin must be connected to VDD.	
VBUSON ⁽²⁾	11	20	A12	O	—	USB Host and OTG bus power control Output	
D+ ⁽²⁾	37	57	B31	I/O	Analog	USB D+	
D- ⁽²⁾	36	56	A38	I/O	Analog	USB D-	
USBID ⁽²⁾	33	51	A35	I	ST	USB OTG ID Detect	
PGED1	16	25	B14	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1	
PGEC1	15	24	A15	I	ST	Clock Input pin for Programming/Debugging Communication Channel 1	
PGED2	18	27	B16	I/O	ST	Data I/O Pin for Programming/Debugging Communication Channel 2	
PGEC2	17	26	A20	I	ST	Clock Input Pin for Programming/Debugging Communication Channel 2	
PGED3	13	22	A13	I/O	ST	Data I/O Pin for Programming/Debugging Communication Channel 3	
PGEC3	14	23	B13	I	ST	Clock Input Pin for Programming/Debugging Communication Channel 3	
TRCLK	—	91	B51	O	—	Trace clock	
TRD0	—	97	B55	O	—	Trace Data bit 0	
TRD1	—	96	A65	O	—	Trace Data bit 1	
TRD2	—	95	B54	O	—	Trace Data bit 2	
TRD3	—	92	A62	O	—	Trace Data bit 3	
CTED1	—	17	B9	I	ST	CTMU External Edge Input 1	
CTED2	—	38	A26	I	ST	CTMU External Edge Input 2	
CTED3	18	27	B16	I	ST	CTMU External Edge Input 3	

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PIC32MX330/350/370/430/450/470

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
CTED4	22	33	B19	I	ST	CTMU External Edge Input 4
CTED5	29	43	B24	I	ST	CTMU External Edge Input 5
CTED6	30	44	A29	I	ST	CTMU External Edge Input 6
CTED7	—	9	B5	I	ST	CTMU External Edge Input 7
CTED8	—	92	A62	I	ST	CTMU External Edge Input 8
CTED9	—	60	A40	I	ST	CTMU External Edge Input 9
CTED10	21	32	A23	I	ST	CTMU External Edge Input 10
CTED11	23	34	A24	I	ST	CTMU External Edge Input 11
CTED12	15	24	A15	I	ST	CTMU External Edge Input 12
CTED13	14	23	B13	I	ST	CTMU External Edge Input 13
MCLR	7	13	B7	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	A22	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	B18	P	P	Ground reference for analog modules
VDD	10, 26, 38, 57	2, 16, 37, 46, 62, 86	B1, A10, A14, B21, A30, A41, A48, A59, B53	P	—	Positive supply for peripheral logic and I/O pins
VCAP	56	85	B48	P	—	Capacitor for Internal Voltage Regulator
VSS	9, 25, 41	15, 36, 45, 65, 75	A3, B8, B12, A25, B25, A43, B41, A63	P	—	Ground reference for logic and I/O pins
VREF+	16	29	B17	I	Analog	Analog Voltage Reference (High) Input
VREF-	15	28	A21	I	Analog	Analog Voltage Reference (Low) Input

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