Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog

Operating Conditions

- 2.1V to 3.6V, -40ºC to +85ºC, DC to 252 MHz
- 2.1V to 3.6V, -40ºC to +125ºC, DC to 180 MHz

Core: 252 MHz (up to 415 DMIPS) M-Class

- 16 KB I-Cache, 4 KB D-Cache
- FPU for 32-bit and 64-bit floating point math
- MMU for optimum embedded OS execution
- microMIPS™ mode for up to 35% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating, and fractional math
  - IEEE 754-compliant
- Code-efficient (C and Assembly) architecture

Clock Management

- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timers (WDT) and Deadman Timer (DMT)
- Fast wake-up and start-up

Power Management

- Low-power modes (Sleep and Idle)
- Integrated Power-on Reset (POR) and Brown-out Reset (BOR)

Memory Interfaces

- 50 MHz External Bus Interface (EBI)
- 50 MHz Serial Quad Interface (SQI)

Audio and Graphics Interfaces

- Graphics interfaces: EBI or PMP
- Audio data communication: I^2S, LJ, and RJ
- Audio control interfaces: SPI and I^2C
- Audio master clock: Fractional clock frequencies with USB synchronization

High-Speed (HS) Communication Interfaces (with Dedicated DMA)

- USB 2.0-compliant Hi-Speed On-The-Go (OTG) controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface

Security Features

- Crypto Engine with RNG for data encryption/decryption and authentication (AES, 3DES, SHA, MD5, and HMAC)
- Advanced memory protection:
  - Peripheral and memory region access control

Direct Memory Access (DMA)

- Eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)

Advanced Analog Features

- 12-bit ADC module:
  - 18 Msps with up to six Sample and Hold (S&H) circuits (five dedicated and one shared)
  - Up to 48 analog inputs
  - Can operate during Sleep and Idle modes
  - Multiple trigger sources
  - Six Digital Comparators and six Digital Filters
- Two comparators with 32 programmable voltage references
- Temperature sensor with ±2ºC accuracy

Communication Interfaces

- Two CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
  - Supports up to LIN 2.1 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as an additional SPI module (50 MHz)
- Five I^2C modules (up to 1 Mbaud) with SMBus support
- Parallel Master Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

Timers/Output Compare/Input Capture

- Nine 16-bit or up to four 32-bit timers/counters
- Nine Output Compare (OC) modules
- Nine Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module

Input/Output

- 5V-tolerant pins with up to 32 mA source/sink
- Selectable open drain, pull-ups, pull-downs, and slew rate controls
- External interrupts on all I/O pins
- PPS to enable function remap

Qualification and Class B Support

- AEC-Q100 REVH (Grade 1 -40ºC to +125ºC)
- Class B Safety Library, IEC 60730 (planned)
- Back-up internal oscillator

Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Software and Tools Support

- C/C++ compiler with native DSP/fractional and FPU support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™, and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPENRTOS®, Micriμm® μC/OS™, and SEGGER embOS®

Packages

Type	QFN	TQFP			TFBGA(1)		VTLA	LQFP
Pin Count	64	64	100	144	100	144	124	144
I/O Pins (up to)	53	53	78	120	78	120	98	120
Contact/Lead Pitch	0.50 mm	0.50 mm	0.40 mm	0.50 mm	0.40 mm	0.65 mm	0.50 mm	0.50 mm	0.50 mm
Dimensions	9x9x0.9 mm	10x10x1 mm	12x12x1 mm	14x14x1 mm	16x16x1 mm	7x7x1.2 mm	7x7x1.2 mm	9x9x0.9 mm	20x20x1.40 mm

Note 1: Contact your local Microchip Sales Office for information on the availability of devices in the 100-pin and 144-pin TFBGA packages

TABLE 1: PIC32MZ EF FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals						Crypto	RNG	DMA Channels (Programmable/ Dedicated)	ADC (Channels)	Analog Comparators	USB 2.0 HS OTG	I^2C	PMP	EBI	SQI	RTCC	Ethernet	I/O Pins	JTAG	Trace
						Remappable Pins	Timers/ Capture/(1) Compare	UART	SPI/I^2S	External Interrupts(2)	CAN 2.0B															
PIC32MZ0512EFE064	512	128	64	TQFP, QFN	160	34	9/9/9	6	4	5	0	N	Y	8/12	24	2	Y	4	Y	N	Y	Y	Y	46	Y	Y
PIC32MZ0512EFF064											2	N	Y	8/16												
PIC32MZ0512EFK064											2	Y	Y	8/18												
PIC32MZ1024EFE064	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF064											2	N	Y	8/16												
PIC32MZ1024EFK064											2	Y	Y	8/18												
PIC32MZ0512EFE100	512	128	100	TQFP	160	51	9/9/9	6	6	5	0	N	Y	8/12	40	2	Y	5	Y	Y	Y	Y	Y	78	Y	Y
PIC32MZ0512EFF100											2	N	Y	8/16												
PIC32MZ0512EFK100											2	Y	Y	8/18												
PIC32MZ1024EFE100	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF100											2	N	Y	8/16												
PIC32MZ1024EFK100											2	Y	Y	8/18												
PIC32MZ0512EFE124	512	128	124	VTLA	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	Y	97	Y	Y
PIC32MZ0512EFF124											2	N	Y	8/16												
PIC32MZ0512EFK124											2	Y	Y	8/18												
PIC32MZ1024EFE124	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF124											2	N	Y	8/16												
PIC32MZ1024EFK124											2	Y	Y	8/18												
PIC32MZ0512EFE144	512	128	144	LQFP, TQFP	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	Y	120	Y	Y
PIC32MZ0512EFF144											2	N	Y	8/16												
PIC32MZ0512EFK144											2	Y	Y	8/18												
PIC32MZ1024EFE144	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF144											2	N	Y	8/16												
PIC32MZ1024EFK144											2	Y	Y	8/18												

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.
3: This device is available with a 252 MHz speed rating.

TABLE 1: PIC32MZ EF FAMILY FEATURES (CONTINUED)

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals						Crypto	RNG	DMA Channels (Programmable/ Dedicated)	ADC (Channels)	Analog Comparators	USB 2.0 HS OTG	I^2C	PMP	EBI	SQI	RTCC	Ethernet	I/O Pins	JTAG	Trace
						Remappable Pins	Timers/ Capture/(1) Compare	UART	SPI/I^2S	External Interrupts(2)	CAN 2.0B															
PIC32MZ1024EFG064	1024	512	64	TQFP, QFN	160	34	9/9/9	6	4	5	0	N	Y	8/12	24	2	Y	4	Y	N	Y	Y	Y	46	Y	Y
PIC32MZ1024EFH064											2	N	Y	8/16												
PIC32MZ1024EFM064											2	Y	Y	8/18												
PIC32MZ2048EFG064	2048										0	N	Y	8/12												
PIC32MZ2048EFH064(3)											2	N	Y	8/16												
PIC32MZ2048EFM064											2	Y	Y	8/18												
PIC32MZ1024EFG100	1024	512	100	TQFP	160	51	9/9/9	6	6	5	0	N	Y	8/12	40	2	Y	5	Y	Y	Y	Y	Y	78	Y	Y
PIC32MZ1024EFH100											2	N	Y	8/16												
PIC32MZ1024EFM100											2	Y	Y	8/18												
PIC32MZ2048EFG100	2048										0	N	Y	8/12												
PIC32MZ2048EFH100(3)											2	N	Y	8/16												
PIC32MZ2048EFM100											2	Y	Y	8/18												
PIC32MZ1024EFG124	1024	512	124	VTLA	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	Y	97	Y	Y
PIC32MZ1024EFH124											2	N	Y	8/16												
PIC32MZ1024EFM124											2	Y	Y	8/18												
PIC32MZ2048EFG124	2048										0	N	Y	8/12												
PIC32MZ2048EFH124											2	N	Y	8/16												
PIC32MZ2048EFM124											2	Y	Y	8/18												
PIC32MZ1024EFG144	1024	512	144	LQFP, TQFP	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	Y	120	Y	Y
PIC32MZ1024EFH144											2	N	Y	8/16												
PIC32MZ1024EFM144											2	Y	Y	8/18												
PIC32MZ2048EFG144	2048										0	N	Y	8/12												
PIC32MZ2048EFH144(3)											2	N	Y	8/16												
PIC32MZ2048EFM144											2	Y	Y	8/18												

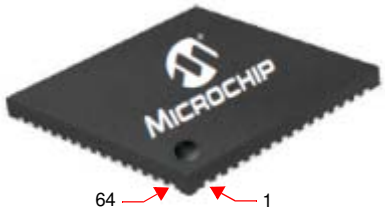
Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.
3: This device is available with a 252 MHz speed rating.

Device Pin Tables

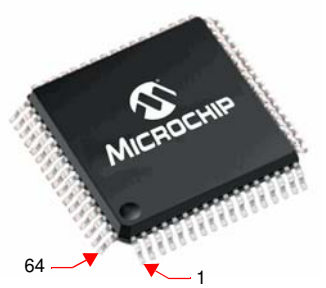
TABLE 2: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN(4) AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)064
PIC32MZ1024EF(G/H/M)064
PIC32MZ1024EF(E/F/K)064
PIC32MZ2048EF(G/H/M)064



QFN(4)



TQFP

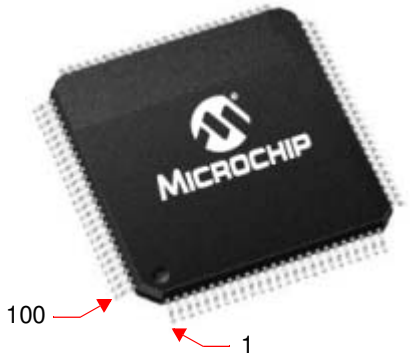
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN17/ETXEN/RPE5/PMD5/RE5	33	VBUS
2	AN16/ETXD0/PMD6/RE6	34	VUSB3V3
3	AN15/ETXD1/PMD7/RE7	35	VSS
4	AN14/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN13/C1INC/RPG7/SDA4/PMA4/RG7	37	D+
6	AN12/C2IND/RPG8/SCL4/PMA3/RG8	38	RPF3/USBID/RF3
7	VSS	39	VDD
8	VDD	40	VSS
9	MCLR	41	RPF4/SDA5/PMA9/RF4
10	AN11/C2INC/RPG9/PMA2/RG9	42	RPF5/SCL5/PMA8/RF5
11	AN45/C1INA/RPB5/RB5	43	AERXD0/ETXD2/RPD9/SDA1/PMCS2/PMA15/RD9
12	AN4/C1INB/RB4	44	ECOL/RPD10/SCL1/SCK4/RD10
13	AN3/C2INA/RPB3/RB3	45	AERXCLK/AEREFCLK/ECRS/RPD11/PMCS1/PMA14/RD11
14	AN2/C2INB/RPB2/RB2	46	AERXD1/ETXD3/RPD0/RTCC/INT0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN46/RPB6/RB6	49	EMDIO/AEMDIO/RPD1/SCK1/RD1
18	PGED2/AN47/RPB7/RB7	50	ETXERR/AETXEN/RPD2/SDA3/RD2
19	AVDD	51	AERXERR/ETXCLK/RPD3/SCL3/RD3
20	AVss	52	SQICS0/RPD4/PMWR/RD4
21	AN48/RPB8/PMA10/RB8	53	SQICS1/RPD5/PMRD/RD5
22	AN49/RPB9/PMA7/RB9	54	VDD
23	TMS/CVREFOUT/AN5/RPB10/PMA13/RB10	55	VSS
24	TDO/AN6/PMA12/RB11	56	ERXD3/AETXD1/RPF0/RF0
25	VSS	57	TRCLK/SQICLK/ERXD2/AETXD0/RPF1/RF1
26	VDD	58	TRD0/SQID0/ERXD1/PMD0/RE0
27	TCK/AN7/PMA11/RB12	59	VSS
28	TDI/AN8/RB13	60	VDD
29	AN9/RPB14/SCK3/PMA1/RB14	61	TRD1/SQID1/ERXD0/PMD1/RE1
30	AN10/EMDC/AEMDC/RPB15/OCFB/PMA0/RB15	62	TRD2/SQID2/ERXDV/ECRSDV/AECRSDV/PMD2/RE2
31	OSC1/CLKI/RC12	63	TRD3/SQID3/ERXCLK/EREFCLK/RPE3/PMD3/RE3
32	OSC2/CLKO/RC15	64	AN18/ERXERR/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 3: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100



Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/AERXERR/RG15	36	VSS
2	EBIA5/AN34/PMA5/RA5	37	VDD
3	EBID5/AN17/RPE5/PMD5/RE5	38	TCK/EBIA19/AN29/RA1
4	EBID6/AN16/PMD6/RE6	39	TDI/EBIA18/AN30/RPF13/SCK5/RF13
5	EBID7/AN15/PMD7/RE7	40	TDO/EBIA17/AN31/RPF12/RF12
6	EBIA6/AN22/RPC1/PMA6/RC1	41	EBIA11/AN7/ERXD0/AECRS/PMA11/RB12
7	EBIA12/AN21/RPC2/PMA12/RC2	42	AN8/ERXD1/AECOL/RB13
8	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	43	EBIA1/AN9/ERXD2/AETXD3/RPB14/SCK3/PMA1/RB14
9	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	44	EBIA0/AN10/ERXD3/AETXD2/RPB15/OCFB/PMA0/RB15
10	AN14/C1IND/ECOL/RPG6/SCK2/RG6	45	VSS
11	EBIA4/AN13/C1INC/ECRS/RPG7/SDA4/PMA4/RG7	46	VDD
12	EBIA3/AN12/C2IND/ERXDV/ECRSDV/AERXDV/ AECRSDV/RPG8/SCL4/PMA3/RG8	47	AN32/AETXD0/RPD14/RD14
13	VSS	48	AN33/AETXD1/RPD15/SCK6/RD15
14	VDD	49	OSC1/CLKI/RC12
15	$\overline{\text{MCLR}}$	50	OSC2/CLKO/RC15
16	EBIA2/AN11/C2INC/ERXCLK/EREFCLK/AERXCLK/ AEREFCLK/RPG9/PMA2/RG9	51	VBUS
17	TMS/EBIA16/AN24/RA0	52	VUSB3V3
18	AN25/AERXD0/RPE8/RE8	53	VSS
19	AN26/AERXD1/RPE9/RE9	54	D-
20	AN45/C1INA/RPB5/RB5	55	D+
21	AN4/C1INB/RB4	56	RPF3/USBID/RF3
22	AN3/C2INA/RPB3/RB3	57	EBIRDY3/RPF2/SDA3/RF2
23	AN2/C2INB/RPB2/RB2	58	EBIRDY2/RPF8/SCL3/RF8
24	PGEC1/AN1/RPB1/RB1	59	$\overline{\text{EBICS0}}$/SCL2/RA2
25	PGED1/AN0/RPB0/RB0	60	EBIRDY1/SDA2/RA3
26	PGEC2/AN46/RPB6/RB6	61	EBIA14/PMCS1/PMA14/RA4
27	PGED2/AN47/RPB7/RB7	62	VDD
28	VREF-/CVREF-/AN27/AERXD2/RA9	63	VSS
29	VREF+/CVREF+/AN28/AERXD3/RA10	64	EBIA9/RPF4/SDA5/PMA9/RF4
30	AVDD	65	EBIA8/RPF5/SCL5/PMA8/RF5
31	AVSS	66	AETXCLK/RPA14/SCL1/RA14
32	EBIA10/AN48/RPB8/PMA10/RB8	67	AETXEN/RPA15/SDA1/RA15
33	EBIA7/AN49/RPB9/PMA7/RB9	68	EBIA15/RPD9/PMCS2/PMA15/RD9
34	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	69	RPD10/SCK4/RD10
35	AN6/ERXERR/AETXERR/RB11	70	EMDC/AEMDC/RPD11/RD11

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

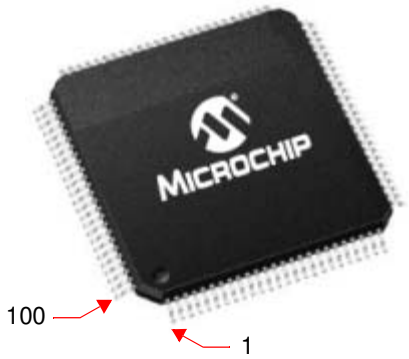
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 3: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100



Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDIO/AEMDIO/RPD0/RTCC/INT0/RD0	86	EBID10/ETXD0/RPF1/PMD10/RF1
72	SOSCI/RPC13/RC13	87	EBID9/ETXERR/RPG1/PMD9/RG1
73	SOSCO/RPC14/T1CK/RC14	88	EBID8/RPG0/PMD8/RG0
74	VDD	89	TRCLK/SQICLK/RA6
75	VSS	90	TRD3/SQID3/RA7
76	RPD1/SCK1/RD1	91	EBID0/PMD0/RE0
77	EBID14/ETXEN/RPD2/PMD14/RD2	92	VSS
78	EBID15/ETXCLK/RPD3/PMD15/RD3	93	VDD
79	EBID12/ETXD2/RPD12/PMD12/RD12	94	EBID1/PMD1/RE1
80	EBID13/ETXD3/PMD13/RD13	95	TRD2/SQID2/RG14
81	$\overline{\text{SQICS0}}$/RPD4/RD4	96	TRD1/SQID1/RG12
82	$\overline{\text{SQICS1}}$/RPD5/RD5	97	TRD0/SQID0/RG13
83	VDD	98	EBID2/PMD2/RE2
84	VSS	99	EBID3/RPE3/PMD3/RE3
85	EBID11/ETXD1/RPF0/PMD11/RF0	100	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

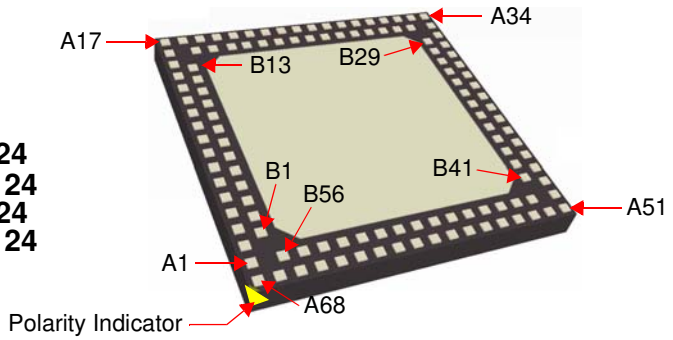
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 4: PIN NAMES FOR 124-PIN DEVICES

124-PIN VTLA (BOTTOM VIEW)

PIC32MZ0512EF(E/F/K)124
PIC32MZ1024EF(G/H/M)124
PIC32MZ1024EF(E/F/K)124
PIC32MZ2048EF(G/H/M)124



Package Pin #	Full Pin Name
A1	No Connect
A2	AN23/RG15
A3	EBID5/AN17/RPE5/PMD5/RE5
A4	EBID7/AN15/PMD7/RE7
A5	AN35/ETXD0/RJ8
A6	EBIA12/AN21/RPC2/PMA12/RC2
A7	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4
A8	EBIA4/AN13/C1INC/RPG7/SDA4/PMA4/RG7
A9	VSS
A10	$\overline{\text{MCLR}}$
A11	TMS/EBIA16/AN24/RA0
A12	AN26/RPE9/RE9
A13	AN4/C1INB/RB4
A14	AN3/C2INA/RPB3/RB3
A15	VDD
A16	AN2/C2INB/RPB2/RB2
A17	PGEC1/AN1/RPB1/RB1
A18	PGED1/AN0/RPB0/RB0
A19	PGED2/AN47/RPB7/RB7
A20	VREF+/CVREF+/AN28/RA10
A21	AVSS
A22	AN39/ETXD3/RH1
A23	EBIA7/AN49/RPB9/PMA7/RB9
A24	AN6/RB11
A25	VDD
A26	TDI/EBIA18/AN30/RPF13/SCK5/RF13
A27	EBIA11/AN7/PMA11/RB12
A28	EBIA1/AN9/RPB14/SCK3/PMA1/RB14
A29	VSS
A30	AN40/ERXERR/RH4
A31	AN42/ERXD2/RH6
A32	AN33/RPD15/SCK6/RD15
A33	OSC2/CLKO/RC15
A34	No Connect

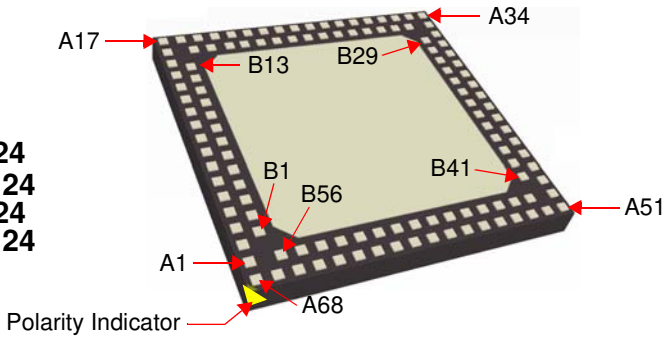
Package Pin #	Full Pin Name
A35	VBUS
A36	VUSB3V3
A37	D-
A38	RPF3/USBID/RF3
A39	EBIRDY2/RPF8/SCL3/RF8
A40	ERXD3/RH9
A41	$\overline{\text{EBICS0}}$/SCL2/RA2
A42	EBIA14/PMCS1/PMA14/RA4
A43	VSS
A44	EBIA8/RPF5/SCL5/PMA8/RF5
A45	RPA15/SDA1/RA15
A46	RPD10/SCK4/RD10
A47	ECRS/RH12
A48	RPD0/RTCC/INT0/RD0
A49	SOSCO/RPC14/T1CK/RC14
A50	VDD
A51	VSS
A52	RPD1/SCK1/RD1
A53	EBID15/RPD3/PMD15/RD3
A54	EBID13/PMD13/RD13
A55	EMDIO/RJ1
A56	$\overline{\text{SQICS0}}$/RPD4/RD4
A57	ETXEN/RPD6/RD6
A58	VDD
A59	EBID11/RPF0/PMD11/RF0
A60	EBID9/RPG1/PMD9/RG1
A61	TRCLK/SQICLK/RA6
A62	RJ4
A63	VSS
A64	EBID1/PMD1/RE1
A65	TRD1/SQID1/RG12
A66	EBID2/SQID2/PMD2/RE2
A67	EBID4/AN18/PMD4/RE4
A68	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 4: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)

PIC32MZ0512EF(E/F/K)124
PIC32MZ1024EF(G/H/M)124
PIC32MZ1024EF(E/F/K)124
PIC32MZ2048EF(G/H/M)124



Package Pin #	Full Pin Name
B1	EBIA5/AN34/PMA5/RA5
B2	EBID6/AN16/PMD6/RE6
B3	EBIA6/AN22/RPC1/PMA6/RC1
B4	AN36/ETXD1/RJ9
B5	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3
B6	AN14/C1IND/RPG6/SCK2/RG6
B7	EBIA3/AN12/C2IND/RPG8/SCL4/PMA3/RG8
B8	VDD
B9	EBIA2/AN11/C2INC/RPG9/PMA2/RG9
B10	AN25/RPE8/RE8
B11	AN45/C1INA/RPB5/RB5
B12	AN37/ERXCLK/EREFCLK/RJ11
B13	VSS
B14	PGEC2/AN46/RPB6/RB6
B15	VREF-/CVREF-/AN27/RA9
B16	AVDD
B17	AN38/ETXD2/RH0
B18	EBIA10/AN48/RPB8/PMA10/RB8
B19	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10
B20	VSS
B21	TCK/EBIA19/AN29/RA1
B22	TDO/EBIA17/AN31/RPF12/RF12
B23	AN8/RB13
B24	EBIA0/AN10/RPB15/OCFB/PMA0/RB15
B25	VDD
B26	AN41/ERXD1/RH5
B27	AN32/AETXD0/RPD14/RD14
B28	OSC1/CLKI/RC12

Package Pin #	Full Pin Name
B29	VSS
B30	D+
B31	RPF2/SDA3/RF2
B32	ERXD0/RH8
B33	ECOL/RH10
B34	EBIRDY1/SDA2/RA3
B35	VDD
B36	EBIA9/RPF4/SDA5/PMA9/RF4
B37	RPA14/SCL1/RA14
B38	EBIA15/RPD9/PMCS2/PMA15/RD9
B39	EMDC/RPD11/RD11
B40	ERXDV/ECRSDV/RH13
B41	SOSCI/RPC13/RC13
B42	EBID14/RPD2/PMD14/RD2
B43	EBID12/RPD12/PMD12/RD12
B44	ETXERR/RJ0
B45	EBIRDY3/RJ2
B46	$\overline{\text{SQICS1}}$/RPD5/RD5
B47	ETXCLK/RPD7/RD7
B48	VSS
B49	EBID10/RPF1/PMD10/RF1
B50	EBID8/RPG0/PMD8/RG0
B51	TRD3/SQID3/RA7
B52	EBID0/PMD0/RE0
B53	VDD
B54	TRD2/SQID2/RG14
B55	TRD0/SQID0/RG13
B56	EBID3/RPE3/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

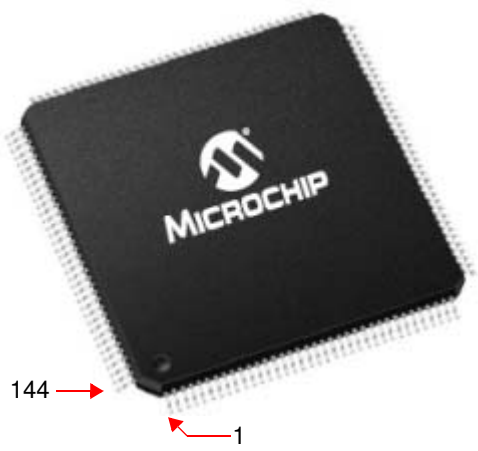
3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 5: PIN NAMES FOR 144-PIN DEVICES

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)144
PIC32MZ1024EF(G/H/M)144
PIC32MZ1024EF(E/F/K)144
PIC32MZ2048EF(G/H/M)144



Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	AN23/RG15	37	PGEC2/AN46/RPB6/RB6
2	EBIA5/AN34/PMA5/RA5	38	PGED2/AN47/RPB7/RB7
3	EBID5/AN17/RPE5/PMD5/RE5	39	VREF-/CVREF-/AN27/RA9
4	EBID6/AN16/PMD6/RE6	40	VREF+/CVREF+/AN28/RA10
5	EBID7/AN15/PMD7/RE7	41	AVDD
6	EBIA6/AN22/RPC1/PMA6/RC1	42	AVSS
7	AN35/ETXD0/RJ8	43	AN38/ETXD2/RH0
8	AN36/ETXD1/RJ9	44	AN39/ETXD3/RH1
9	$\overline{\text{EBIBS0}}$/RJ12	45	$\overline{\text{EBIRP}}$/RH2
10	$\overline{\text{EBIBS1}}$/RJ10	46	RH3
11	EBIA12/AN21/RPC2/PMA12/RC2	47	EBIA10/AN48/RPB8/PMA10/RB8
12	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	48	EBIA7/AN49/RPB9/PMA7/RB9
13	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	49	CVREFOUT/AN5/RPB10/RB10
14	AN14/C1IND/RPG6/SCK2/RG6	50	AN6/RB11
15	AN13/C1INC/RPG7/SDA4/RG7	51	EBIA1/PMA1/RK1
16	AN12/C2IND/RPG8/SCL4/RG8	52	EBIA3/PMA3/RK2
17	VSS	53	EBIA17/RK3
18	VDD	54	VSS
19	EBIA16/RK0	55	VDD
20	$\overline{\text{MCLR}}$	56	TCK/AN29/RA1
21	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	57	TDI/AN30/RPF13/SCK5/RF13
22	TMS/AN24/RA0	58	TDO/AN31/RPF12/RF12
23	AN25/RPE8/RE8	59	AN7/RB12
24	AN26/RPE9/RE9	60	AN8/RB13
25	AN45/C1INA/RPB5/RB5	61	AN9/RPB14/SCK3/RB14
26	AN4/C1INB/RB4	62	AN10/RPB15/OCFB/RB15
27	AN37/ERXCLK/EREFCLK/RJ11	63	VSS
28	EBIA13/PMA13/RJ13	64	VDD
29	EBIA11/PMA11/RJ14	65	AN40/ERXERR/RH4
30	EBIA0/PMA0/RJ15	66	AN41/ERXD1/RH5
31	AN3/C2INA/RPB3/RB3	67	AN42/ERXD2/RH6
32	VSS	68	EBIA4/PMA4/RH7
33	VDD	69	AN32/RPD14/RD14
34	AN2/C2INB/RPB2/RB2	70	AN33/RPD15/SCK6/RD15
35	PGEC1/AN1/RPB1/RB1	71	OSC1/CLKI/RC12
36	PGED1/AN0/RPB0/RB0	72	OSC2/CLKO/RC15

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

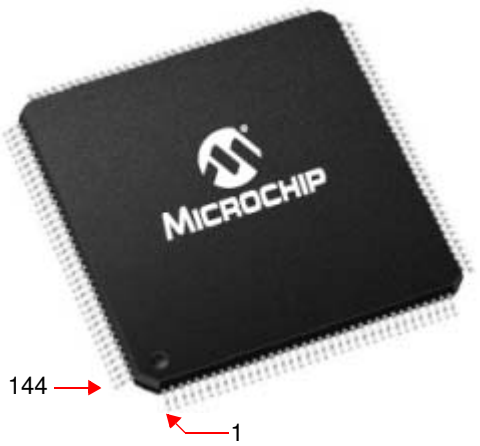
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 5: PIN NAMES FOR 144-PIN DEVICES (CONTINUED)

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)144
PIC32MZ1024EF(G/H/M)144
PIC32MZ1024EF(E/F/K)144
PIC32MZ2048EF(G/H/M)144



Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	VBUS	109	RPD1/SCK1/RD1
74	VUSB3V3	110	EBID14/RPD2/PMD14/RD2
75	VSS	111	EBID15/RPD3/PMD15/RD3
76	D-	112	EBID12/RPD12/PMD12/RD12
77	D+	113	EBID13/PMD13/RD13
78	RPF3/USBID/RF3	114	ETXERR/RJ0
79	SDA3/RPF2/RF2	115	EMDIO/RJ1
80	SCL3/RPF8/RF8	116	EBIRDY3/RJ2
81	ERXD0/RH8	117	EBIA22/RJ3
82	ERXD3/RH9	118	$\overline{\text{SQICS0}}$/RPD4/RD4
83	ECOL/RH10	119	$\overline{\text{SQICS1}}$/RPD5/RD5
84	EBIRDY2/RH11	120	ETXEN/RPD6/RD6
85	SCL2/RA2	121	ETXCLK/RPD7/RD7
86	EBIRDY1/SDA2/RA3	122	VDD
87	EBIA14/PMCS1/PMA14/RA4	123	VSS
88	VDD	124	EBID11/RPF0/PMD11/RF0
89	VSS	125	EBID10/RPF1/PMD10/RF1
90	EBIA9/RPF4/SDA5/PMA9/RF4	126	EBIA21/RK7
91	EBIA8/RPF5/SCL5/PMA8/RF5	127	EBID9/RPG1/PMD9/RG1
92	EBIA18/RK4	128	EBID8/RPG0/PMD8/RG0
93	EBIA19/RK5	129	TRCLK/SQICLK/RA6
94	EBIA20/RK6	130	TRD3/SQID3/RA7
95	RPA14/SCL1/RA14	131	$\overline{\text{EBICS0}}$/RJ4
96	RPA15/SDA1/RA15	132	$\overline{\text{EBICS1}}$/RJ5
97	EBIA15/RPD9/PMCS2/PMA15/RD9	133	$\overline{\text{EBICS2}}$/RJ6
98	RPD10/SCK4/RD10	134	$\overline{\text{EBICS3}}$/RJ7
99	EMDC/RPD11/RD11	135	EBID0/PMD0/RE0
100	ECRS/RH12	136	VSS
101	ERXDV/ECRSDV/RH13	137	VDD
102	RH14	138	EBID1/PMD1/RE1
103	EBIA23/RH15	139	TRD2/SQID2/RG14
104	RPD0/RTCC/INT0/RD0	140	TRD1/SQID1/RG12
105	SOSCI/RPC13/RC13	141	TRD0/SQID0/RG13
106	SOSCO/RPC14/T1CK/RC14	142	EBID2/PMD2/RE2
107	VDD	143	EBID3/RPE3/PMD3/RE3
108	VSS	144	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 35. "Ethernet Controller"** (DS60001155)
- **Section 41. "Prefetch Module for Devices with L1 CPU Cache"** (DS60001183)
- **Section 42. "Oscillators with Enhanced PLL"** (DS60001250)
- **Section 46. "Serial Quad Interface (SQI)"** (DS60001244)
- **Section 47. "External Bus Interface (EBI)"** (DS60001245)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 51. "Hi-Speed USB with On-The-Go (OTG)"** (DS60001326)
- **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193)

NOTES:

1.0 DEVICE OVERVIEW

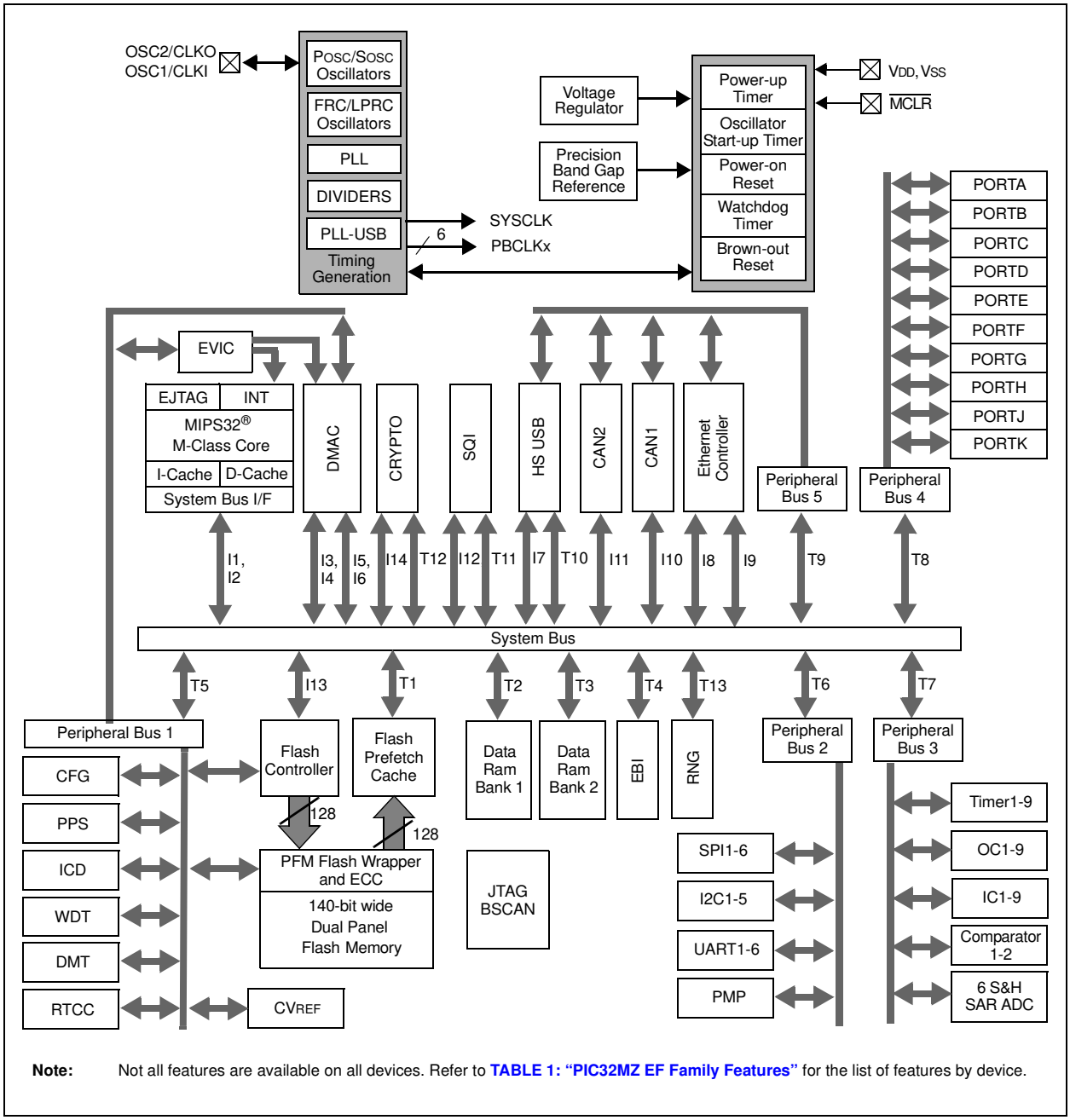
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This data sheet contains device-specific information for PIC32MZ EF devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EF family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 5).

FIGURE 1-1: PIC32MZ EF FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to **TABLE 1: "PIC32MZ EF Family Features"** for the list of features by device.

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AN0	16	25	A18	36	I	Analog	Analog Input Channels
AN1	15	24	A17	35	I	Analog	
AN2	14	23	A16	34	I	Analog	
AN3	13	22	A14	31	I	Analog	
AN4	12	21	A13	26	I	Analog	
AN5	23	34	B19	49	I	Analog	
AN6	24	35	A24	50	I	Analog	
AN7	27	41	A27	59	I	Analog	
AN8	28	42	B23	60	I	Analog	
AN9	29	43	A28	61	I	Analog	
AN10	30	44	B24	62	I	Analog	
AN11	10	16	B9	21	I	Analog	
AN12	6	12	B7	16	I	Analog	
AN13	5	11	A8	15	I	Analog	
AN14	4	10	B6	14	I	Analog	
AN15	3	5	A4	5	I	Analog	
AN16	2	4	B2	4	I	Analog	
AN17	1	3	A3	3	I	Analog	
AN18	64	100	A67	144	I	Analog	
AN19	—	9	A7	13	I	Analog	
AN20	—	8	B5	12	I	Analog	
AN21	—	7	A6	11	I	Analog	
AN22	—	6	B3	6	I	Analog	
AN23	—	1	A2	1	I	Analog	
AN24	—	17	A11	22	I	Analog	
AN25	—	18	B10	23	I	Analog	
AN26	—	19	A12	24	I	Analog	
AN27	—	28	B15	39	I	Analog	
AN28	—	29	A20	40	I	Analog	
AN29	—	38	B21	56	I	Analog	
AN30	—	39	A26	57	I	Analog	
AN31	—	40	B22	58	I	Analog	
AN32	—	47	B27	69	I	Analog	
AN33	—	48	A32	70	I	Analog	
AN34	—	2	B1	2	I	Analog	
AN35	—	—	A5	7	I	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AN36	—	—	B4	8	I	Analog	Analog Input Channels
AN37	—	—	B12	27	I	Analog	
AN38	—	—	B17	43	I	Analog	
AN39	—	—	A22	44	I	Analog	
AN40	—	—	A30	65	I	Analog	
AN41	—	—	B26	66	I	Analog	
AN42	—	—	A31	67	I	Analog	
AN45	11	20	B11	25	I	Analog	
AN46	17	26	B14	37	I	Analog	
AN47	18	27	A19	38	I	Analog	
AN48	21	32	B18	47	I	Analog	
AN49	22	33	A23	48	I	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
CLKI	31	49	B28	71	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	32	50	A33	72	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	31	49	B28	71	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	32	50	A33	72	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	72	B41	105	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	48	73	A49	106	O	—	32.768 low-power oscillator crystal output.
REFCLKI1	PPS	PPS	PPS	PPS	I	—	Reference Clock Generator Inputs 1-4
REFCLKI3	PPS	PPS	PPS	PPS	I	—	
REFCLKI4	PPS	PPS	PPS	PPS	I	—	
REFCLKO1	PPS	PPS	PPS	PPS	O	—	Reference Clock Generator Outputs 1-4
REFCLKO3	PPS	PPS	PPS	PPS	O	—	
REFCLKO4	PPS	PPS	PPS	PPS	O	—	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-3: IC1 THROUGH IC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Input Capture							
IC1	PPS	PPS	PPS	PPS	I	ST	Input Capture Inputs 1-9
IC2	PPS	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	PPS	I	ST	
IC6	PPS	PPS	PPS	PPS	I	ST	
IC7	PPS	PPS	PPS	PPS	I	ST	
IC8	PPS	PPS	PPS	PPS	I	ST	
IC9	PPS	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Output Compare							
OC1	PPS	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	B24	62	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
External Interrupts							
INT0	46	71	A48	104	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTA							
RA0	—	17	A11	22	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	B21	56	I/O	ST	
RA2	—	59	A41	85	I/O	ST	
RA3	—	60	B34	86	I/O	ST	
RA4	—	61	A42	87	I/O	ST	
RA5	—	2	B1	2	I/O	ST	
RA6	—	89	A61	129	I/O	ST	
RA7	—	90	B51	130	I/O	ST	
RA9	—	28	B15	39	I/O	ST	
RA10	—	29	A20	40	I/O	ST	
RA14	—	66	B37	95	I/O	ST	
RA15	—	67	A45	96	I/O	ST	
PORTB							
RB0	16	25	A18	36	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A17	35	I/O	ST	
RB2	14	23	A16	34	I/O	ST	
RB3	13	22	A14	31	I/O	ST	
RB4	12	21	A13	26	I/O	ST	
RB5	11	20	B11	25	I/O	ST	
RB6	17	26	B14	37	I/O	ST	
RB7	18	27	A19	38	I/O	ST	
RB8	21	32	B18	47	I/O	ST	
RB9	22	33	A23	48	I/O	ST	
RB10	23	34	B19	49	I/O	ST	
RB11	24	35	A24	50	I/O	ST	
RB12	27	41	A27	59	I/O	ST	
RB13	28	42	B23	60	I/O	ST	
RB14	29	43	A28	61	I/O	ST	
RB15	30	44	B24	62	I/O	ST	
PORTC							
RC1	—	6	B3	6	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	A6	11	I/O	ST	
RC3	—	8	B5	12	I/O	ST	
RC4	—	9	A7	13	I/O	ST	
RC12	31	49	B28	71	I/O	ST	
RC13	47	72	B41	105	I/O	ST	
RC14	48	73	A49	106	I/O	ST	
RC15	32	50	A33	72	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTD							
RD0	46	71	A48	104	I/O	ST	PORTD is a bidirectional I/O port
RD1	49	76	A52	109	I/O	ST	
RD2	50	77	B42	110	I/O	ST	
RD3	51	78	A53	111	I/O	ST	
RD4	52	81	A56	118	I/O	ST	
RD5	53	82	B46	119	I/O	ST	
RD6	—	—	A57	120	I/O	ST	
RD7	—	—	B47	121	I/O	ST	
RD9	43	68	B38	97	I/O	ST	
RD10	44	69	A46	98	I/O	ST	
RD11	45	70	B39	99	I/O	ST	
RD12	—	79	B43	112	I/O	ST	
RD13	—	80	A54	113	I/O	ST	
RD14	—	47	B27	69	I/O	ST	
RD15	—	48	A32	70	I/O	ST	
PORTE							
RE0	58	91	B52	135	I/O	ST	PORTE is a bidirectional I/O port
RE1	61	94	A64	138	I/O	ST	
RE2	62	98	A66	142	I/O	ST	
RE3	63	99	B56	143	I/O	ST	
RE4	64	100	A67	144	I/O	ST	
RE5	1	3	A3	3	I/O	ST	
RE6	2	4	B2	4	I/O	ST	
RE7	3	5	A4	5	I/O	ST	
RE8	—	18	B10	23	I/O	ST	
RE9	—	19	A12	24	I/O	ST	
PORTF							
RF0	56	85	A59	124	I/O	ST	PORTF is a bidirectional I/O port
RF1	57	86	B49	125	I/O	ST	
RF2	—	57	B31	79	I/O	ST	
RF3	38	56	A38	78	I/O	ST	
RF4	41	64	B36	90	I/O	ST	
RF5	42	65	A44	91	I/O	ST	
RF8	—	58	A39	80	I/O	ST	
RF12	—	40	B22	58	I/O	ST	
RF13	—	39	A26	57	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTG							
RG0	—	88	B50	128	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	87	A60	127	I/O	ST	
RG6	4	10	B6	14	I/O	ST	
RG7	5	11	A8	15	I/O	ST	
RG8	6	12	B7	16	I/O	ST	
RG9	10	16	B9	21	I/O	ST	
RG12	—	96	A65	140	I/O	ST	
RG13	—	97	B55	141	I/O	ST	
RG14	—	95	B54	139	I/O	ST	
RG15	—	1	A2	1	I/O	ST	
PORTH							
RH0	—	—	B17	43	I/O	ST	PORTH is a bidirectional I/O port
RH1	—	—	A22	44	I/O	ST	
RH2	—	—	—	45	I/O	ST	
RH3	—	—	—	46	I/O	ST	
RH4	—	—	A30	65	I/O	ST	
RH5	—	—	B26	66	I/O	ST	
RH6	—	—	A31	67	I/O	ST	
RH7	—	—	—	68	I/O	ST	
RH8	—	—	B32	81	I/O	ST	
RH9	—	—	A40	82	I/O	ST	
RH10	—	—	B33	83	I/O	ST	
RH11	—	—	—	84	I/O	ST	
RH12	—	—	A47	100	I/O	ST	
RH13	—	—	B40	101	I/O	ST	
RH14	—	—	—	102	I/O	ST	
RH15	—	—	—	103	I/O	ST	
PORTJ							
RJ0	—	—	B44	114	I/O	ST	PORTJ is a bidirectional I/O port
RJ1	—	—	A55	115	I/O	ST	
RJ2	—	—	B45	116	I/O	ST	
RJ3	—	—	—	117	I/O	ST	
RJ4	—	—	A62	131	I/O	ST	
RJ5	—	—	—	132	I/O	ST	
RJ6	—	—	—	133	I/O	ST	
RJ7	—	—	—	134	I/O	ST	
RJ8	—	—	A5	7	I/O	ST	
RJ9	—	—	B4	8	I/O	ST	
RJ10	—	—	—	10	I/O	ST	
RJ11	—	—	B12	27	I/O	ST	
RJ12	—	—	—	9	I/O	ST	
RJ13	—	—	—	28	I/O	ST	
RJ14	—	—	—	29	I/O	ST	
RJ15	—	—	—	30	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTK							
RK0	—	—	—	19	I/O	ST	PORTK is a bidirectional I/O port
RK1	—	—	—	51	I/O	ST	
RK2	—	—	—	52	I/O	ST	
RK3	—	—	—	53	I/O	ST	
RK4	—	—	—	92	I/O	ST	
RK5	—	—	—	93	I/O	ST	
RK6	—	—	—	94	I/O	ST	
RK7	—	—	—	126	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-7: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Timer1 through Timer9							
T1CK	48	73	A49	106	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar							
RTCC	46	71	A48	104	O	—	Real-Time Clock Alarm/Seconds Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-8: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Universal Asynchronous Receiver Transmitter 1							
U1RX	PPS	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	PPS	O	—	UART1 Transmit
U1CTS	PPS	PPS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2							
U2RX	PPS	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	PPS	O	—	UART2 Transmit
U2CTS	PPS	PPS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3							
U3RX	PPS	PPS	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	PPS	PPS	O	—	UART3 Transmit
U3CTS	PPS	PPS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4							
U4RX	PPS	PPS	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	PPS	PPS	O	—	UART4 Transmit
U4CTS	PPS	PPS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5							
U5RX	PPS	PPS	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	PPS	PPS	O	—	UART5 Transmit
U5CTS	PPS	PPS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6							
U6RX	PPS	PPS	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	PPS	PPS	O	—	UART6 Transmit
U6CTS	PPS	PPS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select