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PIC32MZ Graphics (DA) Family

32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology

Operating Conditions
- 2.2V to 3.6V, -40ºC to +85ºC, DC to 200 MHz
- 2.2V to 3.6V, -40ºC to +105ºC (Planned)

Core: 200 MHz / 330 DMIPS MIPS32® microAptiv™
- 32 KB I-Cache, 32 KB D-Cache
- MMU for optimum embedded OS execution
- microMIPS™ mode for up to 35% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating and fractional math
- Code-efficient (C and Assembly) architecture

Clock Management
- Programmable PLLs and oscillator clock sources
- Dedicated PLL for DDR2
- Fail-Safe Clock Monitor
- Independent Watchdog and Deadman Timers
- Fast wake-up and start-up

Power Management
- Various power management options for extreme power reduction (V_{BAT}, Deep Sleep, Sleep and Idle)
- Deep Sleep current: < 1 µA (typical)
- Integrated POR and BOR
- Programmable High/Low-Voltage Detect (HLVD) on V_{DDIO} and High-Voltage Detect (HVD) on V_{DDR1V8}

Memory Interfaces
- DDR2 SDRAM interface (up to DDR2-400)
- SD/SDIO/eMMC bus interface (up to 50 MHz)
- Serial Quad Interface (up to 80 MHz)
- External Bus Interface (up to 50 MHz)

Graphics Features
- 3-layer Graphics Controller with up to 24-bit color support
- High-performance 2D Graphics Processing Unit (GPU)

Audio Interfaces
- Audio data communication: I^2S, LJ, and RJ
- Audio control interfaces: SPI and I^2C
- Audio master clock: Fractional clock frequencies with USB synchronization

High-Speed Communication Interfaces (with Dedicated DMA)
- USB 2.0-compliant High-Speed On-The-Go (OTG) controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface

Security Features
- Crypto Engine with a RNG for data encryption/decryption and authentication (AES, 3DES, SHA, MD5, and HMAC)
- Advanced memory protection:
  - Peripheral and memory region access control

Direct Memory Access (DMA)
- Eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)

Advanced Analog Features
- 12-bit ADC modules:
  - 18 Msps with up to six ADC circuits (five dedicated and one shared)
  - Up to 45 analog input
  - Can operate during Sleep and Idle modes
  - Multiple trigger sources
  - Six Digital Comparators and six Digital Filters
- Two Comparators with 32 programmable voltage references
- Temperature sensor with ±2ºC accuracy
- Charge Time Measurement Unit (CTMU)

Communication Interfaces
- Two CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
  - Supports LIN 1.2 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as additional SPI module (up to 80 MHz)
- Five I^2C modules (up to 1 Mbaud) with SMBus support
- Parallel Master Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

Timers/Output Compare/Input Capture
- Nine 16-bit and up to four 32-bit timers/counters
- Nine Output Compare (OC) modules
- Nine Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module

Input/Output
- 5V-tolerant pins with up to 32 mA source/sink
- Selectable open drain, pull-ups, and pull-downs
- Selectable slew rate control
- External interrupts on all I/O pins
- PPS to enable function remap

Qualification and Class B Support
- AEC-Q100 REVG (Grade 2 -40ºC to +105ºC) (Planned)
- Class B Safety Library, IEC 60730
- Back-up internal oscillator

Debugger Development Support
- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Integrated Software Libraries and Tools
- C/C++ compiler with native DSP/fractional support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™, and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPENRTOS®, Micriμm® µC/OS™, and SEGGER embOS®

Packages

Type	LFBGA		LQFP
Pin Count	169	288	176
I/O Pins (up to)	120	120	120
Contact/Lead Pitch	0.8 mm	0.8 mm	0.4 mm
Dimensions	11x11 mm	15x15 mm	20x20 mm

TABLE 1: PIC32MZ DA FEATURES COMMON TO ALL DEVICES

Boot Flash Memory (KB)	Remappable Peripherals						12-bit ADC Channels	Analog Comparators	CTMU	USB 2.0 HS OTG	I^2C	GLCD	GPU	EBI	PMP	SQI	SDHC	RTCC	Ethernet	I/O Pins	JTAG	Trace
	Remappable Pins	Timers[1]/Capture/ Compare	UART	SPI/I^2S	CAN 2.0B	External Interrupts[2]																
160	47	9/9/9	6	6	2	5	45	2	Y	Y	5	Y	Y	Y	Y	Y	Y	Y	Y	120	Y	Y

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.

TABLE 2: 169-PIN LFBGA PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/ Dedicated)
PIC32MZ1025DAA169	1024	256	No	—	N	8/24
PIC32MZ1025DAB169					Y	8/26
PIC32MZ1064DAA169		640			N	8/24
PIC32MZ1064DAB169					Y	8/26
PIC32MZ2025DAA169	2048	256			N	8/24
PIC32MZ2025DAB169					Y	8/26
PIC32MZ2064DAA169		640			N	8/24
PIC32MZ2064DAB169					Y	8/26
PIC32MZ1025DAG169	1024	256	Yes (INT)	32	N	8/24
PIC32MZ1025DAH169					Y	8/26
PIC32MZ1064DAG169		640			N	8/24
PIC32MZ1064DAH169					Y	8/26
PIC32MZ2025DAG169	2048	256			N	8/24
PIC32MZ2025DAH169					Y	8/26
PIC32MZ2064DAG169		640			N	8/24
PIC32MZ2064DAH169					Y	8/26

TABLE 3: 176-PIN LQFP PIC32MZ DA FEATURES

Devices	Program Memory (KB	Data Memory (KB	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/ Dedicated)
PIC32MZ1025DAA176	1024	256	No	—	N	8/24
PIC32MZ1025DAB176					Y	8/26
PIC32MZ1064DAA176		640			N	8/24
PIC32MZ1064DAB176					Y	8/26
PIC32MZ2025DAA176	2048	256			N	8/24
PIC32MZ2025DAB176					Y	8/26
PIC32MZ2064DAA176		640			N	8/24
PIC32MZ2064DAB176					Y	8/26
PIC32MZ1025DAG176	1024	256	Yes (INT)	32	N	8/24
PIC32MZ1025DAH176					Y	8/26
PIC32MZ1064DAG176		640			N	8/24
PIC32MZ1064DAH176					Y	8/26
PIC32MZ2025DAG176	2048	256			N	8/24
PIC32MZ2025DAH176					Y	8/26
PIC32MZ2064DAG176		640			N	8/24
PIC32MZ2064DAH176					Y	8/26

TABLE 4: 288-PIN LFBGA PIC32MZ DA FEATURES

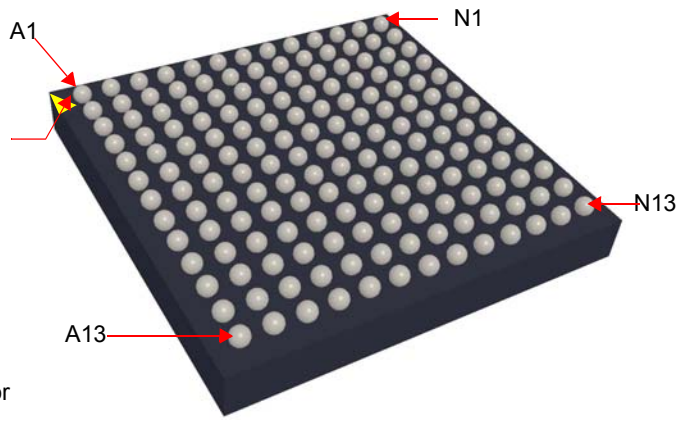
Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	Crypto/RNG	DMA Channels (Programmable/Dedicated)
PIC32MZ1025DAA288	1024	256	Yes (EXT)	N	8/24
PIC32MZ1025DAB288				Y	8/26
PIC32MZ1064DAA288		640		N	8/24
PIC32MZ1064DAB288				Y	8/26
PIC32MZ2025DAA288	2048	256		N	8/24
PIC32MZ2025DAB288				Y	8/26
PIC32MZ2064DAA288		640		N	8/24
PIC32MZ2064DAB288				Y	8/26

Device Pin Tables

TABLE 5: PIN NAMES FOR 169-PIN DEVICES

169-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA169
PIC32MZ1025DAB169
PIC32MZ1064DAA169
PIC32MZ1064DAB169
PIC32MZ2025DAA169
PIC32MZ2025DAB169
PIC32MZ2064DAA169
PIC32MZ2064DAB169
PIC32MZ1025DAG169
PIC32MZ1025DAH169
PIC32MZ1064DAG169
PIC32MZ1064DAH169
PIC32MZ2025DAG169
PIC32MZ2025DAH169
PIC32MZ2064DAG169
PIC32MZ2064DAH169



Ball/Pin Number	Full Pin Name
A1	No Connect
A2	VBUS
A3	RPF2/SDA3/RF2
A4	EBID1/AN39/PMD1/RE1
A5	AN21/RG15
A6	TDI/AN17/SCK5/RF13
A7	$\overline{\text{EBIWE}}$/AN34/RPC3/PMWR/RC3
A8	EBID12/AN10/RPC2/PMD12/RC2
A9	EBID10/AN4/RPB8/PMD10/RB8
A10	AN8/RPB3/RB3
A11	EBIA5/AN7/PMA5/RA5
A12	AN2/C1INB/RB4
A13	AN1/C2INB/RPB2/RB2
B1	D-
B2	VUSB3V3
B3	EBID4/AN18/PMD4/RE4
B4	VDDCORE
B5	AN30/C2IND/RPG8/SCL4/RG8
B6	VDDIO
B7	EBID5/AN12/RPC1/PMD5/RC1
B8	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4
B9	PGEC1/AN9/RPB1/CTED1/RB1
B10	AN3/C2INA/RPB15/OCFB/RB15
B11	VREF-/CVREF-/AN27/RA9
B12	EBIA7/AN47/HLVDIN/RPB9/PMA7/RB9
B13	AN6/RB12
C1	D+
C2	VSS
C3	INT0/RH14
C4	EBID0/PMD0/RE0

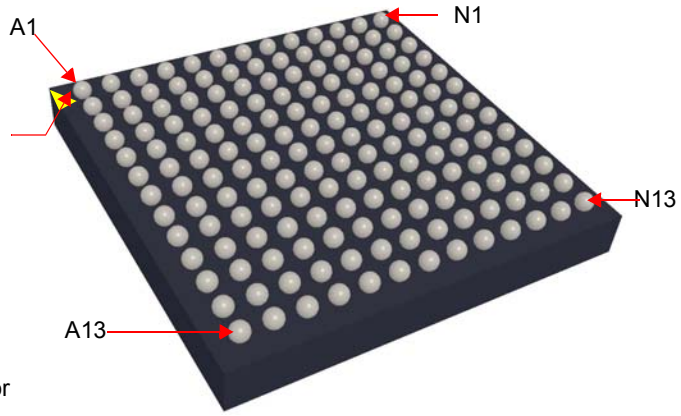
Ball/Pin Number	Full Pin Name
C5	EBIA2/AN23/C2INC/RPG9/PMA2/RG9
C6	TDO/AN31/RPF12/RF12
C7	EBID7/AN15/PMD7/RE7
C8	AVSS
C9	VDDCORE
C10	VREF+/CVREF+/AN28/RA10
C11	CVREFOUT/AN5/RPB10/RB10
C12	PGED1/AN0/RPB0/CTED2/RB0
C13	SOSCI/RPC13(6)/RC13(6)
D1	TRD3/SDDATA3/SQID3/RA7
D2	TMS/$\overline{\text{SDCD}}$/RA0
D3	USBID
D4	AN20/RH4
D5	AN13/C1INC/RPG7/SDA4/RG7
D6	AN26/RPE9/RE9
D7	PGEC2/RPB6/RB6
D8	AVSS
D9	AVDD
D10	VBAT
D11	AN45/RPB5/RB5
D12	PGED2/C1INA/AN46/RPB7/RB7
D13	SOSCO/RPC14(6)/T1CK/RC14(6)
E1	TRD2/SDDATA2/SQID2/RG14
E2	TRD0/SDDATA0/SQID0/RG13
E3	TRD1/SDDATA1/SQID1/RG12
E4	TRCLK/SDCK/SQICLK/RA6
E5	AN14/C1IND/SCK2/RG6
E6	AN25/RPE8/RE8
E7	AN49/RB11
E8	GD20/EBIA22/RJ3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 2 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
5: This pin is a No Connect in devices without DDR.
6: These pins are restricted to input functions only.

TABLE 5: PIN NAMES FOR 169-PIN DEVICES (CONTINUED)

169-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA169
PIC32MZ1025DAB169
PIC32MZ1064DAA169
PIC32MZ1064DAB169
PIC32MZ2025DAA169
PIC32MZ2025DAB169
PIC32MZ2064DAA169
PIC32MZ2064DAB169
PIC32MZ1025DAG169
PIC32MZ1025DAH169
PIC32MZ1064DAG169
PIC32MZ1064DAH169
PIC32MZ2025DAG169
PIC32MZ2025DAH169
PIC32MZ2064DAG169
PIC32MZ2064DAH169



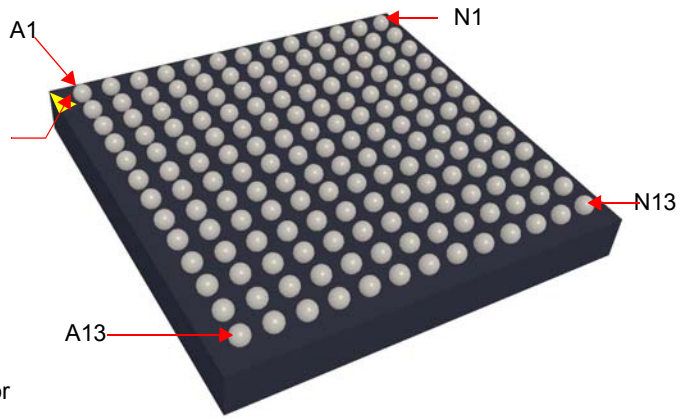
Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
E9	AN22/RPD14/RD14	H2	SCK4/RD10
E10	AN29/SCK3/RB14	H3	RTCC/RPD0/RD0
E11	TCK/AN24/RA1	H4	V_{SS1V8}
E12	OSC1/CLKI/RC12	H5	V_{DDR1V8}(4)
E13	OSC2/CLKO/RC15	H6	V_{DDR1V8}(4)
F1	SDCMD/SQICS0/RPD4/RD4	H7	V_{SS}
F2	SQICS1/RPD5/RD5	H8	V_{SS}
F3	EBIA6/RPE5/PMA6/RE5	H9	V_{DDIO}
F4	$DDRV_{REF}$(5)	H10	GD13/EBIA18/RK4
F5	V_{SS}	H11	EBIA3/AN11/PMA3/RK2
F6	EBID6/AN16/PMD6/RE6	H12	$\overline{SDWP}$/EBIRP/RH2
F7	AN48/CTPLS/RB13	H13	EBIA0/PMA0/RJ15
F8	GD18/EBIBS1/RJ10	J1	GD7/EBIA12/RPD12/PMA12/RD12
F9	GD9/EBIBS0/RJ12	J2	GD22/EBIA13/PMA13/RD13
F10	EBIRDY3/AN32/RJ2	J3	RPF8/SCL3/RF8
F11	AN33/SCK6/RD15	J4	V_{SS1V8}
F12	HSYNC/EBICS1/RJ5	J5	V_{DDR1V8}(4)
F13	VSYNC/EBICS0/RJ4	J6	V_{DDR1V8}(4)
G1	SCK1/RD1	J7	V_{SS}
G2	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2	J8	V_{SS}
G3	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3	J9	V_{DDIO}
G4	V_{SS1V8}	J10	GD14/EBIA19/RK5
G5	V_{SS}	J11	EBIA1/AN38/PMA1/RK1
G6	V_{SS}	J12	EBIA4/AN36/PMA4/RH7
G7	V_{SS}	J13	AN35/RH3
G8	V_{SS}	K1	$\overline{MCLR}$
G9	V_{DDIO}	K2	GD16/EBID8/RPF5/SCL5/PMD8/RF5
G10	GD8/EBID11/PMD11/RJ14	K3	GD5/EBIA10/RPF1/PMA10/RF1
G11	GCLK/EBICS2/RJ6	K4	V_{SS1V8}
G12	GD0/EBID13/PMD13/RJ13	K5	V_{DDR1V8}(4)
G13	GEN/EBICS3/RJ7	K6	V_{DDR1V8}(4)
H1	GD2/EBID15/RPD9/PMD15/RD9	K7	Vss

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 2 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
5: This pin is a No Connect in devices without DDR.
6: These pins are restricted to input functions only.

TABLE 5: PIN NAMES FOR 169-PIN DEVICES (CONTINUED)

169-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA169
PIC32MZ1025DAB169
PIC32MZ1064DAA169
PIC32MZ1064DAB169
PIC32MZ2025DAA169
PIC32MZ2025DAB169
PIC32MZ2064DAA169
PIC32MZ2064DAB169
PIC32MZ1025DAG169
PIC32MZ1025DAH169
PIC32MZ1064DAG169
PIC32MZ1064DAH169
PIC32MZ2025DAG169
PIC32MZ2025DAH169
PIC32MZ2064DAG169
PIC32MZ2064DAH169



Ball/Pin Number	Full Pin Name
K8	VSS
K9	VDDIO
K10	EMDIO/RJ1
K11	ETXEN/RPD6/RD6
K12	GD23/EBIA16/RK0
K13	EBIRDY2/AN37/RH11
L1	GD6/EBIA11/RPF0/PMA11/RF0
L2	GD21/EBIA23/RH15
L3	GD17/EBID9/RPF4/SDA5/PMD9/RF4
L4	VSS1V8
L5	VSS1V8
L6	VDDIO
L7	VDDIO
L8	VDDCORE
L9	VDDIO
L10	ETXERR/RJ0
L11	GD1/EBID14/PMD14/RA4
L12	SCL2/RA2
L13	GD12/EBIA17/RK3
M1	ERXERR/RPF3/RF3
M2	GD4/EBIA9/RPG1/PMA9/RG1
M3	EBID3/RPE3/PMD3/RE3
M4	ERXD1/RH5

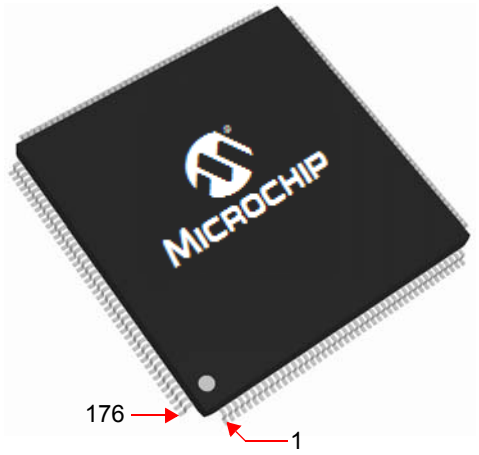
Ball/Pin Number	Full Pin Name
M5	ERXDV/ECRSDV/RH13
M6	ECOL/RH10
M7	ETXD3/RH1
M8	ETXD2/RH0
M9	ETXD1/RJ9
M10	ETXCLK/RPD7/RD7
M11	RPA14/SCL1/RA14
M12	GD19/EBIA21/RK7
M13	GD15/EBIA20/RK6
N1	VDDCORE
N2	GD3/EBIA8/RPG0/PMA8/RG0
N3	EBID2/PMD2/RE2
N4	ERXD2/RH6
N5	ECRS/RH12
N6	ERXD3/RH9
N7	ERXD0/RH8
N8	ERXCLK/EREFCLK/RJ11
N9	ETXD0/RJ8
N10	EMDC/RPD11/RD11
N11	RPA15/SDA1/RA15
N12	EBIRDY1/SDA2/RA3
N13	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 2 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
5: This pin is a No Connect in devices without DDR.
6: These pins are restricted to input functions only.

TABLE 6: PIN NAMES FOR 176-PIN DEVICES

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAA176
PIC32MZ1025DAB176
PIC32MZ1064DAA176
PIC32MZ1064DAB176
PIC32MZ2025DAA176
PIC32MZ2025DAB176
PIC32MZ2064DAA176
PIC32MZ2064DAB176
PIC32MZ1025DAG176
PIC32MZ1025DAH176
PIC32MZ1064DAG176
PIC32MZ1064DAH176
PIC32MZ2025DAG176
PIC32MZ2025DAH176
PIC32MZ2064DAG176
PIC32MZ2064DAH176



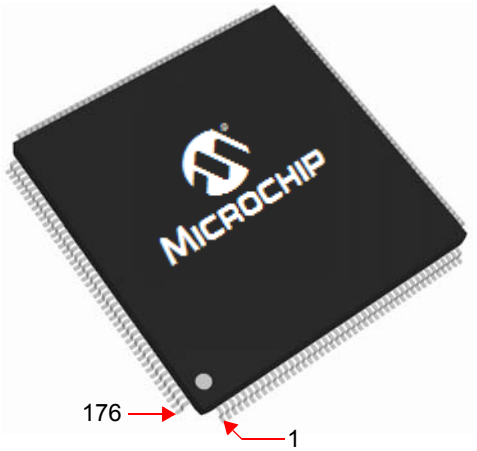
Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	VREF-/CVREF-/AN27/RA9	37	VSS
2	VREF+/CVREF+/AN28/RA10	38	VDDIO
3	AVDD	39	VDDCORE
4	AVDD	40	EBID0/PMD0/RE0
5	AVSS	41	RPF2/SDA3/RF2
6	AVSS	42	INT0/RH14
7	AN3/C2INA/RPB15/OCFB/RB15	43	EBID4/AN18/PMD4/RE4
8	AN8/RPB3/RB3	44	No Connect
9	AN48/CTPLS/RB13	45	VBUS
10	EBID10/AN4/RPB8/PMD10/RB8	46	VUSB3V3
11	PGEC1/AN9/RPB1/CTED1/RB1	47	VUSB3V3
12	AN49/RB11	48	VSS
13	PGEC2/RPB6/RB6	49	VSS
14	EBID12/AN10/RPC2/PMD12/RC2	50	D-
15	EBIWE/AN34/RPC3/PMWR/RC3	51	D+
16	EBIOE/AN19/RPC4/PMRD/RC4	52	USBID
17	EBID5/AN12/RPC1/PMD5/RC1	53	TMS/SDCD/RA0
18	VDDCORE	54	TRCLK/SDCK/SQICLK/RA6
19	VDDIO	55	TRD3/SDDATA3/SQID3/RA7
20	No Connect	56	TRD1/SDDATA1/SQID1/RG12
21	VSS	57	VDDR1V8(5)
22	VSS	58	VDDR1V8(5)
23	EBID6/AN16/PMD6/RE6	59	VDDR1V8(5)
24	EBID7/AN15/PMD7/RE7	60	VDDR1V8(5)
25	AN25/RPE8/RE8	61	VDDR1V8(5)
26	AN26/RPE9/RE9	62	VDDR1V8(5)
27	TDO/AN31/RPF12/RF12	63	VDDR1V8(5)
28	TDI/AN17/SCK5/RF13	64	TRD0/SDDATA0/SQID0/RG13
29	VSS	65	TRD2/SDDATA2/SQID2/RG14
30	AN14/C1IND/SCK2/RG6	66	DDRVREF(6)
31	AN13/C1INC/RPG7/SDA4/RG7	67	VDDR1V8(5)
32	AN30/C2IND/RPG8/SCL4/RG8	68	VDDR1V8(5)
33	EBIA2/AN23/C2INC/RPG9/PMA2/RG9	69	EBIA6/RPE5/PMA6/RE5
34	AN21/RG15	70	SDCMD/SQICS0/RPD4/RD4
35	AN20/RH4	71	SQICS1/RPD5/RD5
36	EBID1/AN39/PMD1/RE1	72	VDDR1V8(5)

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to VSS1V8 and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a No Connect in devices without DDR.
7: These pins are restricted to input functions only.

TABLE 6: PIN NAMES FOR 176-PIN DEVICES (CONTINUED)

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAA176
PIC32MZ1025DAB176
PIC32MZ1064DAA176
PIC32MZ1064DAB176
PIC32MZ2025DAA176
PIC32MZ2025DAB176
PIC32MZ2064DAA176
PIC32MZ2064DAB176
PIC32MZ1025DAG176
PIC32MZ1025DAH176
PIC32MZ1064DAG176
PIC32MZ1064DAH176
PIC32MZ2025DAG176
PIC32MZ2025DAH176
PIC32MZ2064DAG176
PIC32MZ2064DAH176



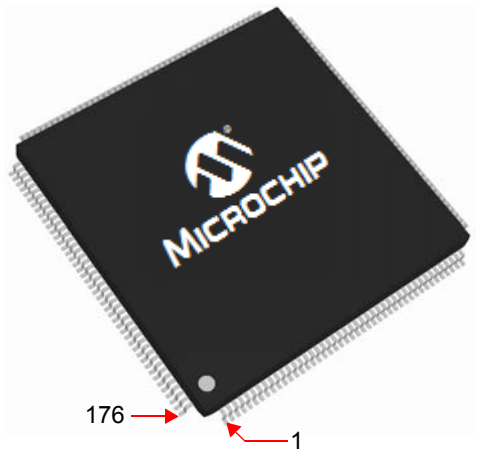
Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	SCK1/RD1	109	ETXD3/RH1
74	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2	110	ETXD2/RH0
75	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3	111	ERXCLK/EREFCLK/RJ11
76	GD2/EBID15/RPD9/PMD15/RD9	112	ETXD1/RJ9
77	SCK4/RD10	113	ETXD0/RJ8
78	VDDR1V8(5)	114	EMDIO/RJ1
79	RTCC/RPD0/RD0	115	VSS
80	GD7/EBIA12/RPD12/PMA12/RD12	116	VDDCORE
81	GD22/EBIA13/PMA13/RD13	117	VDDIO
82	RPF8/SCL3/RF8	118	ETXERR/RJ0
83	VSS	119	EMDC/RPD11/RD11
84	VDDCORE	120	ETXCLK/RPD7/RD7
85	MCLR	121	ETXEN/RPD6/RD6
86	VDDIO	122	VSS
87	VSS	123	VSS
88	No Connect	124	VDDIO
89	GD16/EBID8/RPF5/SCL5/PMD8/RF5	125	RPA15/SDA1/RA15
90	GD5/EBIA10/RPF1/PMA10/RF1	126	RPA14/SCL1/RA14
91	GD6/EBIA11/RPF0/PMA11/RF0	127	GD1/EBID14/PMD14/RA4
92	GD21/EBIA23/RH15	128	EBIRDY1/SDA2/RA3
93	ERXERR/RPF3/RF3	129	SCL2/RA2
94	VSS	130	GD19/EBIA21/RK7
95	GD4/EBIA9/RPG1/PMA9/RG1	131	GD15/EBIA20/RK6
96	GD3/EBIA8/RPG0/PMA8/RG0	132	GD14/EBIA19/RK5
97	GD17/EBID9/RPF4/SDA5/PMD9/RF4	133	GD13/EBIA18/RK4
98	EBID3/RPE3/PMD3/RE3	134	GD12/EBIA17/RK3
99	EBID2/PMD2/RE2	135	EBIA3/AN11/PMA3/RK2
100	ERXD1/RH5	136	EBIA1/AN38/PMA1/RK1
101	ERXD2/RH6	137	GD23/EBIA16/RK0
102	VDDIO	138	EBIRDY2/AN37/RH11
103	VSS	139	EBIA4/AN36/PMA4/RH7
104	ERXDV/ECRSDV/RH13	140	AN35/RH3
105	ECRS/RH12	141	SDWP/EBIRP/RH2
106	ECOL/RH10	142	EBIA0/PMA0/RJ15
107	ERXD3/RH9	143	GD8/EBID11/PMD11/RJ14
108	ERXD0/RH8	144	GD0/EBID13/PMD13/RJ13

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to VSS1V8 and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a No Connect in devices without DDR.
7: These pins are restricted to input functions only.

TABLE 6: PIN NAMES FOR 176-PIN DEVICES (CONTINUED)

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAA176
PIC32MZ1025DAB176
PIC32MZ1064DAA176
PIC32MZ1064DAB176
PIC32MZ2025DAA176
PIC32MZ2025DAB176
PIC32MZ2064DAA176
PIC32MZ2064DAB176
PIC32MZ1025DAG176
PIC32MZ1025DAH176
PIC32MZ1064DAG176
PIC32MZ1064DAH176
PIC32MZ2025DAG176
PIC32MZ2025DAH176
PIC32MZ2064DAG176
PIC32MZ2064DAH176



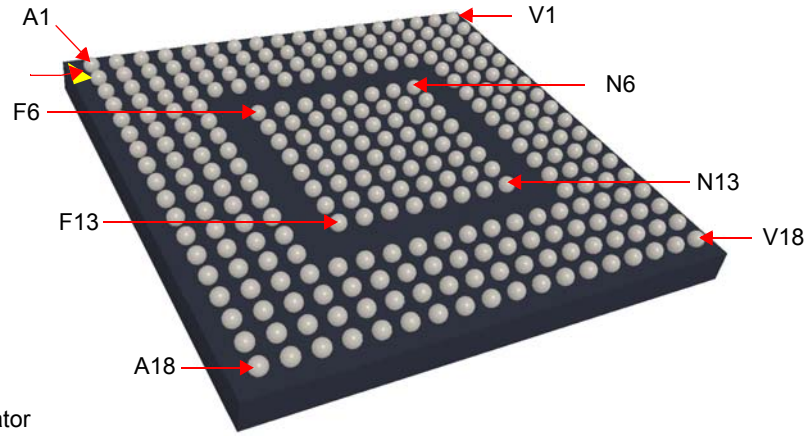
Pin Number	Full Pin Name	Pin Number	Full Pin Name
145	GD9/EBIBS0/RJ12	161	SOSCO/RPC14(7)/T1CK/RC14(7)
146	GD18/EBIBS1/RJ10	162	SOSCI/RPC13(7)/RC13(7)
147	GEN/EBICS3/RJ7	163	OSC2/CLKO/RC15
148	GCLK/EBICS2/RJ6	164	OSC1/CLKI/RC12
149	HSYNC/EBICS1/RJ5	165	VDDIO
150	VSYNC/EBICS0/RJ4	166	VBAT
151	GD20/EBIA22/RJ3	167	AN45/RPB5/RB5
152	EBIRDY3/AN32/RJ2	168	AN5/RPB10/RB10
153	VSS	169	PGED1/AN0/RPB0/CTED2/RB0
154	VSS	170	PGED2/C1INA/AN46/RPB7/RB7
155	VDDIO	171	AN6/RB12
156	VDDIO	172	AN1/C2INB/RPB2/RB2
157	AN33/SCK6/RD15	173	EBIA7/AN47/HLVDIN/RPB9/PMA7/RB9
158	AN22/RPD14/RD14	174	EBIA5/AN7/PMA5/RA5
159	AN29/SCK3/RB14	175	AN2/C1INB/RB4
160	TCK/AN24/RA1	176	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to VSS1V8 and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a No Connect in devices without DDR.
7: These pins are restricted to input functions only.

TABLE 7: PIN NAMES FOR 288-PIN DEVICES

288-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288



Ball/Pin Number	Full Pin Name
A1	No Connect
A2	DDRUDQS
A3	DDRDM1
A4	D-
A5	VSS
A6	INT0/RH14
A7	RPF2/SDA3/RF2
A8	AN21/RG15
A9	AN14/C1IND/SCK2/RG6
A10	TDI/AN17/SCK5/RF13
A11	TDO/AN31/RPF12/RF12
A12	EBID5/AN12/RPC1/PMD5/RC1
A13	EBIOE/AN19/RPC4/PMRD/RC4
A14	PGEC1/AN9/RPB1/CTED1/RB1
A15	EBID10/AN4/RPB8/PMD10/RB8
A16	AN8/RPB3/RB3
A17	VREF-/CVREF-/AN27/RA9
A18	No Connect
B1	No Connect
B2	DDRUDQS
B3	DDRDQ14
B4	D+
B5	VSS
B6	EBID4/AN18/PMD4/RE4
B7	EBID0/PMD0/RE0
B8	AN20/RH4
B9	EBIA2/AN23/C2INC/RPG9/PMA2/RG9
B10	AN26/RPE9/RE9
B11	EBID7/AN15/PMD7/RE7
B12	No Connect
B13	EBIWE/AN34/RPC3/PMWR/RC3
B14	PGEC2/RPB6/RB6
B15	AN48/CTPLS/RB13
B16	AN3/C2INA/RPB15/OCFB/RB15

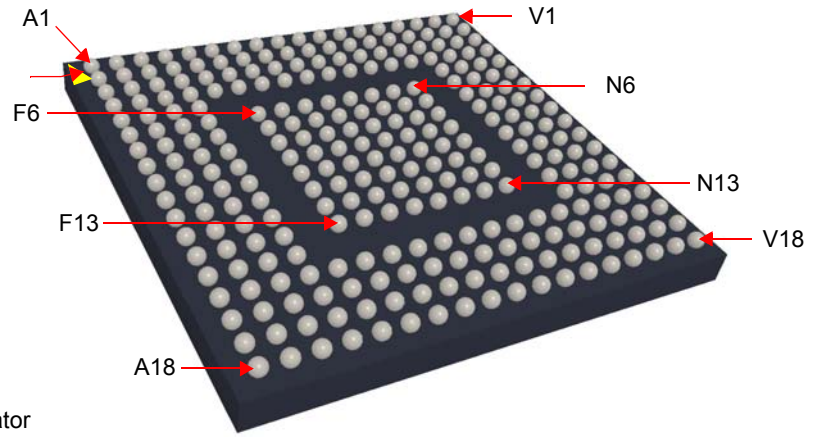
Ball/Pin Number	Full Pin Name
B17	AN2/C1INB/RB4
B18	EBIA5/AN7/PMA5/RA5
C1	DDRDQ8
C2	DDRDQ15
C3	DDRDQ9
C4	VUSB3V3
C5	VBUS
C6	USBID
C7	VSS
C8	No Connect
C9	AN30/C2IND/RPG8/SCL4/RG8
C10	AN25/RPE8/RE8
C11	EBID6/AN16/PMD6/RE6
C12	No Connect
C13	EBID12/AN10/RPC2/PMD12/RC2
C14	AN49/RB11
C15	VREF+/CVREF+/AN28/RA10
C16	VDDIO
C17	AN1/C2INB/RPB2/RB2
C18	AN6/RB12
D1	DDRDQ13
D2	DDRDQ10
D3	VSS1V8
D4	TMS/SDCD/RA0
D5	VUSB3V3
D6	No Connect
D7	VDDCORE
D8	EBID1/AN39/PMD1/RE1
D9	AN13/C1INC/RPG7/SDA4/RG7
D10	VSS
D11	VSS
D12	VSS
D13	VSS
D14	VDDCORE

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.
5: This pin is a No Connect when DDR is not connected in the system.
6: These pins are restricted to input functions only.

TABLE 7: PIN NAMES FOR 288-PIN DEVICES (CONTINUED)

288-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288



Polarity Indicator

Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
D15	VDDIO	G8	VSS1V8
D16	VDDIO	G9	VSS1V8
D17	PGED2/C1INA/AN46/RPB7/RB7	G10	VSS
D18	PGED1/AN0/RPB0/CTED2/RB0	G11	VDDIO
E1	DDRLDQS	G12	AVSS
E2	$\overline{\text{DDRLDQS}}$	G13	AVDD
E3	DDRDQ12	G15	VDDIO
E4	TRCLK/SDCK/SQICLK/RA6	G16	No Connect
E15	VDDIO	G17	OSC1/CLKI/RC12
E16	EBIA7/AN47/HLVDIN/RPB9/PMA7/RB9	G18	OSC2/CLKO/RC15
E17	AN45/RPB5/RB5	H1	DDRDQ2
E18	CVREFOUT/AN5/RPB10/RB10	H2	DDRDQ5
F1	DDRDQ0	H3	DDRDQ6
F2	DDRDQ7	H4	TRD0/SDDATA0/SQID0/RG13
F3	DDRDQ11	H6	VDDR1V8(4)
F4	TRD3/SDDATA3/SQID3/RA7	H7	VDDR1V8(4)
F6	VSS1V8	H8	VDDR1V8(4)
F7	VSS1V8	H9	VSS1V8
F8	VSS1V8	H10	VSS
F9	VSS	H11	VDDIO
F10	VSS	H12	VDDIO
F11	VDDIO	H13	VDDIO
F12	AVSS	H15	VDDIO
F13	AVDD	H16	TCK/AN24/RA1
F15	VDDIO	H17	SOSCI/RPC13(6)/RC13(6)
F16	VBAT	H18	SOSCO/RPC14(6)/T1CK/RC14(6)
F17	No Connect	J1	DDRVREF(5)
F18	No Connect	J2	No Connect
G1	DDRDQ3	J3	DDRDQ1
G2	DDRDQ4	J4	TRD2/SDDATA2/SQID2/RG14
G3	DDRDM0	J6	VDDR1V8(4)
G4	TRD1/SDDATA1/SQID1/RG12	J7	VDDR1V8(4)
G6	VSS1V8	J8	VDDR1V8(4)
G7	VSS1V8	J9	VSS1V8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
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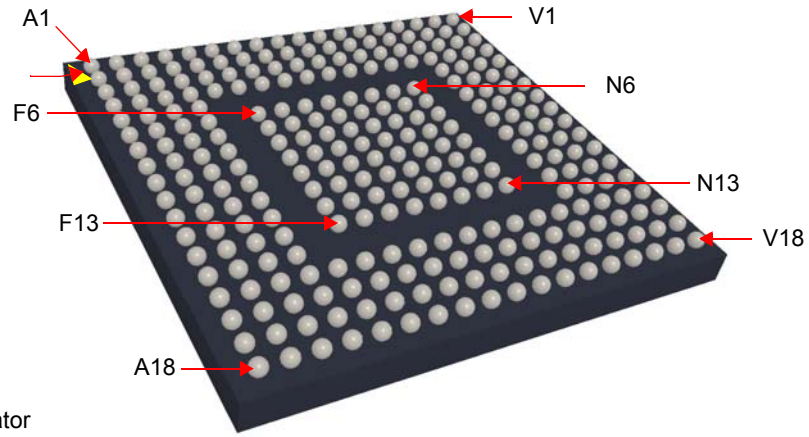
TABLE 7: PIN NAMES FOR 288-PIN DEVICES (CONTINUED)

288-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288



Polarity Indicator

Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
J10	VDDIO	L12	VDDIO
J11	VSS	L13	VSS
J12	VSS	L15	VSS
J13	VSS	L16	GEN/EBICS3/RJ7
J15	VDDIO	L17	GCLK/EBICS2/RJ6
J16	AN33/SCK6/RD15	L18	HSYNC/EBICS1/RJ5
J17	AN29/SCK3/RB14	M1	$\overline{\text{DDRRAS}}$
J18	AN22/RPD14/RD14	M2	DDRBA0
K1	$\overline{\text{DDRCK}}$	M3	DDRBA1
K2	DDRCK	M4	SCK1/RD1
K3	EBIA6/RPE5/PMA6/RE5	M6	VSS1V8
K4	SDCMD/SQICS0/RPD4/RD4	M7	VSS1V8
K6	VDDR1V8(4)	M8	VSS1V8
K7	VDDR1V8(4)	M9	VSS1V8
K8	VDDR1V8(4)	M10	VSS
K9	VSS1V8	M11	VSS
K10	VDDIO	M12	VDDIO
K11	VSS	M13	VDDIO
K12	VSS	M15	VDDIO
K13	VSS	M16	GD0/EBID13/PMD13/RJ13
K15	VSS	M17	GD9/EBIBS0/RJ12
K16	EBIRDY3/AN32/RJ2	M18	GD18/EBIBS1/RJ10
K17	GD20/EBIA22/RJ3	N1	DDRODT
K18	VSYNC/EBICS0/RJ4	N2	$\overline{\text{DDRCS0}}$
L1	$\overline{\text{DDRWE}}$	N3	DDRA2
L2	DDRCKE	N4	GD22/EBIA13/PMA13/RD13
L3	DDRA1	N6	VSS1V8
L4	SQICS1/RPD5/RD5	N7	VSS1V8
L6	VDDR1V8(4)	N8	VSS1V8
L7	VDDR1V8(4)	N9	VSS1V8
L8	VDDR1V8(4)	N10	VSS
L9	VSS1V8	N11	VSS
L10	VSS	N12	VDDIO
L11	VDDIO	N13	VDDIO

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.
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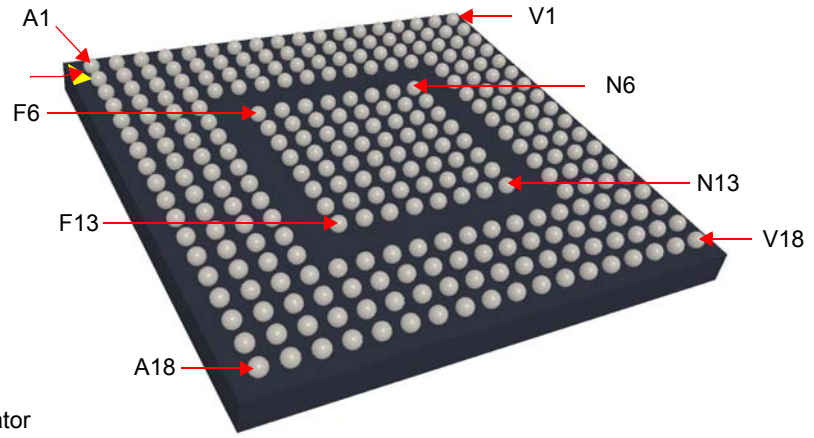
TABLE 7: PIN NAMES FOR 288-PIN DEVICES (CONTINUED)

288-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288



Polarity Indicator

Ball/Pin Number	Full Pin Name
N15	EBIA4/AN36/PMA4/RH7
N16	SDWP/EBIRP/RH2
N17	EBIA0/PMA0/RJ15
N18	GD8/EBID11/PMD11/RJ14
P1	DDRA10
P2	DDRCAS
P3	DDRA4
P4	RPF8/SCL3/RF8
P15	GD13/EBIA18/RK4
P16	GD23/EBIA16/RK0
P17	EBIRDY2/AN37/RH11
P18	AN35/RH3
R1	DDRA0
R2	DDRA3
R3	DDRA9
R4	VSS1V8
R5	MCLR
R6	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2
R7	VSS
R8	VSS
R9	VDDIO
R10	VDDIO
R11	VDDCORE
R12	VDDIO
R13	VDDIO
R14	VDDIO
R15	GD14/EBIA19/RK5
R16	GD12/EBIA17/RK3
R17	EBIA3/AN11/PMA3/RK2
R18	EBIA1/AN38/PMA1/RK1
T1	DDRA5
T2	DDRA7
T3	DDRA12
T4	DDRA14

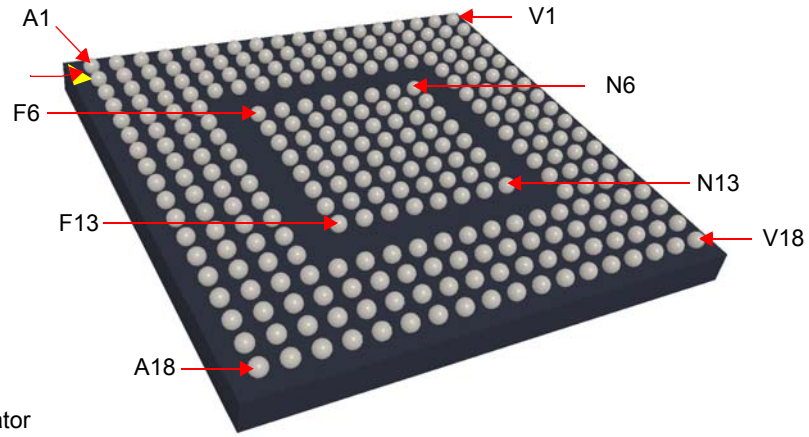
Ball/Pin Number	Full Pin Name
T5	No Connect
T6	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3
T7	GD16/EBID8/RPF5/SCL5/PMD8/RF5
T8	GD4/EBIA9/RPG1/PMA9/RG1
T9	EBID3/RPE3/PMD3/RE3
T10	ERXD2/RH6
T11	ECOL/RH10
T12	ETXD3/RH1
T13	ETXD1/RJ9
T14	No Connect
T15	ETXCLK/RPD7/RD7
T16	RPA14/SCL1/RA14
T17	GD19/EBIA21/RK7
T18	GD15/EBIA20/RK6
U1	DDRA6
U2	DDRA8
U3	DDRA13
U4	DDRBA2
U5	GD7/EBIA12/RPD12/PMA12/RD12
U6	GD2/EBID15/RPD9/PMD15/RD9
U7	GD5/EBIA10/RPF1/PMA10/RF1
U8	ERXERR/RPF3/RF3
U9	GD17/EBID9/RPF4/SDA5/PMD9/RF4
U10	ERXD1/RH5
U11	ECRS/RH12
U12	ERXD0/RH8
U13	ERXCLK/EREFCLK/RJ11
U14	EMDIO/RJ1
U15	EMDC/RPD11/RD11
U16	RPA15/SDA1/RA15
U17	EBIRDY1/SDA2/RA3
U18	SCL2/RA2
V1	No Connect
V2	DDRA11

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.
5: This pin is a No Connect when DDR is not connected in the system.
6: These pins are restricted to input functions only.

TABLE 7: PIN NAMES FOR 288-PIN DEVICES (CONTINUED)

288-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAA288
PIC32MZ1025DAB288
PIC32MZ1064DAA288
PIC32MZ1064DAB288
PIC32MZ2025DAA288
PIC32MZ2025DAB288
PIC32MZ2064DAA288
PIC32MZ2064DAB288



Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
V3	DDRA15	V11	ERXDV/ECRSDV/RH13
V4	VDDCORE	V12	ERXD3/RH9
V5	RTCC/RPD0/RD0	V13	ETXD2/RH0
V6	SCK4/RD10	V14	ETXD0/RJ8
V7	GD6/EBIA11/RPF0/PMA11/RF0	V15	ETXERR/RJ0
V8	GD21/EBIA23/RH15	V16	ETXEN/RPD6/RD6
V9	GD3/EBIA8/RPG0/PMA8/RG0	V17	GD1/EBID14/PMD14/RA4
V10	EBID2/PMD2/RE2	V18	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 4 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor when DDR is not connected in the system.
5: This pin is a No Connect when DDR is not connected in the system.
6: These pins are restricted to input functions only.

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: http://www.microchip.com/pic32.

- **Section 1. "Introduction"** (DS60001127)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 35. "Ethernet Controller"** (DS60001155)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)
- **Section 38. "High/Low Voltage Detect (HLVD)** (DS60001408)
- **Section 41. "Prefetch Module for Devices with L1 CPU Cache"** (DS60001183)
- **Section 42. "Oscillators with Enhanced PLL"** (DS60001250)
- **Section 46. "Serial Quad Interface (SQI)"** (DS60001244)
- **Section 47. "External Bus Interface (EBI)"** (DS60001245)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 51. "High-Speed USB with On-The-Go (OTG)"** (DS60001326)
- **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193)
- **Section 54. "Graphics LCD (GLCD) Controller"** (DS60001379)
- **Section 55. "DDR SDRAM Controller"** (DS60001321)
- **Section 57. "Secure Digital Host Controller (SDHC)"** (DS60001334)

1.0 DEVICE OVERVIEW

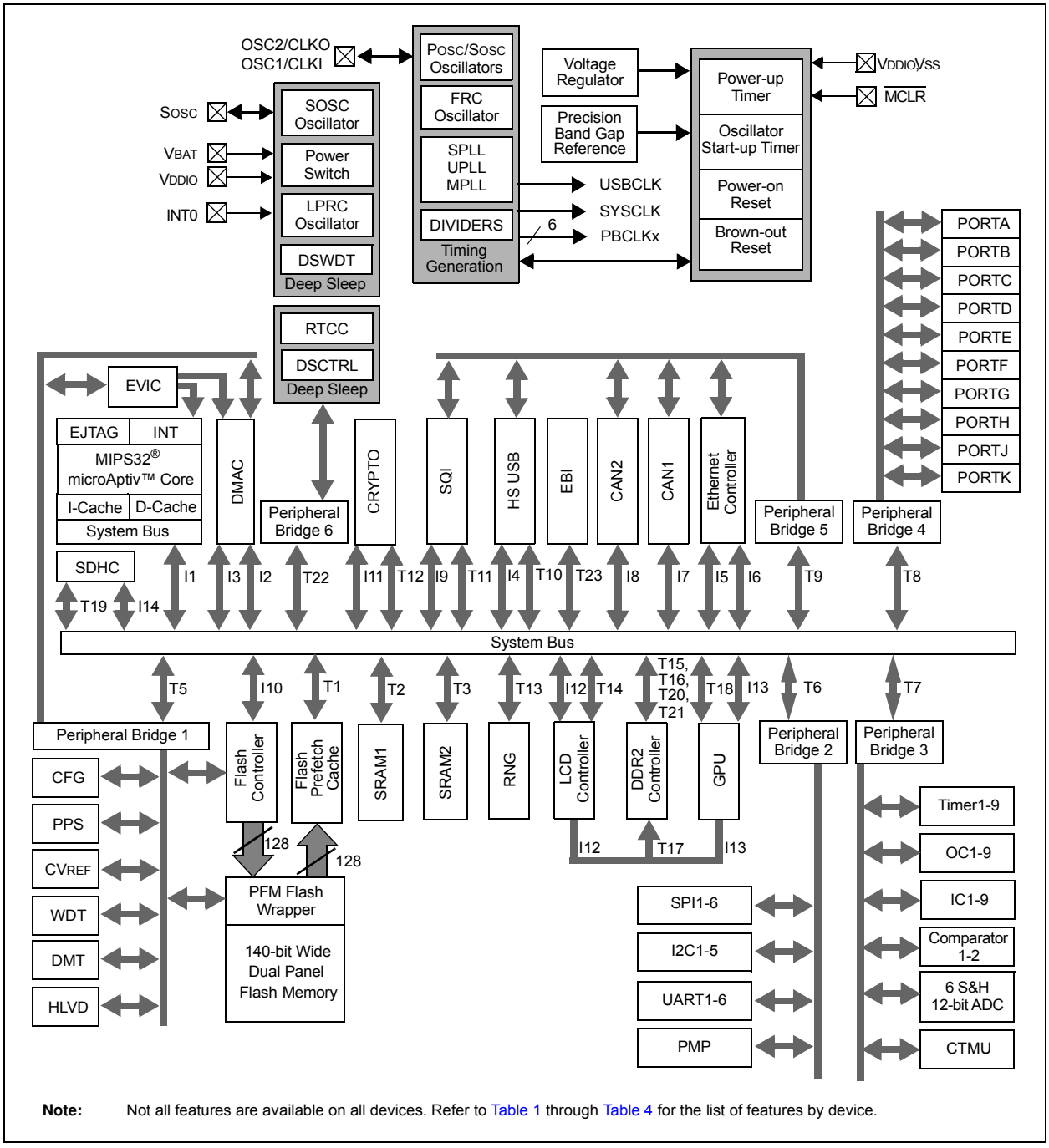
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This data sheet contains device-specific information for the PIC32MZ DA family of devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ DA family of devices.

Table 1-1 through Table 1-24 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 5 through Table 7).

FIGURE 1-1: PIC32MZ DA FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to Table 1 through Table 4 for the list of features by device.

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Analog-to-Digital Converter						
AN0	C12	169	D18	I	Analog	Analog Input Channels
AN1	A13	172	C17	I	Analog	
AN2	A12	175	B17	I	Analog	
AN3	B10	7	B16	I	Analog	
AN4	A9	10	A15	I	Analog	
AN5	C11	168	E18	I	Analog	
AN6	B13	171	C18	I	Analog	
AN7	A11	174	B18	I	Analog	
AN8	A10	8	A16	I	Analog	
AN9	B9	11	A14	I	Analog	
AN10	A8	14	C13	I	Analog	
AN11	H11	135	R17	I	Analog	
AN12	B7	17	A12	I	Analog	
AN13	D5	31	D9	I	Analog	
AN14	E5	30	A9	I	Analog	
AN15	C7	24	B11	I	Analog	
AN16	F6	23	C11	I	Analog	
AN17	A6	28	A10	I	Analog	
AN18	B3	43	B6	I	Analog	
AN19	B8	16	A13	I	Analog	
AN20	D4	35	B8	I	Analog	
AN21	A5	34	A8	I	Analog	
AN22	E9	158	J18	I	Analog	
AN23	C5	33	B9	I	Analog	
AN24	E11	160	H16	I	Analog	
AN25	E6	25	C10	I	Analog	
AN26	D6	26	B10	I	Analog	
AN27	B11	1	A17	I	Analog	
AN28	C10	2	C15	I	Analog	
AN29	E10	159	J17	I	Analog	
AN30	B5	32	C9	I	Analog	
AN31	C6	27	A11	I	Analog	
AN32	F10	152	K16	I	Analog	
AN33	F11	157	J16	I	Analog	
AN34	A7	15	B13	I	Analog	
AN35	J13	140	P18	I	Analog	
AN36	J12	139	N15	I	Analog	
AN37	K13	138	P17	I	Analog	
AN38	J11	136	R18	I	Analog	
AN39	A4	36	D8	I	Analog	
AN45	D11	167	E17	I	Analog	
AN46	D12	170	D17	I	Analog	
AN47	B12	173	E16	I	Analog	
AN48	F7	9	B15	I	Analog	
AN49	E7	12	C14	I	Analog	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Oscillators						
CLKI	E12	164	G17	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	E13	163	G18	O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	E12	164	G17	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	E13	163	G18	O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	C13	162	H17	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	D13	161	H18	O	ST/CMOS	32.768 low-power oscillator crystal output.
REFCLKI1	PPS	PPS	PPS	I	—	Reference Clock Generator Inputs 1-4
REFCLKI3	PPS	PPS	PPS	I	—	
REFCLKI4	PPS	PPS	PPS	I	—	
REFCLKO1	PPS	PPS	PPS	O	—	Reference Clock Generator Outputs 1-4
REFCLKO3	PPS	PPS	PPS	O	—	
REFCLKO4	PPS	PPS	PPS	O	—	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-3: IC1 THROUGH IC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Input Capture						
IC1	PPS	PPS	PPS	I	ST	Input Capture Inputs 1-9
IC2	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	I	ST	
IC6	PPS	PPS	PPS	I	ST	
IC7	PPS	PPS	PPS	I	ST	
IC8	PPS	PPS	PPS	I	ST	
IC9	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Output Compare						
OC1	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
External Interrupts						
INT0	C3	42	A6	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
PORTA						
RA0	D2	53	D4	I/O	ST	PORTA is a bidirectional I/O port
RA1	E11	160	H16	I/O	ST	
RA2	L12	129	U18	I/O	ST	
RA3	N12	128	U17	I/O	ST	
RA4	L11	127	V17	I/O	ST	
RA5	A11	174	B18	I/O	ST	
RA6	E4	54	E4	I/O	ST	
RA7	D1	55	F4	I/O	ST	
RA9	B11	1	A17	I/O	ST	
RA10	C10	2	C15	I/O	ST	
RA14	M11	126	T16	I/O	ST	
RA15	N11	125	U16	I/O	ST	
PORTB						
RB0	C12	169	D18	I/O	ST	PORTB is a bidirectional I/O port
RB1	B9	11	A14	I/O	ST	
RB2	A13	172	C17	I/O	ST	
RB3	A10	8	A16	I/O	ST	
RB4	A12	175	B17	I/O	ST	
RB5	D11	167	E17	I/O	ST	
RB6	D7	13	B14	I/O	ST	
RB7	D12	170	D17	I/O	ST	
RB8	A9	10	A15	I/O	ST	
RB9	B12	173	E16	I/O	ST	
RB10	C11	168	E18	I/O	ST	
RB11	E7	12	C14	I/O	ST	
RB12	B13	171	C18	I/O	ST	
RB13	F7	9	B15	I/O	ST	
RB14	E10	175	J17	I/O	ST	
RB15	B10	7	B16	I/O	ST	
PORTC						
RC1	B7	17	A12	I/O	ST	PORTC is a bidirectional I/O port
RC2	A8	14	C13	I/O	ST	
RC3	A7	15	B13	I/O	ST	
RC4	B8	16	A13	I/O	ST	
RC12	E12	164	G17	I/O	ST	
RC13	C13	162	H17	I	ST	
RC14	D13	161	H18	I	ST	
RC15	E13	163	G18	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
PORTD						
RD0	H3	79	V5	I/O	ST	PORTD is a bidirectional I/O port
RD1	G1	73	M4	I/O	ST	
RD2	G2	74	R6	I/O	ST	
RD3	G3	75	T6	I/O	ST	
RD4	F1	70	K4	I/O	ST	
RD5	F2	71	L4	I/O	ST	
RD6	K11	121	V16	I/O	ST	
RD7	M10	120	T15	I/O	ST	
RD9	H1	76	U6	I/O	ST	
RD10	H2	77	V6	I/O	ST	
RD11	N10	119	U15	I/O	ST	
RD12	J1	80	U5	I/O	ST	
RD13	J2	81	N4	I/O	ST	
RD14	E9	158	J18	I/O	ST	
RD15	F11	157	J16	I/O	ST	
PORTE						
RE0	C4	40	B7	I/O	ST	PORTE is a bidirectional I/O port
RE1	A4	36	D8	I/O	ST	
RE2	N3	99	V10	I/O	ST	
RE3	M3	98	T9	I/O	ST	
RE4	B3	43	B6	I/O	ST	
RE5	F3	17	K3	I/O	ST	
RE6	F6	23	C11	I/O	ST	
RE7	C7	24	B11	I/O	ST	
RE8	E6	25	C10	I/O	ST	
RE9	D6	26	B10	I/O	ST	
PORTF						
RF0	L1	91	V7	I/O	ST	PORTF is a bidirectional I/O port
RF1	K3	90	U7	I/O	ST	
RF2	A3	41	A7	I/O	ST	
RF3	M1	93	U8	I/O	ST	
RF4	L3	44	U9	I/O	ST	
RF5	K2	89	T7	I/O	ST	
RF8	J3	82	P4	I/O	ST	
RF12	C6	27	A11	I/O	ST	
RF13	A6	28	A10	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
PORTG						
RG0	N2	96	V9	I/O	ST	PORTG is a bidirectional I/O port
RG1	M2	95	T8	I/O	ST	
RG6	E5	30	A9	I/O	ST	
RG7	D5	31	D9	I/O	ST	
RG8	B5	32	C9	I/O	ST	
RG9	C5	33	B9	I/O	ST	
RG12	E3	56	G4	I/O	ST	
RG13	E2	64	H4	I/O	ST	
RG14	E1	65	J4	I/O	ST	
RG15	A5	34	A8	I/O	ST	
PORTH						
RH0	M8	110	V13	I/O	ST	PORTH is a bidirectional I/O port
RH1	M7	109	T12	I/O	ST	
RH2	H12	141	N16	I/O	ST	
RH3	J13	140	P18	I/O	ST	
RH4	D4	35	B8	I/O	ST	
RH5	M4	100	U10	I/O	ST	
RH6	N4	101	T10	I/O	ST	
RH7	J12	139	N15	I/O	ST	
RH8	N7	108	U12	I/O	ST	
RH9	N6	107	V12	I/O	ST	
RH10	M6	106	T11	I/O	ST	
RH11	K13	138	P17	I/O	ST	
RH12	N5	105	U11	I/O	ST	
RH13	M5	104	V11	I/O	ST	
RH14	C3	42	A6	I/O	ST	
RH15	L2	92	V8	I/O	ST	
PORTJ						
RJ0	L10	118	V15	I/O	ST	PORTJ is a bidirectional I/O port
RJ1	K10	114	U14	I/O	ST	
RJ2	F10	152	K16	I/O	ST	
RJ3	E8	151	K17	I/O	ST	
RJ4	F13	150	K18	I/O	ST	
RJ5	F12	149	L18	I/O	ST	
RJ6	G11	148	L17	I/O	ST	
RJ7	G13	147	L16	I/O	ST	
RJ8	N9	113	V14	I/O	ST	
RJ9	M9	112	T13	I/O	ST	
RJ10	F8	146	M18	I/O	ST	
RJ11	N8	111	U13	I/O	ST	
RJ12	F9	145	M17	I/O	ST	
RJ13	G12	144	M16	I/O	ST	
RJ14	G10	143	N18	I/O	ST	
RJ15	H13	142	N17	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
PORTK						
RK0	K12	137	P16	I/O	ST	PORTK is a bidirectional I/O port
RK1	J11	136	R18	I/O	ST	
RK2	H11	135	R17	I/O	ST	
RK3	L13	134	R16	I/O	ST	
RK4	H10	133	P15	I/O	ST	
RK5	J10	132	R15	I/O	ST	
RK6	M13	131	T18	I/O	ST	
RK7	M12	130	T17	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-7: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Timer1 through Timer9						
T1CK	D13	161	H18	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar						
RTCC(1)	H3	79	V5	O	—	Real-Time Clock Alarm/Seconds Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: RTCC pin function in not available during VBAT operation.

TABLE 1-8: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Universal Asynchronous Receiver Transmitter 1						
U1RX	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	O	—	UART1 Transmit
$\overline{\text{U1CTS}}$	PPS	PPS	PPS	I	ST	UART1 Clear to Send
$\overline{\text{U1RTS}}$	PPS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2						
U2RX	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	O	—	UART2 Transmit
$\overline{\text{U2CTS}}$	PPS	PPS	PPS	I	ST	UART2 Clear To Send
$\overline{\text{U2RTS}}$	PPS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3						
U3RX	PPS	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	PPS	O	—	UART3 Transmit
$\overline{\text{U3CTS}}$	PPS	PPS	PPS	I	ST	UART3 Clear to Send
$\overline{\text{U3RTS}}$	PPS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4						
U4RX	PPS	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	PPS	O	—	UART4 Transmit
$\overline{\text{U4CTS}}$	PPS	PPS	PPS	I	ST	UART4 Clear to Send
$\overline{\text{U4RTS}}$	PPS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5						
U5RX	PPS	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	PPS	O	—	UART5 Transmit
$\overline{\text{U5CTS}}$	PPS	PPS	PPS	I	ST	UART5 Clear to Send
$\overline{\text{U5RTS}}$	PPS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6						
U6RX	PPS	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	PPS	O	—	UART6 Transmit
$\overline{\text{U6CTS}}$	PPS	PPS	PPS	I	ST	UART6 Clear to Send
$\overline{\text{U6RTS}}$	PPS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select