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## High Speed Translator Buffer to LVDS

### FEATURES

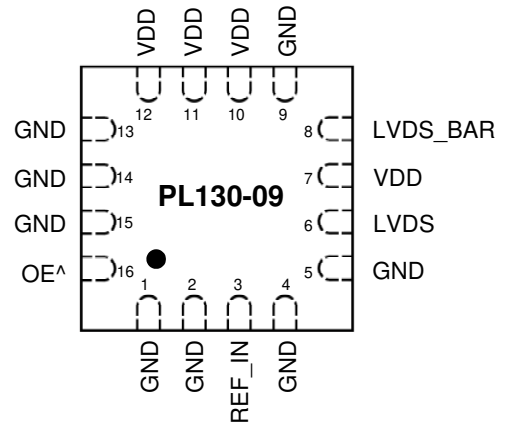
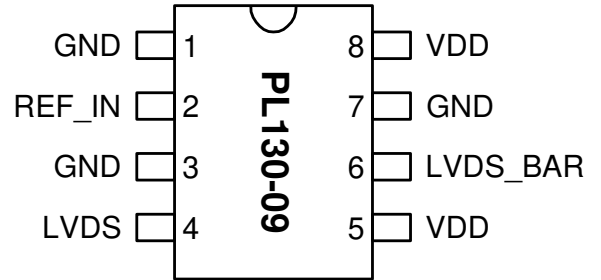
- Differential LVDS output
- Single AC coupled input (min. 100mV swing).
- Input range from 0 to 1.0GHz.
- 2.5V to 3.3V operation.
- Available in 8-Pin SOP or 3x3mm QFN GREEN/RoHS compliant packaging.

### DESCRIPTION

The PL130-09 is a low cost, high performance, high speed, buffer that reproduces any input frequency from 0 to 1.0GHz. It provides a pair of differential LVDS output. Any input signal with at least 100mV swing can be used as reference signal. This chip is ideal for conversion from sine wave, TTL, CMOS, or PECL to LVDS.

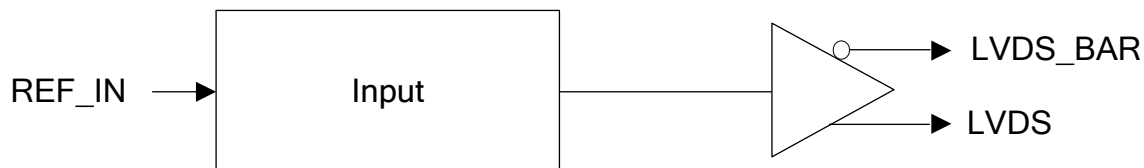
### PIN CONFIGURATION

(TOP VIEW)



Note: ^ denotes internal pull up

### BLOCK DIAGRAM



**High Speed Translator Buffer to LVDS**
**PIN DESCRIPTIONS**

Name	Pin Number		Type	Description
	SOP-8L	QFN-16L		
GND	1,3,7	1,2,4,5, 9,13,14,15	P	Ground.
VDD	5,8	7,10,11,12	P	Power supply.
REF_IN	2	3	I	Reference input signal. The frequency of this signal will be reproduced at the output (after translation to LVDS level).
LVDS	4	6	O	LVDS True output.
LVDS_BAR	6	8	O	LVDS Complementary output.
OE	N/A	16	I	Output enable ('1' for enable). Internal pull-up (default is '1').

**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_i$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_o$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_s$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_j$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. \*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

**2. General Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, No Load	$I_{DD}$	$F_{out} = 200\text{MHz}$ , LVDS		25	30	mA
Operating Voltage	$V_{DD}$		2.25		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	±5% of input			%
Short Circuit Current				±50		mA

**High Speed Translator Buffer to LVDS**
**3. AC Specifications**

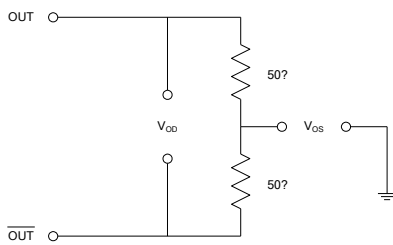
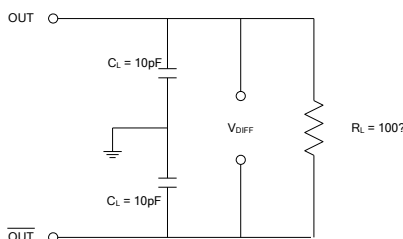
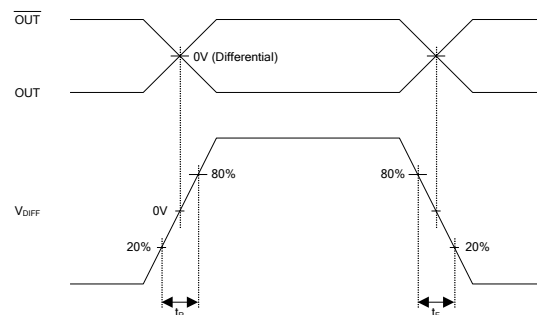
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		0		1000	MHz
Input signal swing	REF_IN input	100			mV
Output Frequency		0		1000	MHz

**4. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND, $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

**5. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

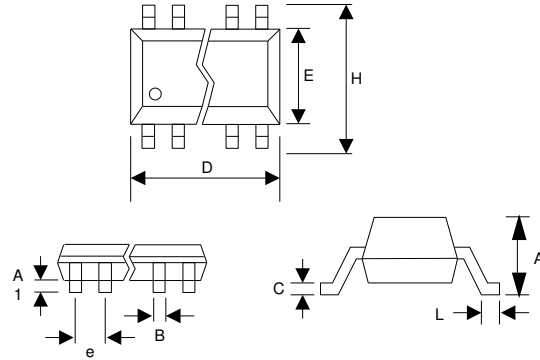
**LVDS Levels Test Circuit**

**LVDS Switching Test Circuit**

**LVDS Transition Time Waveform**


## High Speed Translator Buffer to LVDS

### PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

8 PIN SOP ( dimensions in mm )

SOP-8L		
Symbol	Min.	Max.
A	1.47	1.73
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	4.95
E	3.80	4.00
H	5.80	6.20
L	0.38	1.27
e	1.27 BSC	



VARIATIONS:

SYMBOL	QFN-16L		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		

