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PL135-27

Low Power, 1.62V to 3.63V, 10MHz to 40MHz, 1:2 Oscillator Fanout Buffer

Revision 2.0

General Description

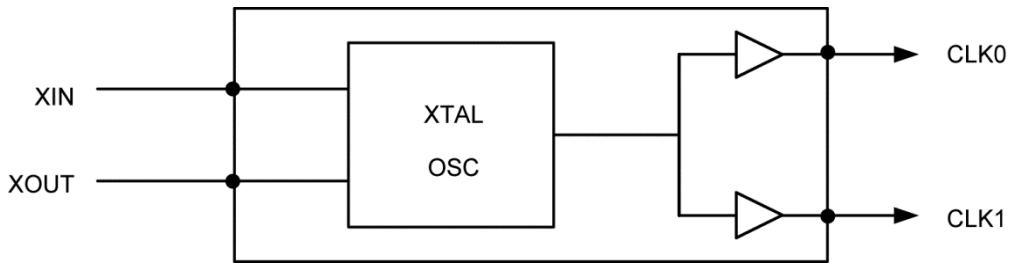
The PL135-27 is an advanced oscillator fanout buffer design for high performance, low-power, small form-factor applications. The PL135-27 accepts a fundamental crystal input of 10MHz to 40MHz and produces two LVCMOS outputs of the same frequency. The PL135-27 is designed to fit in a small 2mm × 1.3mm DFN package and offers the best phase noise, jitter performance and lowest power consumption of any comparable IC.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- Advanced oscillator design for wide frequency coverage
- Two LVCMOS outputs
- 8mA output drive strength
- Input/output frequency: 10MHz to 40MHz fundamental crystal
- Very low jitter and phase noise
- Low current consumption
- Single 1.62V to 3.63V power supply
- Available in 2.0mm × 1.3mm DFN-6L, GREEN/RoHS-compliant package

Block Diagram



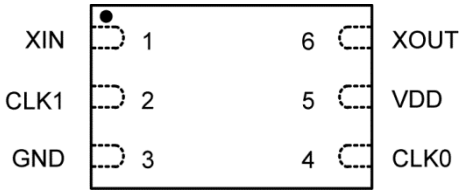
Ordering Information

Part Number	Ambient Temperature Range	Marking[1]	Package
PL135-27GC-R	0°C to +70°C	J27 LLL	6-Pin 2.0mm × 1.3mm DFN
PL135-27GI-R	-40°C to +85°C		

Note:

1. LLL designates lot number.

Pin Configuration



6-Lead DFN

Pin Description

Pin Number DFN-6L	Pin Name	Type	Pin Description
1	XIN	I	Crystal input
2	CLK1	O	Clock output
3	GND	P	GND connection
4	CLK0	O	Clock output
5	VDD	P	V_{DD} connection
6	XOUT	O	Crystal output

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Absolute Maximum Ratings[2]

Supply Voltage (V_{DD}) ..... –0.5V to +4.6V
Output Voltage (V_{OUT}) ..... –0.5V to V_{DD}+0.5V
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[3]

Supply Voltage (V_{DD}) ..... +1.62V to +3.63V
Ambient Temperature (T_A) ..... –40°C to +85°C

AC Electrical Characteristics

V_{DD} = 1.8V ±10%, 2.5V ±10% or 3.3V ±10%; C_L = 15pF; T_A = -40°C to +85°C, unless otherwise noted

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_X	Crystal Input Frequency	Fundamental crystal	10		40	MHz
t_{SETTLE}	Settling Time	At Power-Up ($V_{DD} \geq$ 1.62V)			2	ms
dF/dV_{DD}	V_{DD} Sensitivity	Frequency vs. V_{DD}, ±10%	-0.5		0.5	ppm
t_R	Output Rise Time	10/90% V_{DD}, V_{DD}=3.3V		2	3	ns
t_F	Output Fall Time	90/10% V_{DD}, V_{DD}=3.3V		2	3	ns
t_{SKEW}	Output to Output Skew				500	ps
D-C	Duty Cycle		45	50	55	%

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. The device is not guaranteed to function outside its operating ratings.

DC Electrical Characteristics

V_{DD} = 1.8V ±10%, 2.5V ±10% or 3.3V ±10%; C_L = 15pF; T_A = -40°C to +85°C, unless otherwise noted

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DD}	Supply Current, Dynamic	V_{DD} = 3.3V, 25MHz, No Load		1.6		mA
		V_{DD} = 2.5V, 25MHz, No Load		1.2		mA
		V_{DD} = 1.8V, 25MHz, No Load		0.9		mA
V_{DD}	Operating Voltage		1.62		3.63	V
V_{OL}	Output Low Voltage	I_{OL} = +4mA, 3.3V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, 3.3V	2.4			V
I_{OSD}	Output Current	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA

Crystal Specifications

V_{DD} = 1.8V ±10%, 2.5V ±10% or 3.3V ±10%; C_L = 15pF; T_A = -40°C to +85°C, unless otherwise noted

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{XIN}	Fundamental Crystal Resonator Frequency		10		40	MHz
$C_{L(xtal)}$	Crystal Loading Rating			12		pF
P_D	Operating Drive Level			0.1	2	mW
C0	Shunt Capacitance				5.5	pF
ESR	Effective Series Resistance	C0 ≤ 5.5pF			40	Ω
		C0 ≤ 2.5pF			60	Ω

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Layout Recommendations

The following guidelines are to assist you with a performance optimized PCB design:

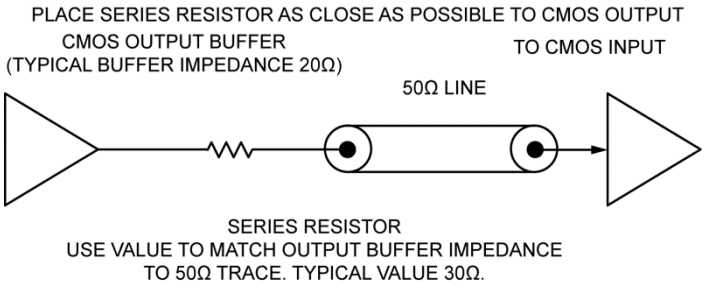
Signal Integrity and Termination Considerations

- Keep traces short.
- Trace = Inductor. With a capacitive load this equals ringing.
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

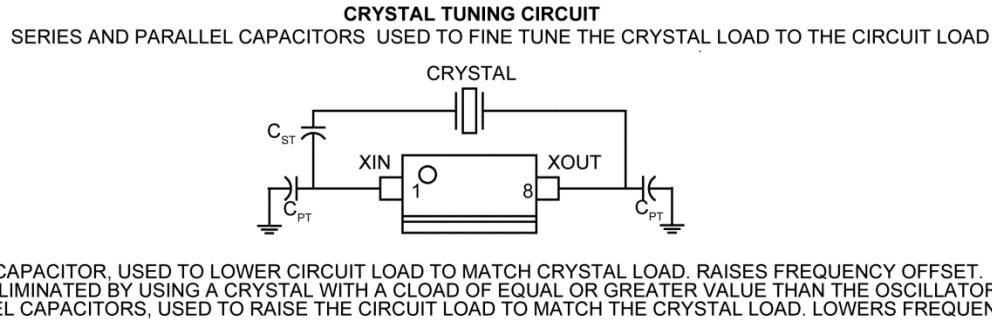
Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Multiple VDD pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependent. Typical value to use is 0.1µF.

TYPICAL CMOS TERMINATION



CRYSTAL TUNING CIRCUIT



CST – SERIES CAPACITOR, USED TO LOWER CIRCUIT LOAD TO MATCH CRYSTAL LOAD. RAISES FREQUENCY OFFSET.
THIS CAN BE ELIMINATED BY USING A CRYSTAL WITH A CLOAD OF EQUAL OR GREATER VALUE THAN THE OSCILLATOR.
CPT – PARALLEL CAPACITORS, USED TO RAISE THE CIRCUIT LOAD TO MATCH THE CRYSTAL LOAD. LOWERS FREQUENCY OFFSET.

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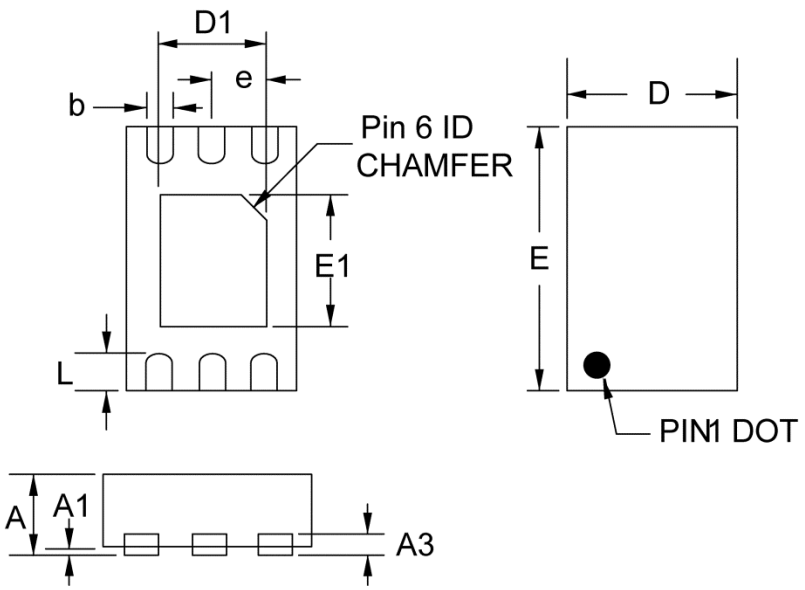
Package Information[4]

Symbol	Dimension in MM	
	Min.	Max.
A	0.45	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



6-Lead DFN

Note:

4. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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