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### PL135-27



# Low Power, 1.62V to 3.63V, 10MHz to 40MHz, 1:2 Oscillator Fanout Buffer

Revision 2.0

### **General Description**

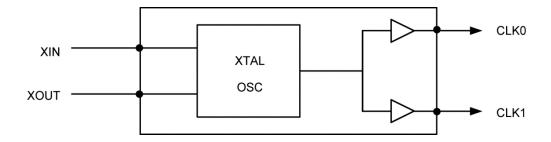
The PL135-27 is an advanced oscillator fanout buffer design for high performance, low-power, small form-factor applications. The PL135-27 accepts a fundamental crystal input of 10MHz to 40MHz and produces two LVCMOS outputs of the same frequency. The PL135-27 is designed to fit in a small 2mm × 1.3mm DFN package and offers the best phase noise, jitter performance and lowest power consumption of any comparable IC.

Datasheets and support documentation are available on Micrel's web site at: <a href="https://www.micrel.com">www.micrel.com</a>.

### **Features**

- Advanced oscillator design for wide frequency coverage
- Two LVCMOS outputs
- · 8mA output drive strength
- Input/output frequency: 10MHz to 40MHz fundamental crystal
- Very low jitter and phase noise
- Low current consumption
- Single 1.62V to 3.63V power supply
- Available in 2.0mm x 1.3mm DFN-6L, GREEN/RoHScompliant package

### **Block Diagram**



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# **Ordering Information**

Part Number	Ambient Temperature Range	Marking <sup>(1)</sup>	Package
PL135-27GC-R	0°C to +70°C	J27	6 Din 2 Omm 1 2mm DEN
PL135-27GI-R	-40°C to +85°C	LLL	6-Pin 2.0mm × 1.3mm DFN

### Note:

# **Pin Configuration**



6-Lead DFN

# **Pin Description**

Pin Number DFN-6L	Pin Name	Туре	Pin Description
1	XIN	I	Crystal input
2	CLK1	0	Clock output
3	GND	Р	GND connection
4	CLK0	0	Clock output
5	VDD	Р	V <sub>DD</sub> connection
6	XOUT	0	Crystal output

<sup>1.</sup> LLL designates lot number.

# Absolute Maximum Ratings<sup>(2)</sup>

# Operating Ratings<sup>(3)</sup>

Supply Voltage (V <sub>DD</sub> )	0.5V to +4.6V
Output Voltage (V <sub>OUT</sub> )	
Storage Temperature (T <sub>S</sub> )	65°C to +150°C

Supply Voltage (V <sub>DD</sub> )	+1.62V to +3.63V
Ambient Temperature (T <sub>A</sub> )	40°C to +85°C

### **AC Electrical Characteristics**

 $V_{DD} = 1.8V \pm 10\%$ , 2.5V  $\pm 10\%$  or 3.3V  $\pm 10\%$ ;  $C_L = 15pF$ ;  $T_A = -40$ °C to +85°C, unless otherwise noted

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
F <sub>X</sub>	Crystal Input Frequency	Fundamental crystal	10		40	MHz
t <sub>SETTLE</sub>	Settling Time	At Power-Up (V <sub>DD</sub> ≥ 1.62V)			2	ms
dF/dV <sub>DD</sub>	V <sub>DD</sub> Sensitivity	Frequency vs. V <sub>DD</sub> , ±10%	-0.5		0.5	ppm
t <sub>R</sub>	Output Rise Time	10/90% V <sub>DD</sub> , V <sub>DD</sub> =3.3V		2	3	ns
t <sub>F</sub>	Output Fall Time	90/10% V <sub>DD</sub> , V <sub>DD</sub> =3.3V		2	3	ns
t <sub>SKEW</sub>	Output to Output Skew				500	ps
D-C	Duty Cycle		45	50	55	%

#### Notes:

- 2. Exceeding the absolute maximum ratings may damage the device.
- 3. The device is not guaranteed to function outside its operating ratings.

### **DC Electrical Characteristics**

 $V_{DD} = 1.8V \pm 10\%$ , 2.5V  $\pm 10\%$  or 3.3V  $\pm 10\%$ ;  $C_L = 15pF$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
		V <sub>DD</sub> = 3.3V, 25MHz, No Load		1.6		mA
$I_{DD}$	Supply Current, Dynamic	V <sub>DD</sub> = 2.5V, 25MHz, No Load		1.2		mA
		V <sub>DD</sub> = 1.8V, 25MHz, No Load		0.9		mA
V <sub>DD</sub>	Operating Voltage		1.62		3.63	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +4mA, 3.3V			0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, 3.3V	2.4			V
I <sub>OSD</sub>	Output Current	$V_{OL} = 0.4V, V_{OH} = 2.4V$	8			mA

## **Crystal Specifications**

 $V_{DD} = 1.8V \pm 10\%$ , 2.5V  $\pm 10\%$  or 3.3V  $\pm 10\%$ ;  $C_L = 15pF$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
F <sub>XIN</sub>	Fundamental Crystal Resonator Frequency		10		40	MHz
C <sub>L(xtal)</sub>	Crystal Loading Rating			12		pF
P <sub>D</sub>	Operating Drive Level			0.1	2	mW
C0	Shunt Capacitance				5.5	pF
ESR	Effective Series Resistance	C0 ≤ 5.5pF			40	Ω
		C0 ≤ 2.5pF			60	Ω

### **Layout Recommendations**

The following guidelines are to assist you with a performance optimized PCB design:

#### Signal Integrity and Termination Considerations

- Keep traces short.
- Trace = Inductor. With a capacitive load this equals ringing.
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as "striplines" or "microstrips" with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

### **Decoupling and Power Supply Considerations**

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Multiple VDD pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependent.
   Typical value to use is 0.1µF.

#### **TYPICAL CMOS TERMINATION**

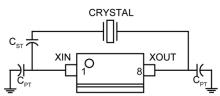
PLACE SERIES RESISTOR AS CLOSE AS POSSIBLE TO CMOS OUTPUT CMOS OUTPUT BUFFER TO CMOS INPUT (TYPICAL BUFFER IMPEDANCE 20Ω)

SERIES RESISTOR
USE VALUE TO MATCH OUTPUT BUFFER IMPEDANCE

# TO $50\Omega$ TRACE. TYPICAL VALUE $30\Omega$ .

#### **CRYSTAL TUNING CIRCUIT**

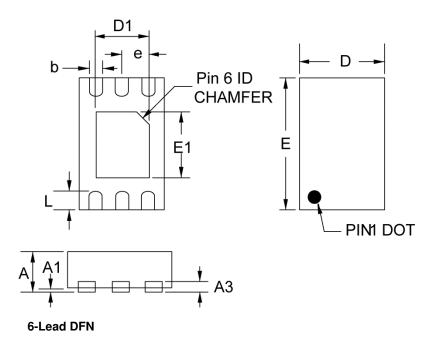
SERIES AND PARALLEL CAPACITORS USED TO FINE TUNE THE CRYSTAL LOAD TO THE CIRCUIT LOAD



CST – SERIES CAPACITOR, USED TO LOWER CIRCUIT LOAD TO MATCH CRYSTAL LOAD. RAISES FREQUENCY OFFSET. THIS CAN BE ELIMINATED BY USING A CRYSTAL WITH A CLOAD OF EQUAL OR GREATER VALUE THAN THE OSCILLATOR. CPT – PARALLEL CAPACITORS, USED TO RAISE THE CIRCUIT LOAD TO MATCH THE CRYSTAL LOAD. LOWERS FREQUENCY OFFSET.

# Package Information<sup>(4)</sup>

Symbol	Dimension in MM		
Symbol	Min.	Max.	
Α	0.45	0.60	
A1	0.00	0.05	
A3	0.152	0.152	
Ь	0.15	0.25	
е	0.40BSC		
D	1.25	1.35	
Е	1.95	2.05	
D1	0.75	0.85	
E1	0.95	1.05	
L	0.20	0.30	



#### Note:

4. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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